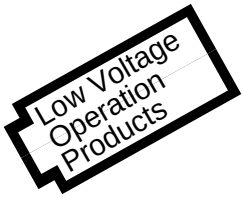
EPSON

SLA100X Series

Low Voltage Gate Array



- **Low Power Silicon Gate CMOS**
- **Low Operating Voltages**
- **CMOS-Compatible I/O**
- **Low Voltage Operational Oscillator on Chip**

■ DESCRIPTION

The SLA100X series gate arrays are fabricated utilizing our low threshold CMOS technology. Six devices, with raw gates ranging from 1,530 gates up to 7,750 gates, are available in a range of packages. All devices have level-shifter and low-power oscillator on chip.

Designers can select 3.0V or 1.5V operation, making the devices in this series ideal for portable equipment and other low and very-low power applications. Eight power / ground pins are dedicated.

SLA100X series LSIs can be designed with the same schematic capture and simulation tools as the SEIKO EPSON SLA9000F series gate arrays.

■ FEATURES

- Channeled Array
- Adopting 2.0μm silicon gate CMOS with 2-metal layers
- Low power consumption (V_{DD} = 0.9V to 6.0V)
- Available dual-power supplies (built-in level shift circuit)
- Available built-in oscillator circuit

■ PRODUCT LINEUP

Features \ Master		SLA115X	SLA121X	SLA132X	SLA147X	SLA159X	SLA177X
Total BCs (Raw Gates)		1,530	2,108	3,276	4,704	5,980	7,750
Usable BCs		1,300	1,786	2,784	3,998	5,083	6,587
Number of PADs		78	90	112	136	158	178
Number of I/O PADs		70	82	104	128	150	170
Number of Power Supply Pins		8	8	8	8	8	8
Propagation Delay Coefficient		The coefficient value is calculated by multiplying the coefficient value of Max. or Min. for Typ. value for VDD = 1.5V described in the SLA100X series MSI CELL Library by lowest value or highest value of using voltage. For more information about the coefficient value, contact our sales office for technical support.					
Propagation Delay	Internal Gates	tpd = 8.5ns (standard at 1.5V), tpd = 3.0ns (standard at 3.0V)					
	Input Buffers	tpd = 12.0ns (standard at 1.5V), tpd = 4.0ns (standard at 3.0V)					
	Output Buffers	tpd = 40.0ns (standard at 1.5V), tpd = 14.0ns (standard at 3.0V) CL = 50pF					
I/O Level		CMOS					
Input Mode		CMOS, Pull-up/Pull-down, Schmitt, Dual power level interface (Level shifter)					
Output Mode		Normal, Open drain, 3-state, Bi-directional, Dual power level interface (Level shifter)					

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Rating	Symbol	Value	Unit
Supply voltage	$V_{DD1,2}$	– 0.5 to 7.0	V
Input voltage	V_I	– 0.5 to $V_{DD1,2}$+0.5	V
Output voltage	V_O	– 0.5 to $V_{DD1,2}$+0.5	V
Storage temperature	T_{stg}	– 65 to 150	°C

■ RECOMMENDED OPERATING CONDITIONS

Condition	Symbol	Remark	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD1}	1.5V	1.35	1.50	1.65	V
	V_{DD2}	3V (V_{DD1}=1.5V)	2.70	3.00	3.30	V
	V_{DD1}	3V	2.70	3.00	3.30	V
	V_{DD2}	5V (V_{DD1}=3.0V)	4.50	5.00	5.50	V
Operating voltage	$V_{DD1,2}$		0.90	–	6.00	V
Operating temperature	Topr		0	–	70	°C

Note: Please contact your local SEIKO EPSON sales representative to operate at V_{DD1}=1.5V and/or V_{DD2}=5.0V.

■ ELECTRICAL CHARACTERISTICS

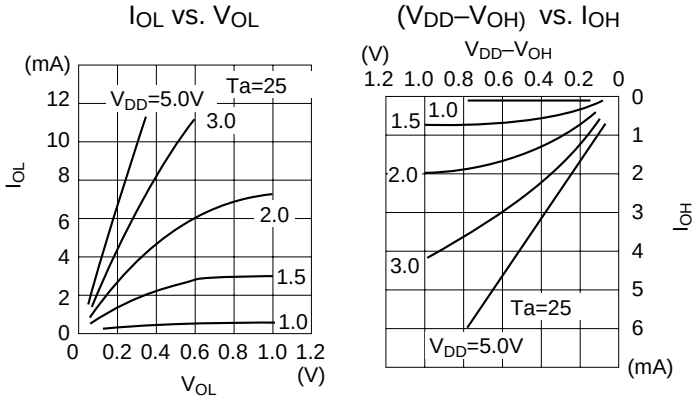
(Ta=0 to 70°C)

Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Standby supply current	I_{DDS1}	Static state, V_{DD1}=1.5V	–	–	200	nA
	I_{DDS1}	Static state, V_{DD1}=3.0V	–	–	1.0	µA
	I_{DDS2}	Static state, V_{DD2}=3.0V Per one level shifter	–	–	90	nA
	I_{DDS2}	Static state, V_{DD2}=5.0V Per one level shifter	–	–	100	nA
High level output volrage	V_{OH}	V_{DD1}=1.5V, I_{OH}= – 0.23mA	1.3	–	–	V
	V_{OH}	$V_{DD1,2}$=3.0V, I_{OH}= – 0.6mA	2.7	–	–	V
	V_{OH}	V_{DD2}=4.5V, I_{OH}= – 1.2mA	4.1	–	–	V
Low level output voltage	V_{OL}	V_{DD1}=1.5V, I_{OL}=0.7mA	–	–	0.2	V
	V_{OL}	$V_{DD1,\ 2}$=3.0V, I_{OL}=1.9mA	–	–	0.3	V
	V_{OL}	V_{DD2}=4.5V, I_{OL}=4.0mA	–	–	0.4	V
High level input voltage	V_{IH}	V_{DD1}=1.5V	1.25	–	–	V
	V_{IH}	$V_{DD1,2}$=3.0V	2.40	–	–	V
	V_{IH}	V_{DD2}=5.0V	3.5	–	–	V
Low level input voltage	V_{IL}	V_{DD1}=1.5V	–	–	0.25	V
	V_{IL}	$V_{DD1,2}$=3.0V	–	–	0.60	V
	V_{IL}	V_{DD2}=5.0V	–	–	1.5	V
Input leakage current	I_{LI}		–1	–	1	µA

NOTE: I_{DD2} is voltage supplied from V_{DD2} for I/O cell using level shifter.
V_{DD1}: Supply voltage for MSI on chip.
V_{DD2}: External voltage.
$V_{DD2} \geq V_{DD1}$

■ CHARACTERISTICS CURVES

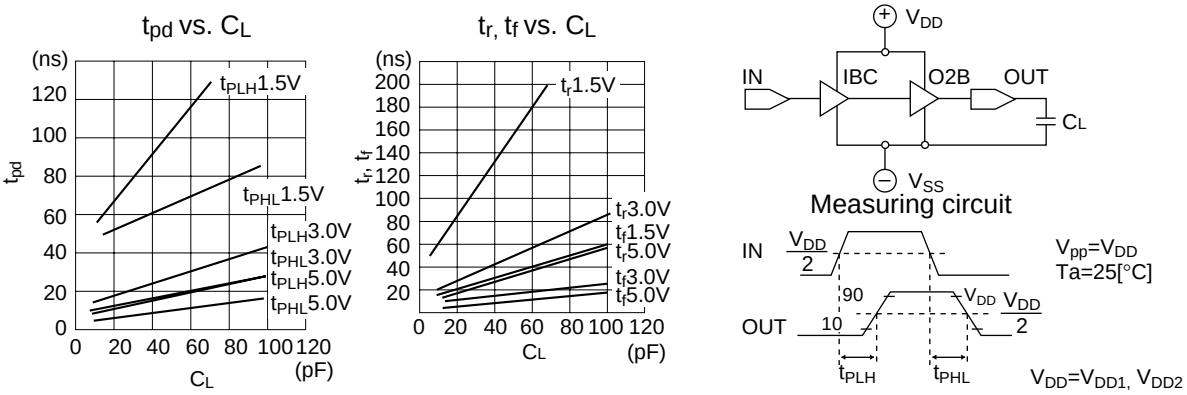
● Output Current



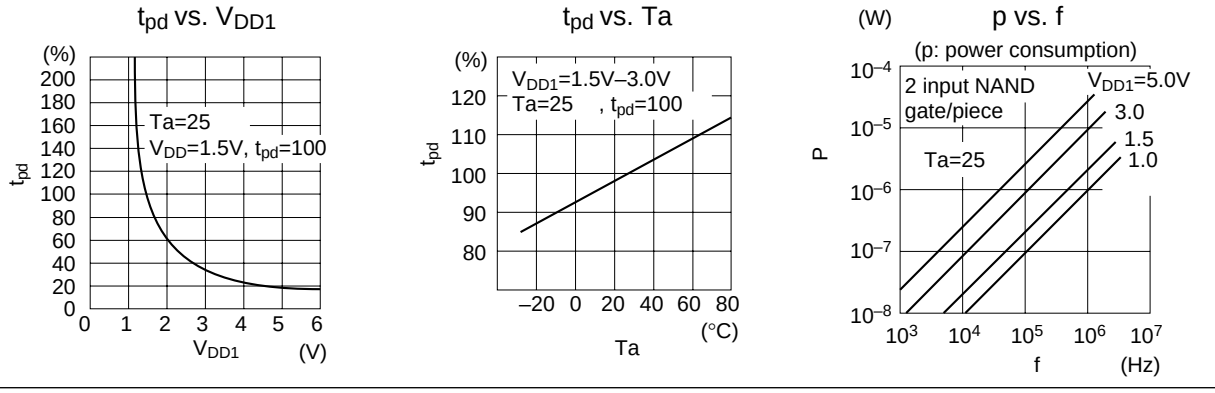
	I_{OH}(mA)	I_{OL}(mA)
TYPE1	–0.2	0.6
TYPE2	–0.6	1.9
TYPE3	–1.2	1.9

$V_{DD}=V_{DD1}, V_{DD2}$

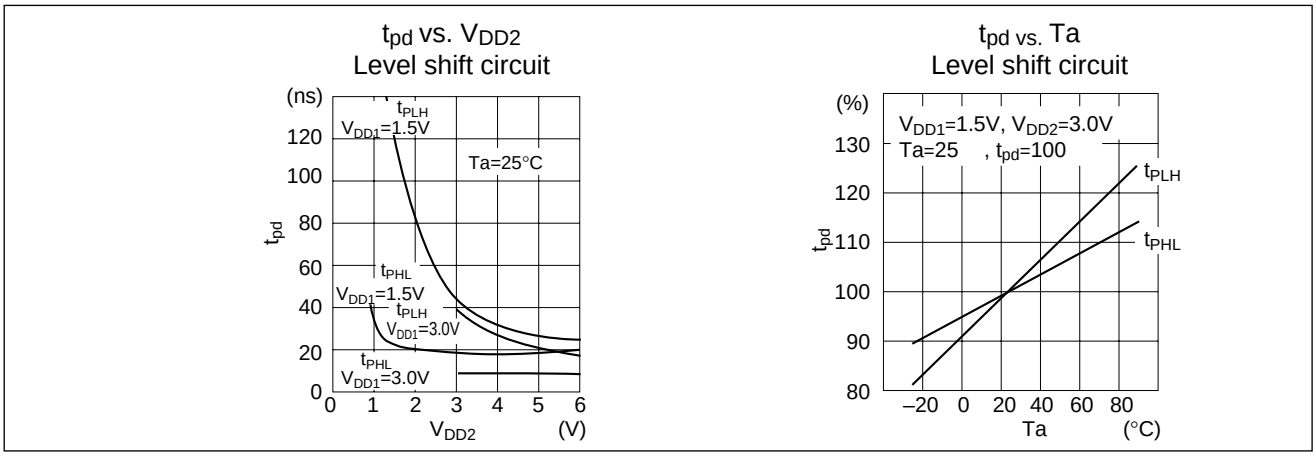
● t_{pd}, t_r, t_f –C_L



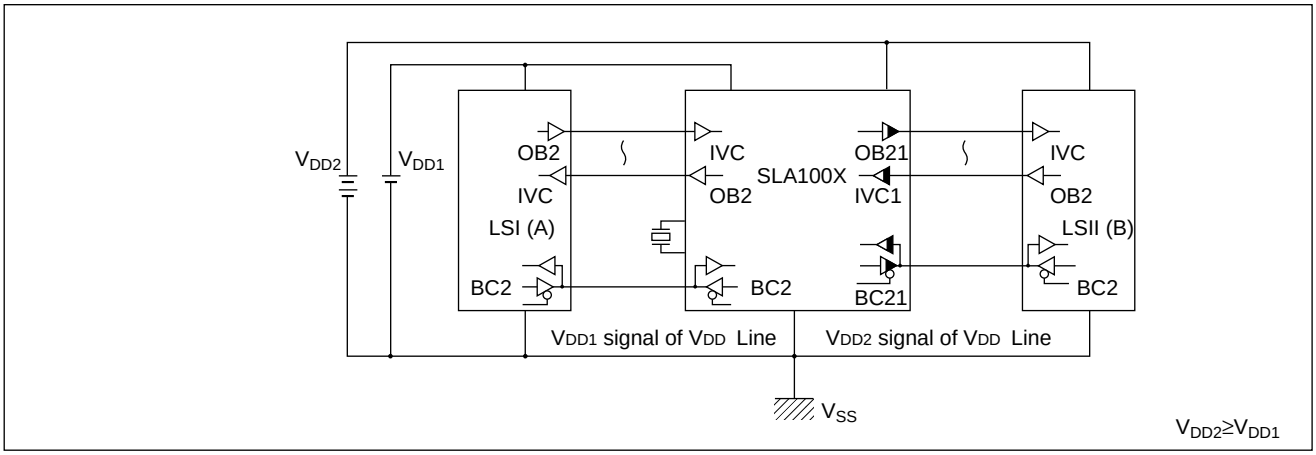
● Propagation delay, Power consumption



● Propagation delay Characteristics for Level Shift Circuit



■ INTERFACE EXAMPLE FOR LEVEL SHIFT CIRCUIT



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