ZAMBEZI

ADVANCE PRODUCT BRIEF

1536 x 1536 STS-1 Grooming Switch Fabric

Features

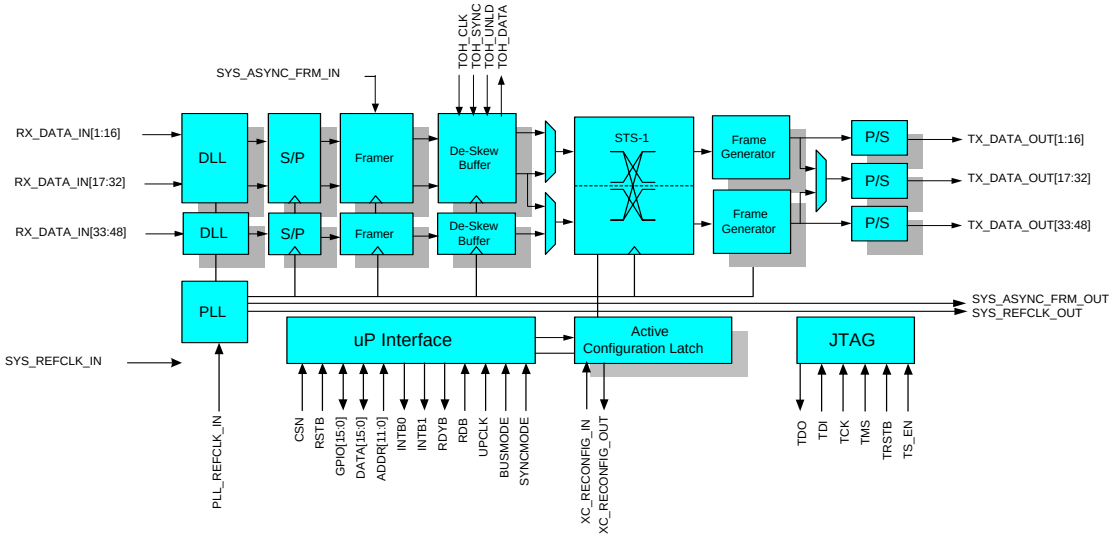
- 1536 x 1536 (80G) STS-1 Time Slot Interchange (TSI) Switch Fabric.
- Dual 768 x 768 (40G) logical-partitioning of the switch fabric allowing a single element to be used as the 1st and Nth stages of a larger, multistage, system switch.
- Dual-casted ouputs/inputs to drive, actively monitor, and seamlessly switch between redundant core stage switches.
- 48 x 48 serial STS-48/STM-16 or STS-12/STM-4 phase compensated inputs/outputs. Selectable on a per input/output basis.
- Single-stage, non-blocking, switch architecture.
- Frame synchronous deskew on all inputs.
- SONET/SDH framers with B1, OOF, LOF, and J0/Z0 monitoring on each input for data-integrity checking. Optional J0/Z0 insertion and B1 recalculation on TX frame generators.
- Processes all valid-input combinations of STS-48c/AU-4-16c, STS-12c/AU-4-4c, STS-3c/AU-4, or STS-1/AU-3 signals within an STS-48/STM-16 or STS-12/STM-4.
- Supports STS-192c/AU-4-64c and STS-768c/AU-4-256c, inverse, multiplexed inputs by path grouping.
- Unconstrained, *n*-by, multicast capability.
- Coordinated, seamless (non-glitching), TSI switching, within a device and across multistage elements.
- Internally biased, 100 ohm, line-to line terminations on high-speed, differential inputs.
- CML ouputs with programmable, output, swing control and pre-emphasis for optimal, signal, integrity control.
- Packaged in a 33mm x 33mm 624 PBGA.
- 8W, typical-power dissipation.
- I/O power-down of unused inputs.
- 0.13u CMOS technology.

Overview and Applications

Transport Hierarchy

The S8710 is a TSI providing SONET/SDH grooming at the STS-1 level. It can be configured as either a single-stage 1536 x 1536 (80G), STS-1 switch or a logically-subdivided, dual, 768 x 768 (40G each), STS-1 switch. The core of the switch fabric is a single-stage, monolithic, non-blocking architecture allowing any STS-*N*c tributary from any of the STS-48/STM-16 serial-input streams to be switched to any STS-*N*c tributaries in any of the STS-48/STM-16 serial-output streams. Any number of STS-*Nc* inputs can be multicast to any or all of the ouputs.

S8710PBGA Block Diagram



AMCC

200 Minuteman Park, Andover, MA 01810 Ph: 978-623-0009 Fax: 978-623-0024

1536 x 1536 STS-1 Grooming Switch Fabric

ADVANCE PRODUCT BRIEF

The S8710 is ideally suited for large, multistage, TSI fabrics for which it can reside either on the line card or on the center-stage, switch card. When resident on the line card, the switch can be logically subdivided to operate as both the 1st- and Nth-stage switches. Sixteen, I/O ports can be dual-casted, allowing it to directly drive and monitor redundant, core-stage, switch elements. Switching between the redundant-line interfaces is always seamless.

When combined with other AMCC products like Missouri, Danube, Mekong, Ohio, or Indus, the S8710 provides a complete, digital, cross-connect solution.

SONET Processing

The S8710 implements SONET/SDH framing and monitoring functions for up to 48 STS-48/STM-16 data streams. It can support any combination of STS-48c/AU-4-16c, STS-12c/AU-4-4c, STS-3c/AU-4, and/or STS-1/AU-3 signals within an STS-48/STM-16. Additionally, inverse-multiplexed, SONET/SDH STS-192c/AU-4-64c and SONET/SDH STS-768/AU-4-256c data-streams are processed and monitored across multiple inputs. Concatenated streams are grouped and switched through the fabric as contiguous or striped STS-1s.

Link integrity-monitoring includes B1, J0/Z0, OOF, and LOF by the RX framers. J0/Z0 can also be inserted at the TX framer to ensure proper switch configuration.

The S8710 is SONET and SDH standards-compliant with TELCORDIA GR-253-CORE, GR-499, ITU G.707, and G.783.

Input/Outputs

The input logic, including the clock-recovery circuits, and the deserializing and framing circuits, can be configured on a per-line basis to operate at either 2.488GHz (STS-48/STM-16) rates or at 622.08MHz (STS-12/STM-4) rates. Operating the inputs or outputs at the lower rate will, however, result in an incremental reduction in the overall bandwidth of the switch. In the extreme case (all I/Os operating at 622MHz), the total-aggregate bandwidth of the switch fabric is reduced to 20G.

The S8710 is a synchronous switch. Because of this, all of the input streams must be frequency-locked (pointer processed) and loosely frame-aligned prior to switching. Plesiochronous and/or sub-rate tributaries can be aggregated and conditioned using AMCC's Missouri or Danube. STS-192/STM-64 channelized streams can be interfaced to the switch fabric using AMCC's Indus or Mekong pointer processor.

The S8710 uses DLL technology to bit-align the serial-input streams. The I/Os have high-jitter tolerance (0.6UI) and can tolerate low-frequency wander (+/- 20ppm) resulting from transmission line-effects, thermal effects, and clock wander within a distributed system.

The ouputs are CML and have programmable, swing control, and also support 4 levels of pre-emphasis for optimizing power and signal-integrity control.

Framing

In the receive direction, once the serial streams have been bit aligned, the data rate is reduced using a serial/parallel converter and then framed. B1 integrity checking, OOF, LOF, and J0/Z0 section trace ensure the quality and connectivity of the transmission path to the switch ingress-port. The SONET/SDH signal is descrambled and then demultiplexed into its constituent tributaries. The tributaries are then processed through the switch fabric according to the connections defined in the active, configuration, control register.

In the transmit direction, the STS-*N* constituents are multiplexed into a SONET/SDH STS-48/STM-16 frame. The S8710 then recalculates B1 and optionally inserts J0/Z0. Data is output serially at either 622.08MHz or 2.488GHz.

TOH Drop

In addition to basic SONET/SDH monitoring, an inband communication-channel can be established between upstream devices and the S8710 using any of the SONET/SDH TOH byte locations. A single byte from each STS-1 TOH can be read by the S8710. 1536 bytes can be read over 12-frame intervals.

Cross-Connect

For all types of traffic, the S8710 provides a fully, non-blocking, single, 1536 x 1536 or dual, 768 x 768, STS-1 level, cross-connect. The cross-connect is configured through the microprocessor port interface. There are 4 configuration images available to control the switch fabric. The active-configuration image defines the current connections through the switch. The other images can be used for protection or for defining future configurations. The alternate image's contents are transferred to the active image upon a reconfiguration command, which is synchronized with a SONET/SDH frame-boundary. A new image can be programmed into the secondary configuration without affecting the current switch configuration.

Buffering is provided within the switch fabric to ensure seamless switching upon reconfiguration.For multistage configurations, a reconfigureable, non-blocking algorithm is used to reconfigure the STS-1 paths within or between devices. The switch-over in all configurations is seamless.

AMCC

200 Minuteman Park, Andover, MA 01810 Ph: 978-623-0009 Fax: 978-623-0024

1536 x 1536 STS-1 Grooming Switch Fabric

ADVANCE PRODUCT BRIEF

Any STS-*N* from any STS-48/STM-16 input can be configured to any STS-*N* in any STS-48/STM-16 output for all types of traffic flows. Because the switch is a single-stage architecture, it is immune to *n*-by, multicast, blocking issues.

STS-192/STM-64 concatenated streams are processed through the switch fabric as 4, inverse-multiplexed, STS-48/STM-16, data streams. Path-grouping can be extended to support STS-768/STM-256 channelized- and concatenated-signals, as well.

Unused STS-1 tributaries within an STS-48/STM-16

Failed or undriven inputs are assigned AIS_P. Unassigned, STS-1 tributaries, within an STS-48/STM-16 output, are assigned as AIS_P.

Microprocessor Interface

The microprocessor port is a 16-bit, synchronous interface, used for device configuration, monitoring, and control functions. The S8710 supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt-driven or polled-mode configuration.

Physicals

The S8710 comes in a 33-mm sq, 624, PBGA package with a 1.2-mm ball pitch. It is built on a 0.13u CMOS process. All inputs are internally biased and terminated. All outputs are source-terminated CML, with programmable-swing and pre-emphasis control.

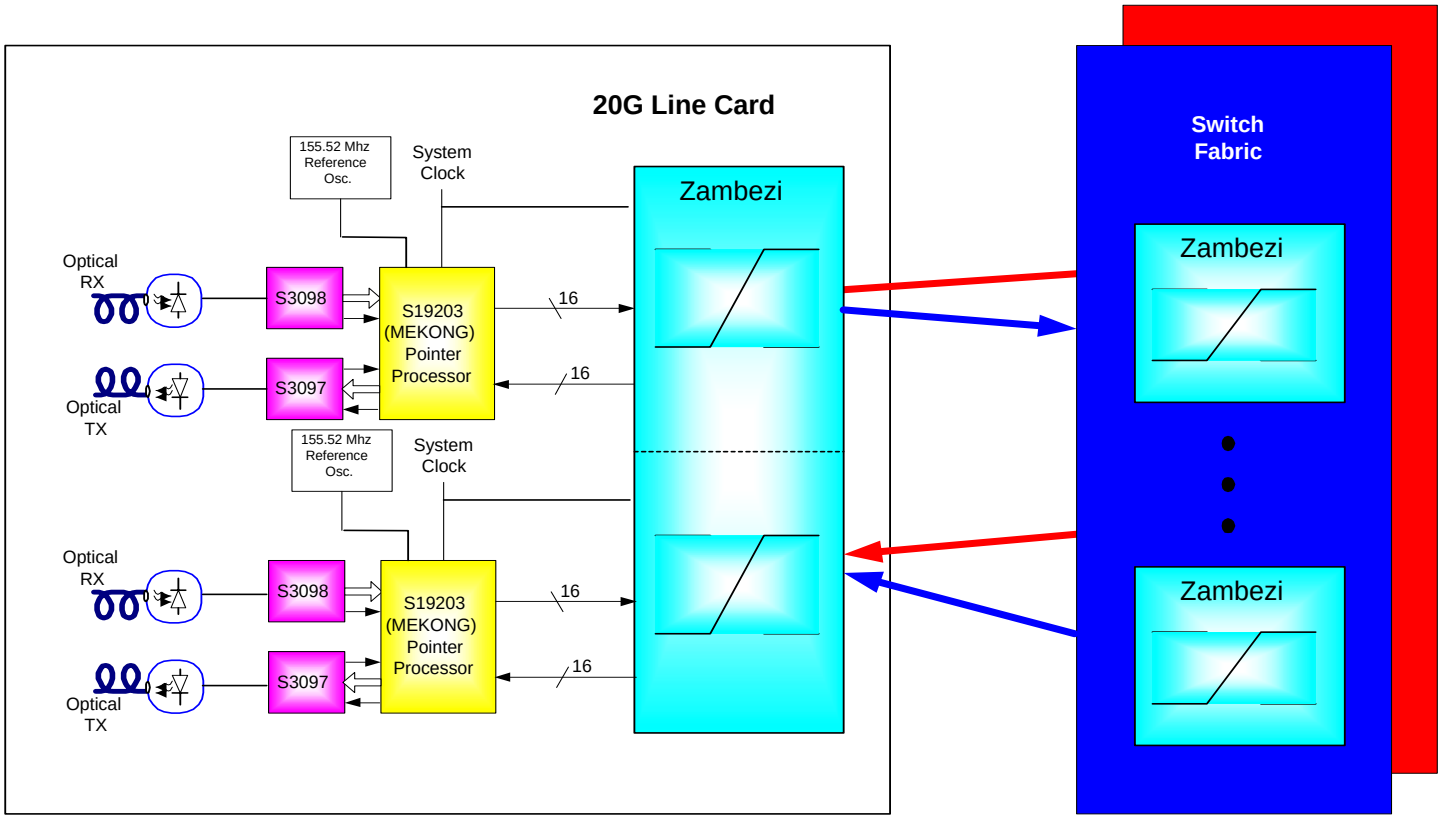


Figure 1. Multistage Switch Configuration

AMCC

200 Minuteman Park, Andover, MA 01810 Ph: 978-623-0009 Fax: 978-623-0024

1536 x 1536 STS-1 Grooming Switch Fabric

ADVANCE PRODUCT BRIEF

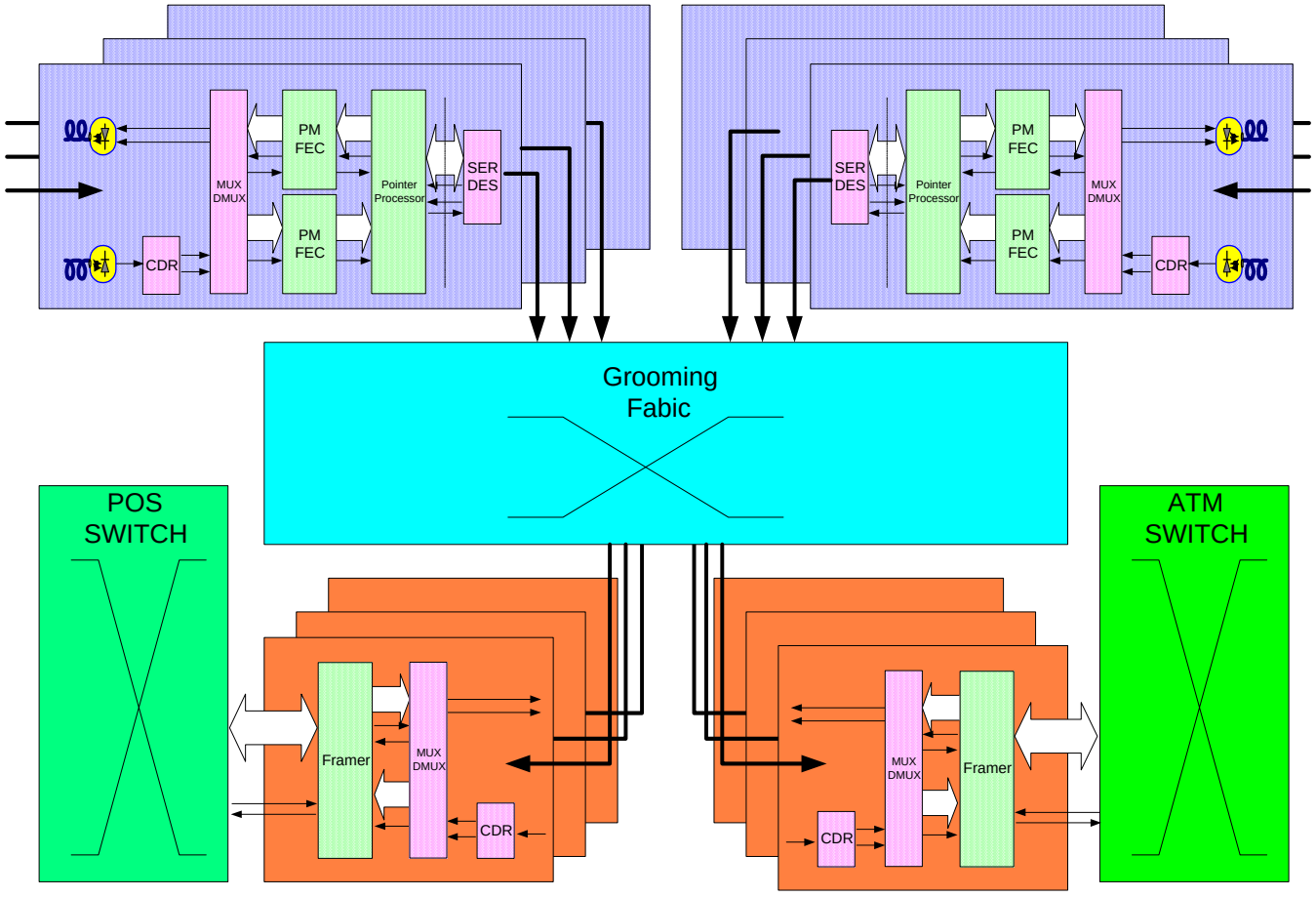


Figure 2. Termination application

AMCC
200 Minuteman Park, Andover, MA 01810 Ph: 978-623-0009 Fax: 978-623-0024