S-MOS SYSTEMS
A Seiko Epson Affiliate

Data Sheet

ASIC

PRELIMINARY

SLA9000F

SLA9000F Series

June 1996

■ DESCRIPTION

The S-MOS SLA9000F series is a family of sea-of-gates 0.6 micron gate arrays. The series consists of 8 arrays ranging from 2,784 to 44,070 usable gates and from 80 to 256 I/O. This series also has a built-in level shifter to provide dual-power interfacing in various low-voltage applications. Also, the micro-ampere order, low-noise output cells are available for portable equipment and instruments of various applications. The arrays are offered in a wide variety of packages from 44QFP up to 256QFP.

■ FEATURES

- Typical 2-input NAND Gate Delay (F/O = 2, Al = 2mm)

Voltage (V)	3.3V	5.0V
tpd (ns)	0.43	0.3

- Input buffer: 0.91 ns (5V Typ.), 1.08 ns (3.3V Typ.)
- Output buffer: 3.5 ns (5V Typ.), 4.2 ns (3.3V Typ.) (C_L = 50 pF)
- RAM blocks available (Async 1–2 port)
- Dual power supplies supported with level shifters
- Selectable supply voltages (5V, 3.3V)

■ PRODUCT CONFIGURATION

Array	SLA902F	SLA904F	SLA907F	SLA909F	SLA913F	SLA919F	SLA927F	SLA944F
Raw Gate	2,784	4,392	7,872	9,540	13,144	19,350	27,234	44,070
Utilization Rate	65%	65%	60%	60%	55%	55%	50%	50%
Usable Gate	1,809	2,854	4,723	5,724	7,229	10,642	13,617	22,035
Total PAD	80	100	128	144	160	184	208	256

■ ELECTRICAL CHARACTERISTICS AND SPECIFICATIONS OF THE SLA9000F SERIES

■ SLA9000F ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Limits	Unit
Power Supply Voltage	V_{DD}	−0.3 to 6.5	V
Input Voltage	V_I	−0.3 to V_{DD} + 0.5	V
Output Voltage	V_O	−0.3 to V_{DD} + 0.5	V
Output Current/Pin	I_{OUT}	±25 (±50*1)	mA
Storage Temperature	T_{STG}	−65 to 150	°C

Note: *1: Applies to the 24 mA output buffer cells

■ RECOMMENDED OPERATING CONDITIONS FOR THE SLA9000F SERIES

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Voltage	V_{DD}	2.70	3.00	3.30	V
		3.00	3.30	3.60	
		4.75	5.00	5.25	
		4.50	5.00	5.50	
Input Voltage	VI	V_{SS}	—	V_{DD}	V
Operating Temperature	T_{opr}	0	25	70	°C
		−40	25	85	°C

				Series	L902F	L904F	L907F	L909F	L913F	L919F	L927F	L944F
				Pads	80	100	128	144	160	184	208	256
				Raw Gates	2,784	4,392	7,426	9,540	13,144	19,350	27,234	44,070
				Usable Gates	1,810	2,855	4,156	5,724	7,229	10,643	13,617	22,035
PKG Type	Pin	PKG	Lead Materials	Lead Option								
	24		42		O							
Plastic DIP	28	DIP	42		O	O						
	40		42					O	O			
	42		42		O	O		O	O			
P.Shrink DIP	64	DIP	42		O							
	44	QFP4	42									
	44	QFP6	42		O	O	O	O		O		
	48	QFP12	42		O	O	O	O				
	52	QFP6	42		O	O	O	O	O			
	60	QFP5	42		O	O	O	O				
	60	QFP6	42		O	O	O	O				
	64	QFP5	42		O	O	O	O				
	64	QFP6	42	S1 only	O	O	O	O				
	64	QFP13	42		O	O	O	O				
	80	QFP5	42	S2	O	O	O	O				
	80	QFP14	42		O	O	O	O	O	O		
	100	QFP5	42	S2	O	O	O	O	O	O	O	
	100	QFP15	42			O	O	O	O	O	O	
	100	TQFP15	Cu			O	O	O	O	O	O	
Plastic QFP	120	QFP8	42	E1 • L2			O	O	O	O	O	
	120	QFP15	42					△	O	O	O	
			Cu						O	O	O	
	128	QFP5	42	S1 only			O	O	O	O	O	
	128	QFP8	42	E1			O					
	128	QFP15	42				O	O	O	O	O	
	128	QFP8	42	E1			O	O	O	O	O	
	128	QFP15	42				O	O	O	O	O	
			Cu							O	O	
	128	TQFP15	Cu				△	O	O	O	O	
	144	QFP17	42					O	O	O	O	O
	144	LQFP20	42					O	O	O	O	O
	160	QFP8	42	E1					O	O	O	O
	176	QFP16	42							O	O	O
	176	LQFP21#	Cu									
	184	QFP16	42									O
	184	QFP17	42							O	O	O
	184	LQFP20	42								△	O
	208	QFP8	42	S1						O	O	O
	208	LQFP22	Cu								O	O
	216	QFP21#	Cu									
	240	QFP16	42	S1 only								O
	256	QFP8	Cu	S3 only								O
	256	LQFP22#	Cu									
Plastic TSOP	28	TSOP (I)	42									
	24	SOP1	42		O	O						
Plastic SOP	28	SOP2	42		O	O						
	32	SOP6	42		O	O						
	52											
	44		Cu		O	O				O		
PLCC	68	PLCC	Cu		O	O	O	O				
	84	PLCC	Cu				O	O	O			

O: In volume production

△: Requires lead frame development (Reliability passed)

✱: Need reliability evaluation* (Possible to assy)

▲: Need reliability evaluation* (Requires lead frame development)

Shading: TS available (No Lead Options. Need to check Lead Frame stock.)

*: As a general rule, we accept an order reliability evaluation (Evaluation lead time: 3 months). Please contact Sales Dept. for further details.

#: Under Development

■ PROPAGATION DELAY TIMES

The progagation delay values printed in our cell libraries and used in simulation are derived from actual measurements of silicon, not spice simulations. The measured coefficient parameters are:

10% Factor
Voltage: 4.50 to 5.50 Volts
Temperature = –40 to 85°C

Name	Function	From	To	Best Case (10%)		Worst Case (10%)		Loads
				tplh (ns)	tphl (ns)	tplh (ns)	tphl (ns)	
NA2	2-Input Nand	In	Out	0.064	0.055	0.208	0.179	0
				0.099	0.083	0.325	0.273	1
				0.135	0.112	0.441	0.357	2
NO2	2-Input Nor	In	Out	0.085	0.054	0.277	0.175	0
				0.150	0.072	0.491	0.236	1
				0.216	0.091	0.705	0.296	2
IN1	1 x Inverter	In	Out	0.057	0.044	0.184	0.143	0
				0.092	0.062	0.298	0.203	1
				0.127	0.080	0.412	0.262	2
IN4	4 x Inverter	In	Out	0.041	0.034	0.134	0.110	0
				0.050	0.038	0.164	0.126	1
				0.059	0.043	0.194	0.142	2
DF	D Flip-Flop	CLK	Q	0.496	0.538	1.608	1.746	0
				0.531	0.557	1.723	1.809	1
				0.566	0.576	1.838	1.872	2
IBT	TTL Level Input Buffer	In	Out	0.261	0.377	0.848	1.223	0
				0.281	0.388	0.914	1.261	1
				0.301	0.400	0.979	1.298	2
PDV1AT + UO1	2mA Output Driver	In	Pad	1.598	1.065	5.185	3.453	10pF
				5.028	2.743	16.313	8.900	50pF
				9.314	4.841	30.223	15.709	100pF
PDV1AT + UO2	6mA Output Driver	In	Pad	0.875	0.771	2.838	2.502	10pF
				2.018	1.609	6.546	5.222	50pF
				3.446	2.656	11.181	8.621	100pF

*The values are based on simple delay model without interconnect load capacitance.

Best Case	Worst Case
Temperature = 0°C Ambient	Temperature = 70°C Ambient
Supply Voltage = 5.25V	Supply Voltage = 4.75V
Process = Best Case	Process = Worst Case

■ ELETRICAL CHARACTERISTICS DATA

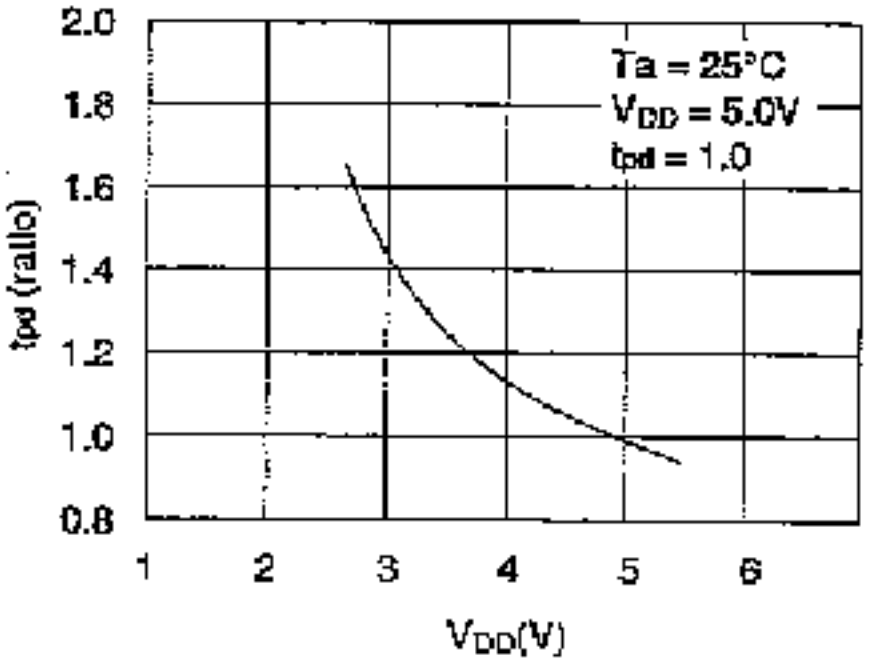
● 5.0 V Operation

– Output Current Characteristics (5V ±10%)

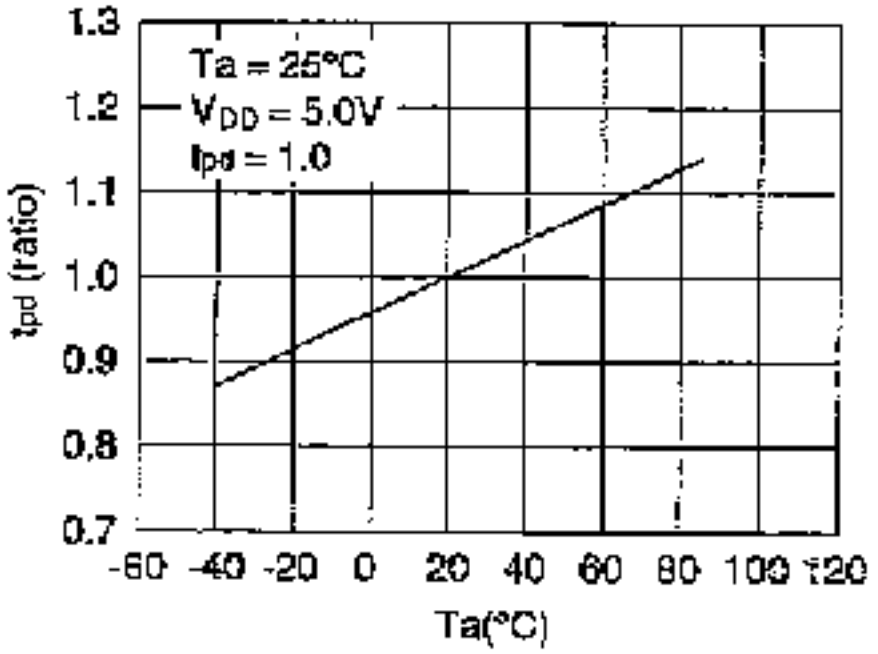
TYPE number	Output current	
	IOH (mA)	IOL (mA)
TYPE S	–0.1	0.1
TYPE 1	–1	2
TYPE 2	–3	6
TYPE 3	–6	12
TYPE 4	–12	24

The alphanumerics of the TYPE* (S, M, 1–4) indicate the output cell names (xx*x).

– Propagation Delay Characteristics



Propagation delay (tpd) vs. supply voltage (V_{DD})



Propagation delay (tpd) vs. ambient temperature (Ta)

TYPE number	Output current	
	IOH (mA)	IOL (mA)
TYPE S	–0.1	–0.1
TYPE 1	–1	2
TYPE 2	–2	4
TYPE 3	–4	8
TYPE 4	–8	12

The alphanumerics of the TYPE* (S, M, 1–4) indicate the output cell names (xx*x).

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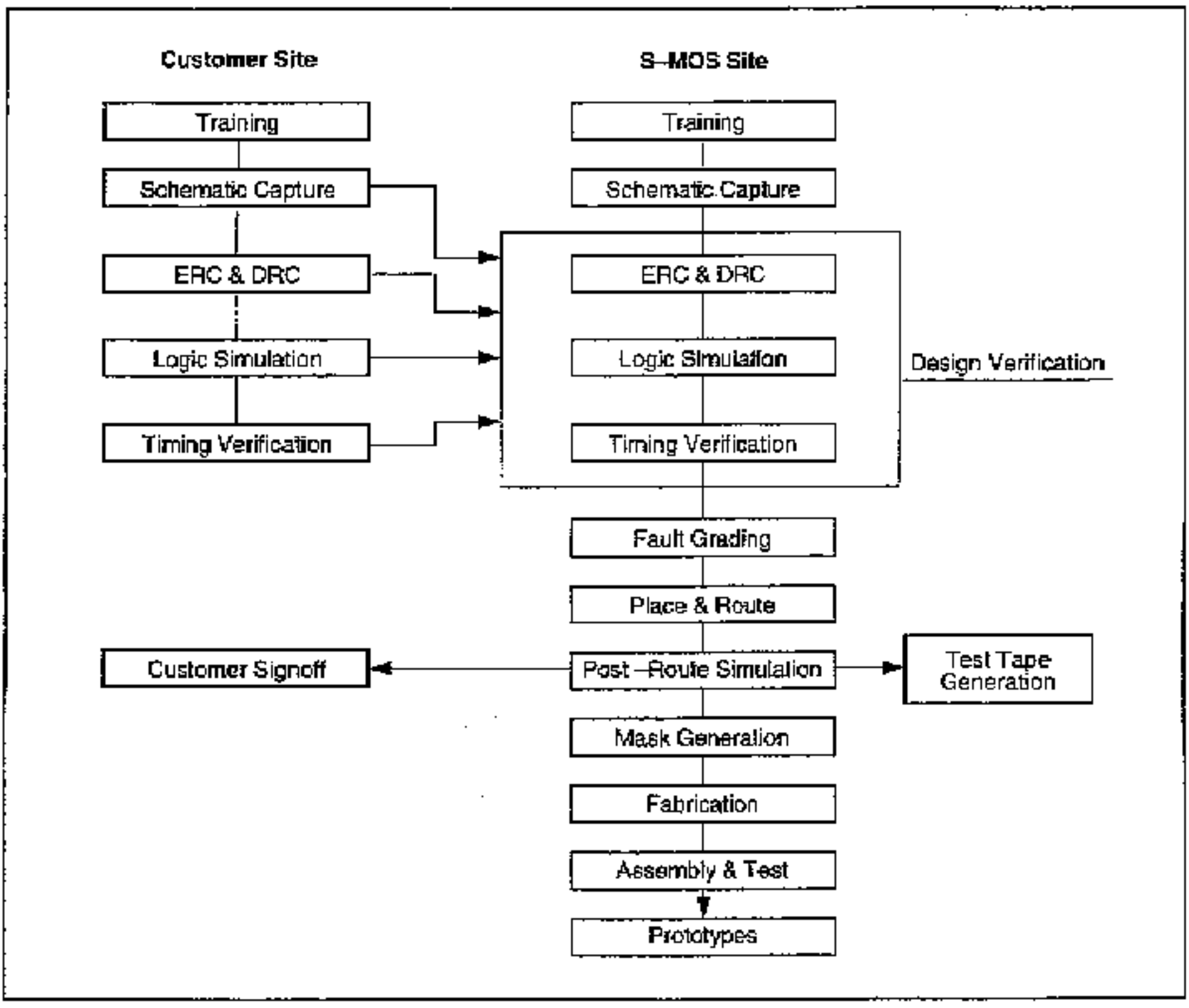
■ GATE ARRAY DEVELOPMENT FLOW



■ S-MOS CUSTOMER ENGINEERING

To help customers inplement their design of S-MOS ASIC's, we offer training at our design centers and at customer sites when required.

When a design is started, an S-MOS engineer is assigned to the project and will remain with the project through its completion. S-MOS engineers will work with the customer on design, software and other technical issues. When the design files are transferred to S-MOS, the assigned engineer will verify the design's integrity and prepare it for place and route. The S-MOS Customer Engineering Group provides all technical customer-support services including:

- •Pre-Sale Technical Support
- •Customer Training
- •Design Assistance
- •Workstation Support
- •Place Route
- •Software Documentation
- •Simulation Support
- •Turnkey Design
- •Design Verification

■ WORKSTATION SUPPORT

Schematic capture, electrical rule checking, design rule checking, simulation and timing verification are supported on:

Verilog, Auklet (PC, WS), ViewLogic, Synopsys, Exampler

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