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SCG305 SYNCHRONOUS CLOCK GENERATOR

FEATURES:

- Phase Locked Output Frequency Control.
- Intrinsically Low Jitter Crystal Oscillator.
- Two Pairs of Differential LVPECL Outputs.
- CMOS 8 KHz Reference Input.
- Fast 1 Second Acquisition Time.
- Input Duty Cycle Tolerant.
- 3.3 Volt Power Supply.
- Small Size: 0.75” x 1.20” Surface Mount Package.

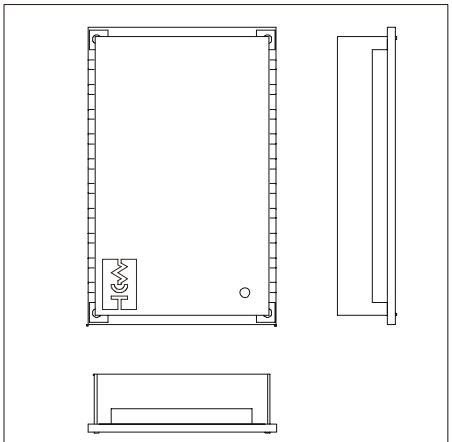


Figure 1: Package Outline

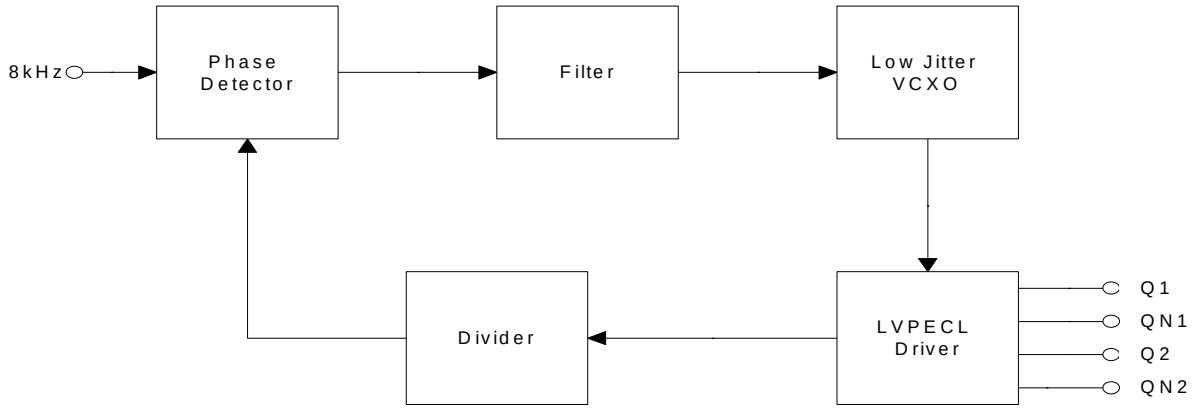
GENERAL DESCRIPTION:

The SCG305 is a digital phase locked loop generating 155.52 MHz LVPECL outputs from an intrinsically low jitter voltage controlled crystal oscillator. The SCG305 is phase locked to an external 8 KHz reference input.

The unit has a fast acquisition time of about 1 seconds and it is tolerant of different reference duty cycles. The SCG305 is ideal for applications using multiplication to obtain higher SONET frequencies.

The package dimensions are 0.75” x 1.20” x .40” on a 4 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand surface mount reflow processes.

BLOCK DIAGRAM:



ORDERING INFORMATION:

SCG305-155.52M

TABLE 1.0 ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V_{CC}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_I	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+150	ºC	1.0

TABLE 2.0 OPERATING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V_{CC}	Power Supply Voltage	+3.135	+3.30	+3.465	Volts	2.0
I_{CC}	Power Supply Current	-	-	220	mA	
T_{op}	Temperature Range	0º	-	70	ºC	
F_o	Output Frequency	-	155.52	-	MHz	
F_{ref}	Reference Frequency	-	8	-	KHz	
F_{cap}	Capture/pull-in range	-25	-	+25	PPM	
F_{bw}	Jitter Filter Bandwidth	-	3	-	Hz	3.0
T_{jtol}	Input Jitter Tolerance	-	-	6.25	us	
T_{aq}	Acquisition Time	-	2	-	secs	4.0
T_{rf}	Output Rise and Fall Time (20% to 80%)	100	225	350	ps	5.0
DC	Output Duty Cycle	45	50	55	%	
σ	Output Jitter	-	1	-	ps rms	6.0

TABLE 3.0 INPUT AND OUTPUT CHARACTERISTICS

CMOS INPUT CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MINIMUM**	**NOMINAL**	**MAXIMUM**	**UNITS**	**NOTE**
V_{IH}	High Level Input Voltage	2.0	-	5.6	V	
V_{IL}	Low Level Input Voltage	0.0	-	0.8	V	
T_{IR}	Input Reference Pulse Width	12.5	-	-	ns	
PECL OUTPUT CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MINIMUM**	**NOMINAL**	**MAXIMUM**	**UNITS**	**NOTE**
V_{OH}	High Level PECL Voltage	2.27	2.34	2.52	V	
V_{OL}	Low Level PECL Voltage	1.49	1.51	1.68	V	
C_L	Output Capacitance	-	-	10	pF	
T_{SKEW}	Differential Output Skew	-	TBD	-	ps	

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires External Regulation and Filter. (22 uF, 330 pF)

3.0 3db loop response relative to 0.01 Hz

4.0 From a 20 PPM step in reference frequency.

5.0 50 ohm load biased to 1.3 volts

6.0 Jitter based on OC48 bandwidth (12KHz to 20 MHz).

TABLE 4.0 PIN DESCRIPTIONS

PIN NUMBER	PIN NAME	PIN INFORMATION	NOTE
1	N/C	No Connection	
2	REF	CMOS Reference Input	
3	TDO	No Connection, Internal Factory Programming Input	7.0
4	V_{ee}	Ground	
5	QN1	LVPECL Complementary Output 1	
6	Q1	LVPECL Output 1	
7	V_{cc}	Supply Voltage relative to ground	
8	V_{ee}	Ground	
9	N/C	No Connection	
10	N/C	No Connection	
11	Q2	LVPECL Output 2	
12	QN2	LVPECL Complementary Output 2	
13	V_{ee}	Ground	
14	V_{ee}	Ground	
15	V_{cc}	Supply Voltage relative to ground	
16	TDI	No Connection, Internal Factory Programming Input	7.0
17	TCK	No Connection, Internal Factory Programming Input	7.0
18	TMS	No Connection, Internal Factory Programming Input	7.0
19	V_{ee}	Ground	
20	N/C	No Connection	

NOTES:

7.0 Do not connect pin.

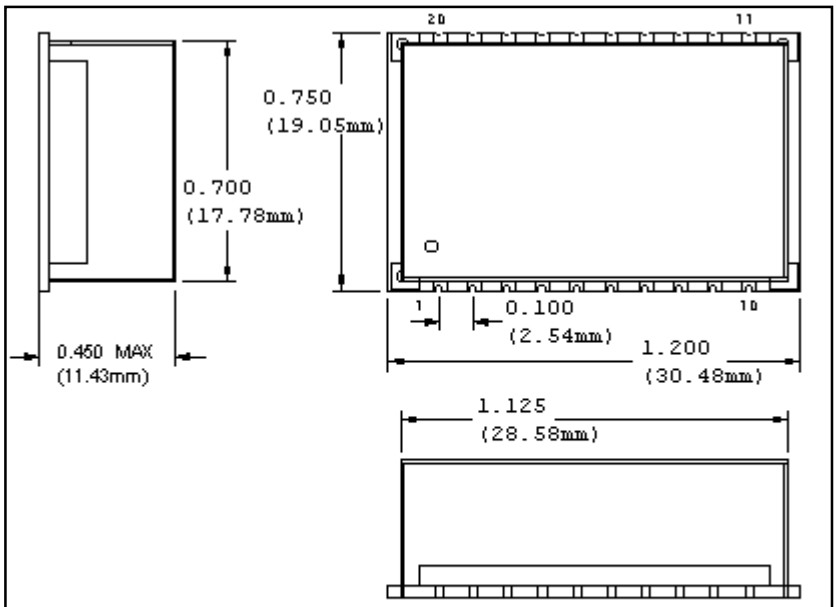


Figure 2 Package Dimensions

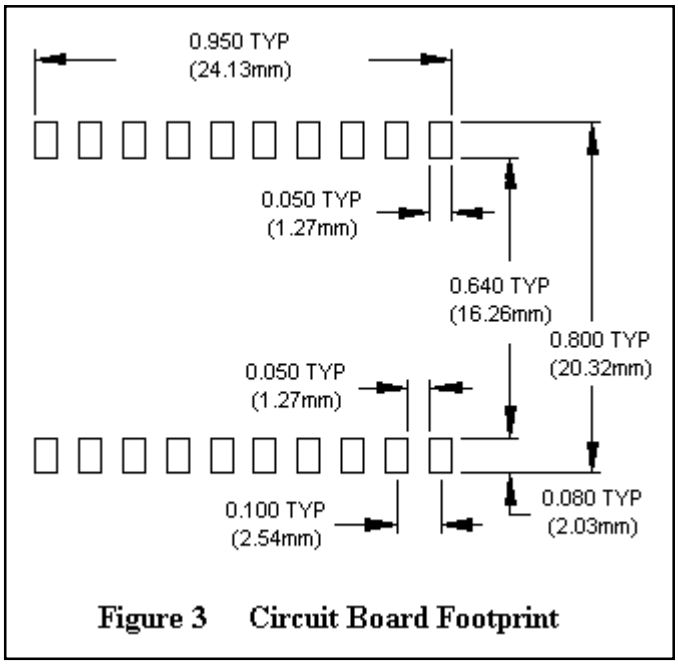
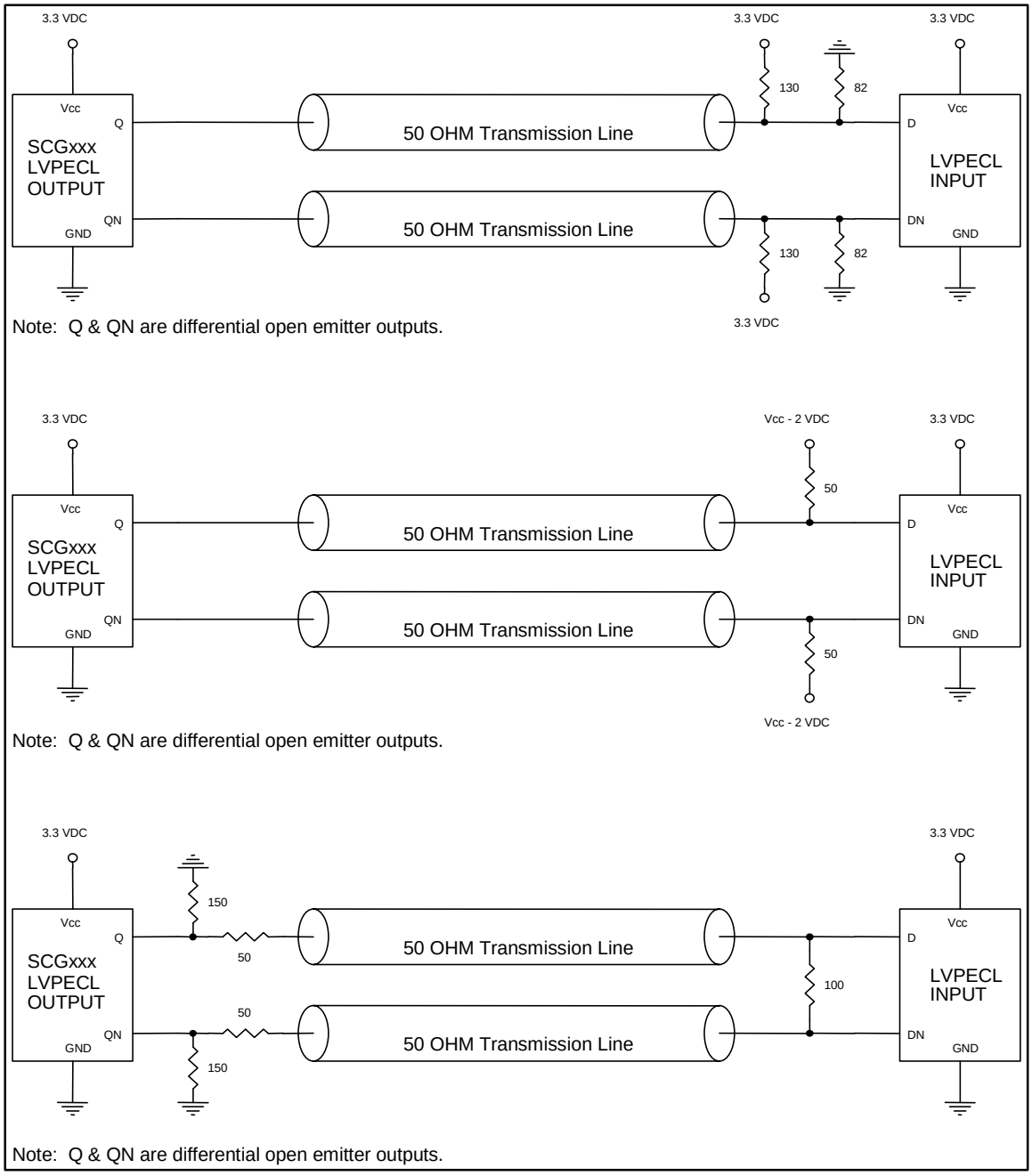


Figure 3 Circuit Board Footprint

FIGURE 4.0 RECOMMENDED PECL TERMINATION



NOTE:

8.0 If PECL outputs do not drive a long line (< 0.5 inch), a single 150Ω termination resistor to ground may be used for each pin.

TABLE A: DATA SHEET REVISION HISTORY

REVISION	REVISION DATE	NOTE
00	09/20/2000	Initial Release.
01	12/4/2000	Added PECL terminations