

**SCG304 SYNCHRONOUS CLOCK
GENERATOR****FEATURES:**

- Phase Locked Output Frequency Control.
- Intrinsically Low Jitter Crystal Oscillator.
- Two Pairs of Differential LVPECL Outputs.
- CMOS 19.44 MHz Reference Input.
- Fast 1 Second Acquisition Time.
- Input Duty Cycle Tolerant.
- 3.3 Volt Power Supply.
- Small Size: 0.75" x 1.20" Surface Mount Package.

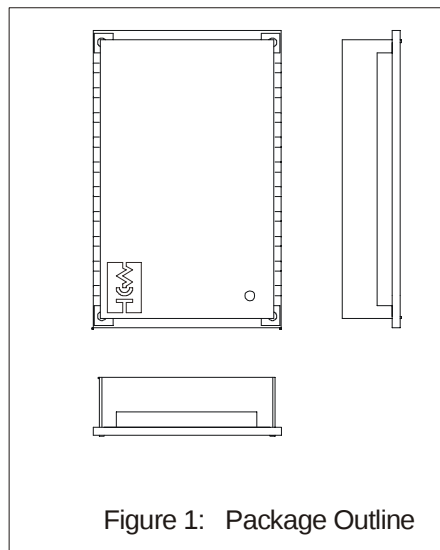


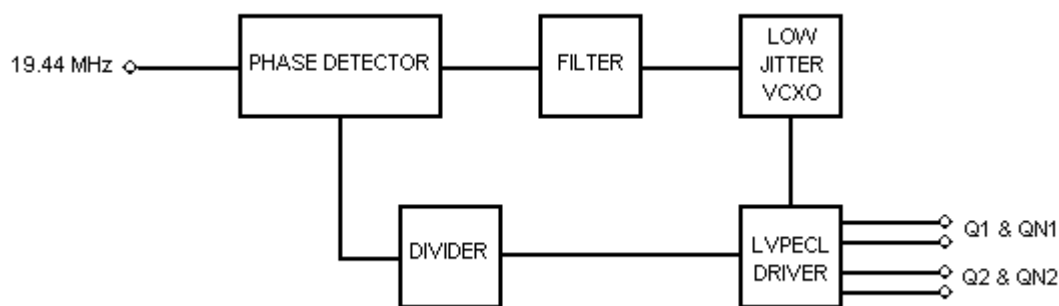
Figure 1: Package Outline

GENERAL DESCRIPTION:

The SCG304 is a digital phase locked loop generating 155.52 MHz LVPECL outputs from an intrinsically low jitter voltage controlled crystal oscillator. The SCG304 is phase locked to an external 19.44 MHz reference input.

The unit has a fast acquisition time of about 1 second and it is tolerant of different reference duty cycles. The SCG304 is ideal for applications using multiplication to obtain higher SONET frequencies.

The package dimensions are 0.75" x 1.20" x .40" on a 4 layer FR4 board with castellated pins. Parts are assembled using high temperature solder to withstand surface mount reflow processes.

BLOCK DIAGRAM:**ORDERING INFORMATION:**

SCG304-155.52M

Specifications are subject to change without notice

TABLE 1.0 ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V _{CC}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V _I	Input Voltage	-0.5	-	+5.5	Volts	1.0
T _s	Storage Temperature	-65.0	-	+150	°C	1.0

TABLE 2.0 OPERATING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V _{CC}	Power Supply Voltage	+3.135	+3.30	+3.465	Volts	2.0
I _{CC}	Power Supply Current	-	200	250	mA	2.1
T _{op}	Temperature Range	0	-	70	°C	
F _o	Output Frequency	-	155.52	-	MHz	
F _{ref}	Reference Frequency	-	19.44	-	MHz	
F _{cap}	Capture/pull-in range	-25	-	+25	PPM	
F _{bw}	Jitter Filter Bandwidth	-	3	-	Hz	3.0
T _{itol}	Input Jitter Tolerance	-	-	6.25	us	
T _{aq}	Acquisition Time	-	1	-	secs	4.0
T _{rf}	Output Rise and Fall Time (20% to 80%)	100	225	350	ps	5.0
DC	Output Duty Cycle	45	50	55	%	5.0
σ	Output Jitter	-	-	1	ps rms	6.0

TABLE 3.0 INPUT AND OUTPUT CHARACTERISTICS

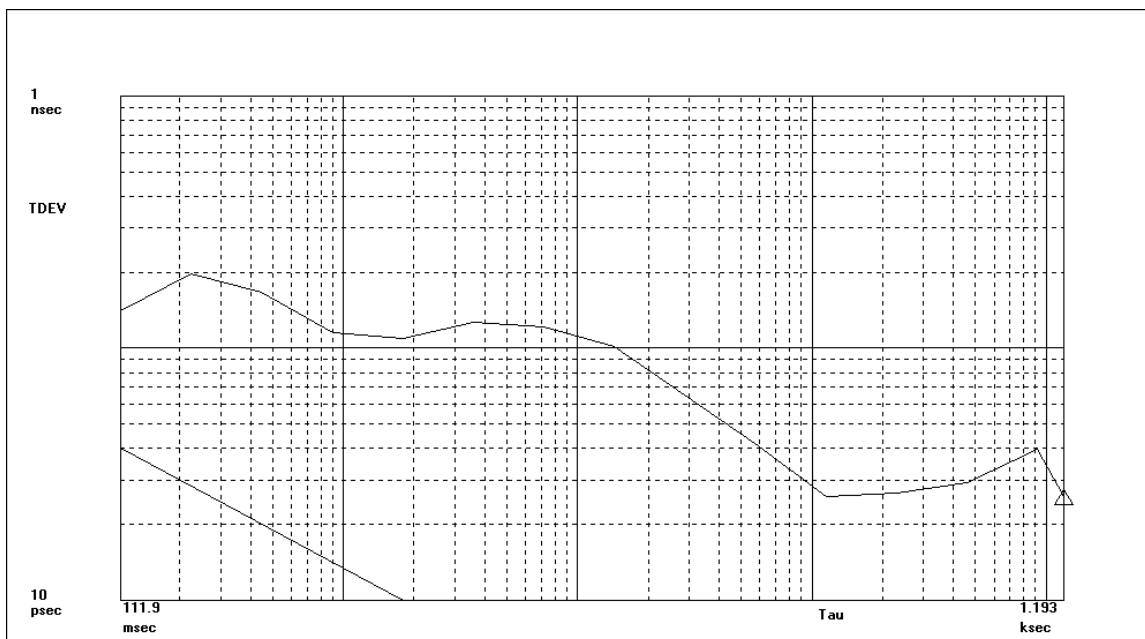
CMOS INPUT CHARACTERISTICS						
SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V _{IH}	Input High Voltage	2.0	-	5.6	V	
V _{IL}	Input Low Voltage	0.0	-	0.8	V	
T _{IR}	Input Reference Pulse Width	12.5	-	-	ns	
PECL OUTPUT CHARACTERISTICS						
SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V _{OH}	Output High Voltage	2.27	2.34	2.52	V	5.0
V _{OL}	Output Low Voltage	1.49	1.51	1.68	V	5.0
C _L	Output Capacitance	-	-	10	pF	
T _{SKEW}	Differential Output Skew	-	50	-	ps	5.0

NOTE:

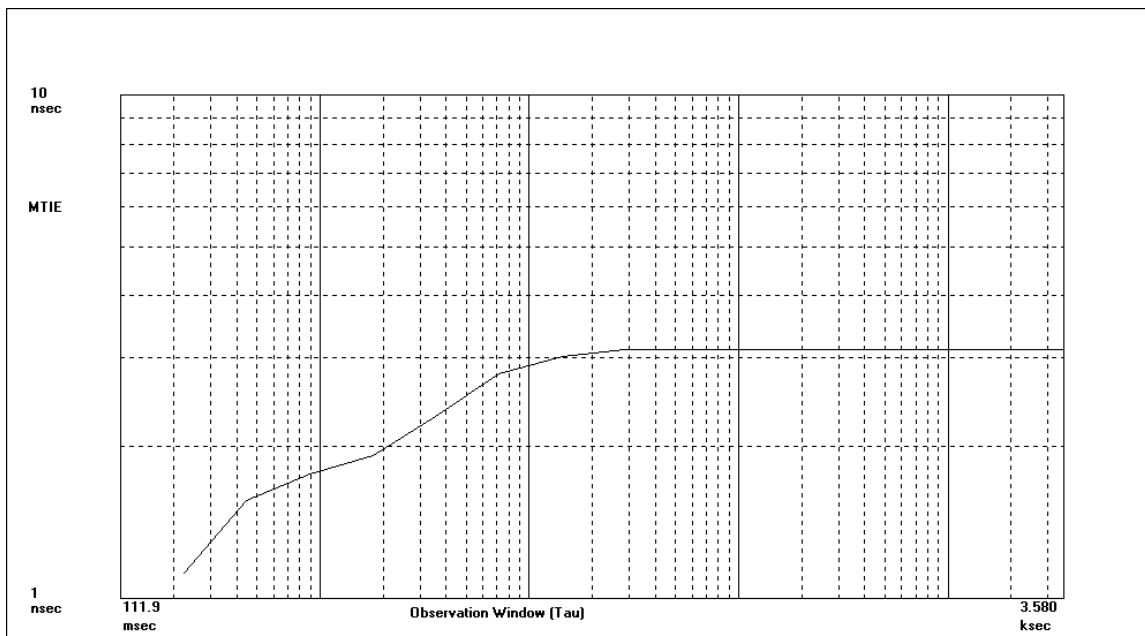
- 1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.
- 2.0 Requires External Regulation and supply decoupling. (22 uF, 330 pF)
- 2.1 PECL outputs terminated into 500Ω, see figure 4.0a.
- 3.0 3db loop response.
- 4.0 From a 20 PPM step in reference frequency.
- 5.0 With PECL Termination as defined by figure 4.0a (Z_o = 50Ω).
- 6.0 Jitter based on SONET OC-48 bandwidth (12KHz to 20 MHz).

Specifications are subject to change without notice

GRAPH 1: Typical TDEV Performance

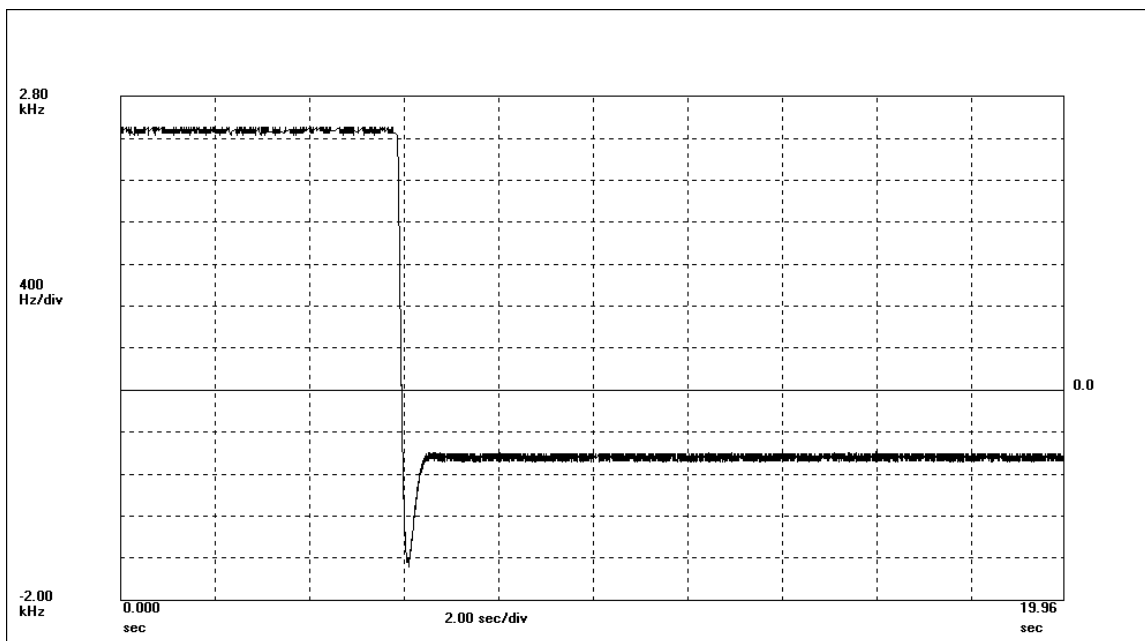


GRAPH 2: Typical MTIE Performance



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GRAPH 3: Typical Acquisition Time



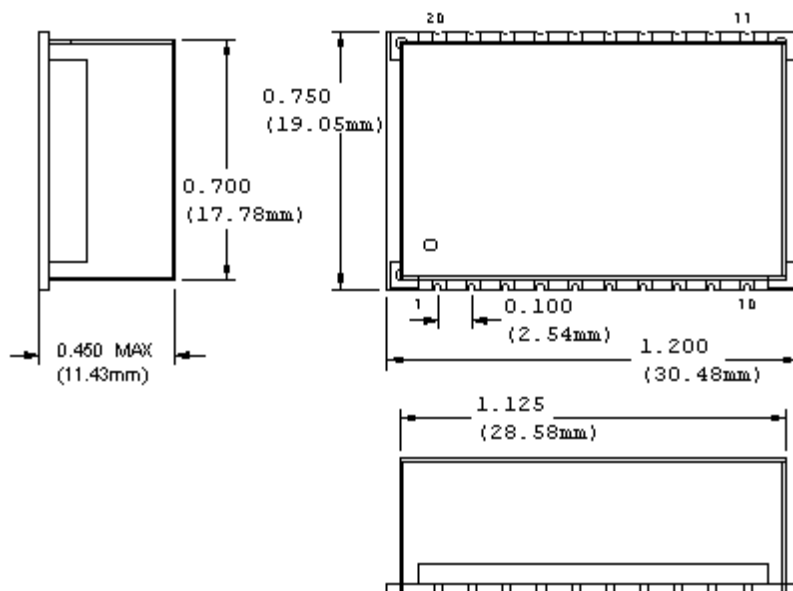
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TABLE 4.0 PIN DESCRIPTIONS

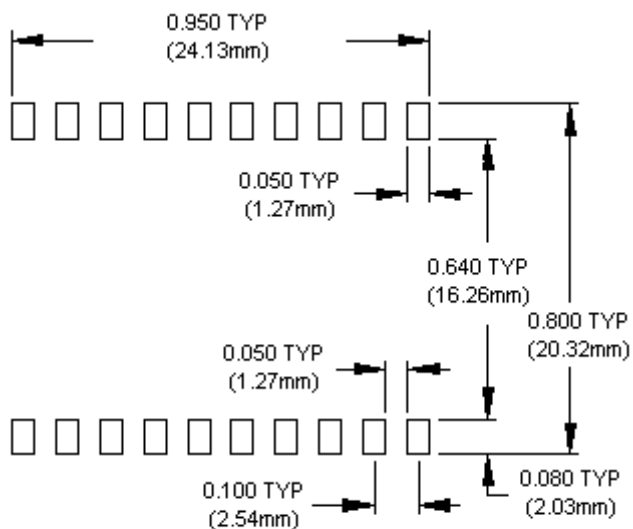
PIN #	PIN NAME	PIN INFORMATION	NOTE
1	N/C	No Connection	
2	REF	CMOS Reference Input	
3	TDO	No Connection, Internal Factory Programming Input	7.0
4	V _{ee}	Ground	
5	QN1	LVPECL Complementary Output 1	
6	Q1	LVPECL Output 1	
7	V _{cc}	Supply Voltage relative to ground	
8	V _{ee}	Ground	
9	N/C	No Connection	
10	N/C	No Connection	
11	Q2	LVPECL Output 2	
12	QN2	LVPECL Complementary Output 2	
13	V _{ee}	Ground	
14	V _{ee}	Ground	
15	V _{cc}	Supply Voltage relative to ground	
16	TDI	No Connection, Internal Factory Programming Input	7.0
17	TCK	No Connection, Internal Factory Programming Input	7.0
18	TMS	No Connection, Internal Factory Programming Input	7.0
19	V _{ee}	Ground	
20	N/C	No Connection	

NOTE:

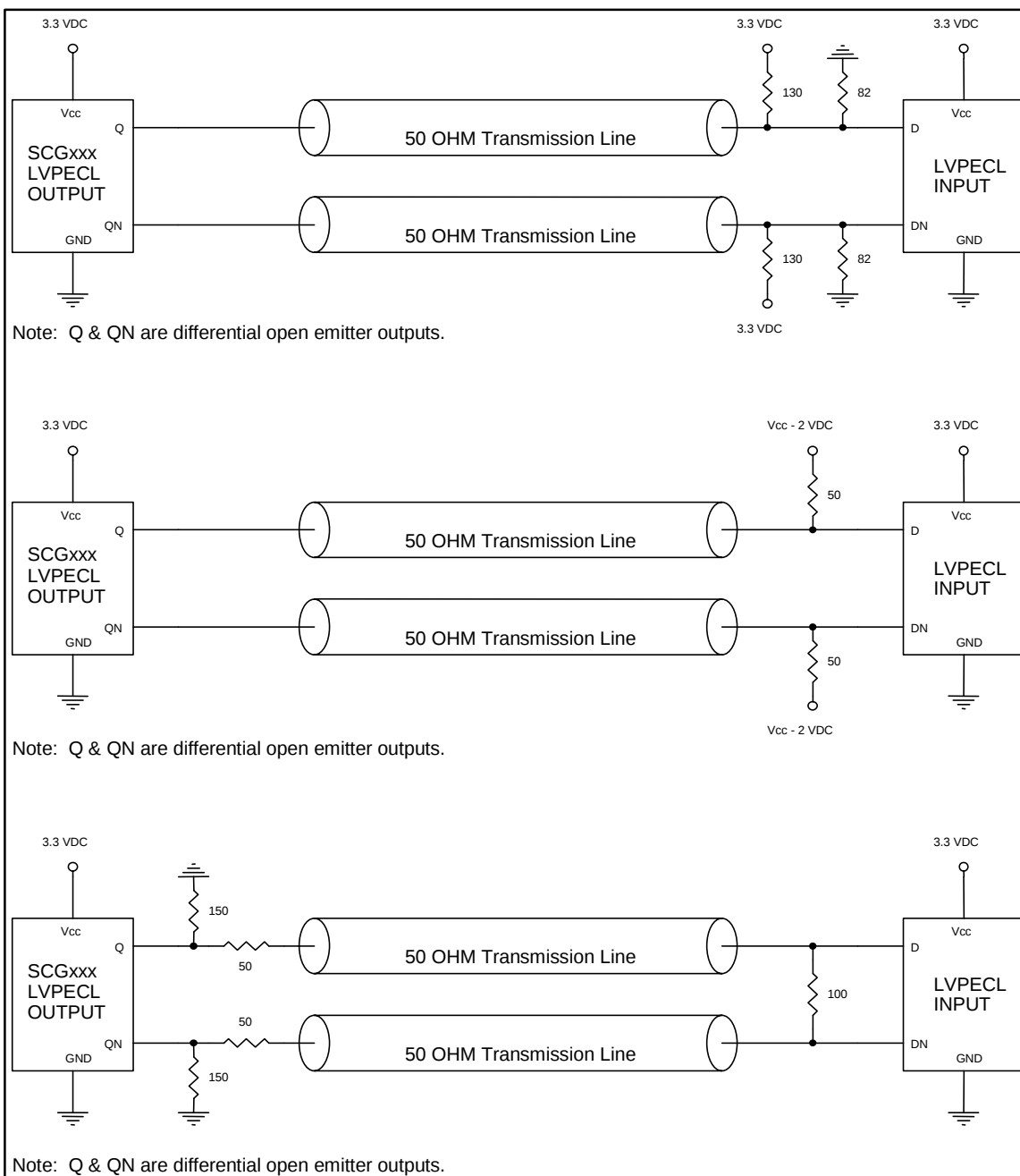
7.0 Do not connect pin.

FIGURE 2.0 PACKAGE DIMENSIONS


Specifications are subject to change without notice

FIGURE 3.0 RECOMMENDED CIRCUIT BOARD FOOTPRINT

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FIGURE 4.0 RECOMMENDED PECL TERMINATION

NOTE:

8.0 If PECL outputs do not drive a long line (< 0.5 inch), a single 150Ω termination resistor to ground may be used for each pin.

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SCG304 SYNCHRONOUS CLOCK GENERATOR

TABLE A: DATA SHEET REVISION HISTORY

REVISION	REVISION DATE	NOTE
00	09/20/00	Initial Release
01	11/27/00	Changed Fig. 4.0

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DATA SHEET #: SG014
DATE: 11/27/2000

REVISION #: 01
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FILENAME: SCG304.DOC
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