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SCG4600 SYNCHRONOUS CLOCK GENERATOR

FEATURES:

- Phase Locked Output Frequency Control.
- Intrinsically Low Jitter Crystal Oscillator.
- CML Outputs.
- Dual 8 kHz References.
- LOR & LOL Alarm.
- Force Free Run Function.
- Automatic Free Run Operation on Loss of Both References A & B.
- Input Duty Cycle Tolerant.
- 3.3VDC Power Supply.
- Small Size: 1 Square Inch.

GENERAL DESCRIPTION:

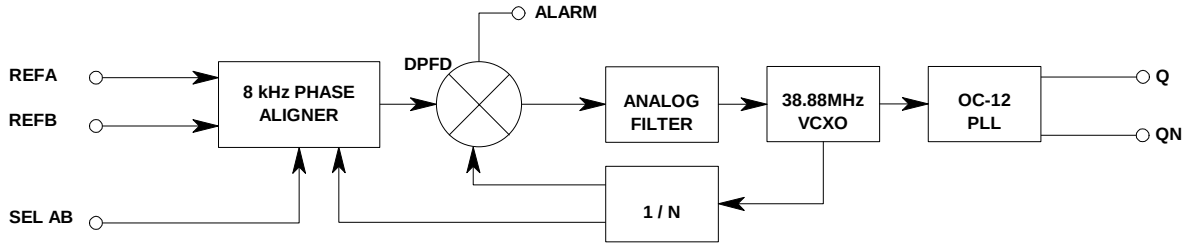
The SCG4600 is a digital phase locked loop generating CML outputs from an intrinsically low jitter voltage controlled crystal oscillator.

The SCG4600 can lock to one of two external 8 kHz references, which is selectable using the SEL_{AB} input select pin. The unit has an acquisition time of about 1.5 seconds and it is tolerant of different reference duty cycles.

The SCG4600 includes an alarm output that indicates deviations from normal operation. If a Loss-of-Reference (LOR) or Loss-of-Lock (LOL) is detected the alarm with indicate the need for a reference rearrangement. If both references A and B are absent the module will enter Free Run operation. The FR_{status} pin will indicate that the module is in Free Run operation. Frequency stability during Free Run operation is guaranteed to ±20 PPM. Additionally the Free Run mode may be entered manually.

The package dimensions are 1” x 1” x .45” on a 4 layer FR4 board with J-Leads. Parts are assembled using high temperature solder to withstand 180°C surface mount reflow processes.

BLOCK DIAGRAM



ORDERING INFORMATION:

SCG4600-622.08M

TABLE 1.0 ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V_{cc}	Power Supply Voltage	-0.5	-	+4.0	Volts	1.0
V_i	Input Voltage	-0.5	-	+5.5	Volts	1.0
T_s	Storage Temperature	-65.0	-	+150	°C	1.0

TABLE 2.0 OPERATING SPECIFICATIONS

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTE
V_{cc}	Power Supply Voltage	3.135	3.300	3.465	Volts	2.0
I_{cc}	Power Supply Current	-	200	-	mA	
T_o	Temperature Range	0	-	70	°C	
F_o	Output Frequency	-	622.08	-	MHz	
F_{fr}	Free Run Frequency	-20	-	20	PPM	
F_{refa}	Reference Frequency A	-	8	-	kHz	
F_{refb}	Reference Frequency B	-	8	-	kHz	
F_{cap}	Capture/pull-in range	-25	-	25	PPM	
F_{bw}	Jitter Filter Bandwidth	-	-	3	Hz	3.0
T_{jtol}	Input Jitter Tolerance	-	-	6.25	µs	
T_{aq}	Acquisition Time	-	1.5	-	s	4.0
T_{rf}	Output Rise and Fall Time	-	100	-	ps	5.0
DC	Output Duty Cycle (20% 80%)	TBD	-	TBD	%	
σ	Jitter Generation	-	2	-	psRMS	6.0
$MTIE_{sr}$	MTIE at Synchronization Rearrangement	GR-253-CORE.1999 R5-136				7.0, 7.1

NOTES:

1.0 Operation of the device at these or any other condition beyond those listed under Operating Specifications is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

2.0 Requires external regulation and supply decoupling. (2.2 uF, 330 pF)

3.0 3db loop response.

4.0 From a 20 PPM step in reference frequency.

5.0 CML outputs ac coupled into 50-ohm load to V_{cc}.

6.0 Jitter based on SONET OC-12 bandwidth. (12 kHz to 5 MHz)

7.0 Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.

7.1 If the selected reference is removed system response to the ALARM must be less than 10µs.

TABLE 3.0 INPUT AND OUTPUT CHARACTERISTICS

CMOS INPUT AND OUTPUT CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MINIMUM**	**NOMINAL**	**MAXIMUM**	**UNITS**	**NOTE**
V_{ih}	High Level Input Voltage	2.0	-	5.6	V	
V_{il}	Low Level Input Voltage	0.0	-	0.8	V	
T_{io}	I/O to Output Valid	-	-	10	ns	
C_l	Output Capacitance	-	-	10	pF	
V_{oh}	High Level Output Voltage	2.4	-	-	V	
V_{ol}	Low Level Output Voltage		-	0.4	V	
T_{ir}	Input Reference Pulse Width	12.5	-	-	ns	
CML OUTPUT CHARACTERISTICS						
SYMBOL	**PARAMETER**	**MINIMUM**	**NOMINAL**	**MAXIMUM**	**UNITS**	**NOTE**
V_{od}	Differential Output Voltage	-	800	-	mV	5.0
V_{ocm}	Output Common Mode Voltage	-	Vcc – 0.75	-	V	5.0

TABLE 4.0 INPUT SELECTION / OUTPUT RESPONSE

INPUTS						OUTPUTS				NOTE
RESET	**ENABLE**	**SEL_{AB}**	**REF_A**	**REF_B**	**FR**	**FR_{status}**	**ALARM**	**Q**	**QN**	
1	0	X	X	X	X	1	1	X	X	FR
X	1	X	X	X	X	HZ	HZ	1	1	
0	0	X	X	X	1	1	1	X	X	FR
0	0	0	A	A	0	0	0	X	X	RA
0	0	1	A	A	0	0	0	X	X	RB
0	0	0	NA	A	0	0	1	X	X	U
0	0	1	NA	A	0	0	0	X	X	RB
0	0	1	A	NA	0	0	1	X	X	U
0	0	0	A	NA	0	0	0	X	X	RA
0	0	X	NA	NA	0	1	1	X	X	FR

NOTES:

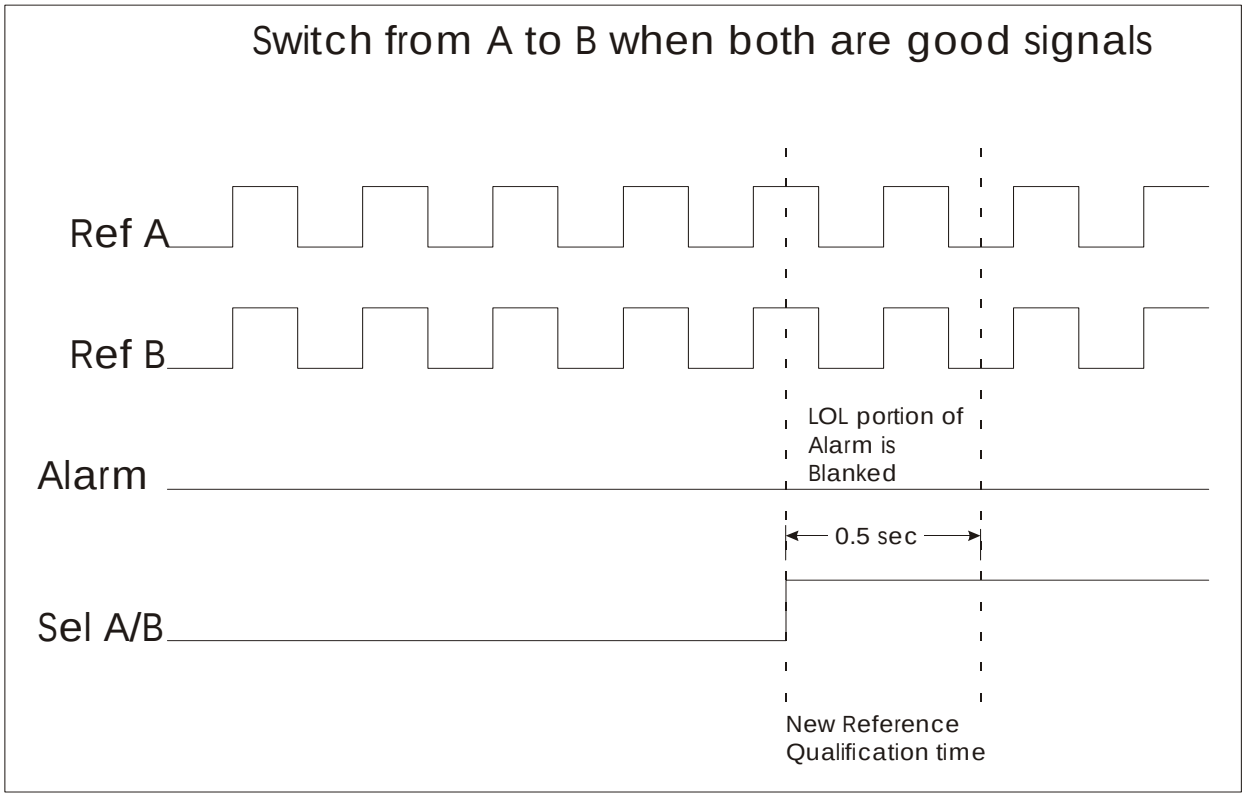
A Active
FR Free Run Mode
HZ High Impedance
NA Not Active
RA Locked to Reference A
RB Locked to Reference B
U Unstable (due to conditions shown, switch to active reference or Free Run)
X Don't care

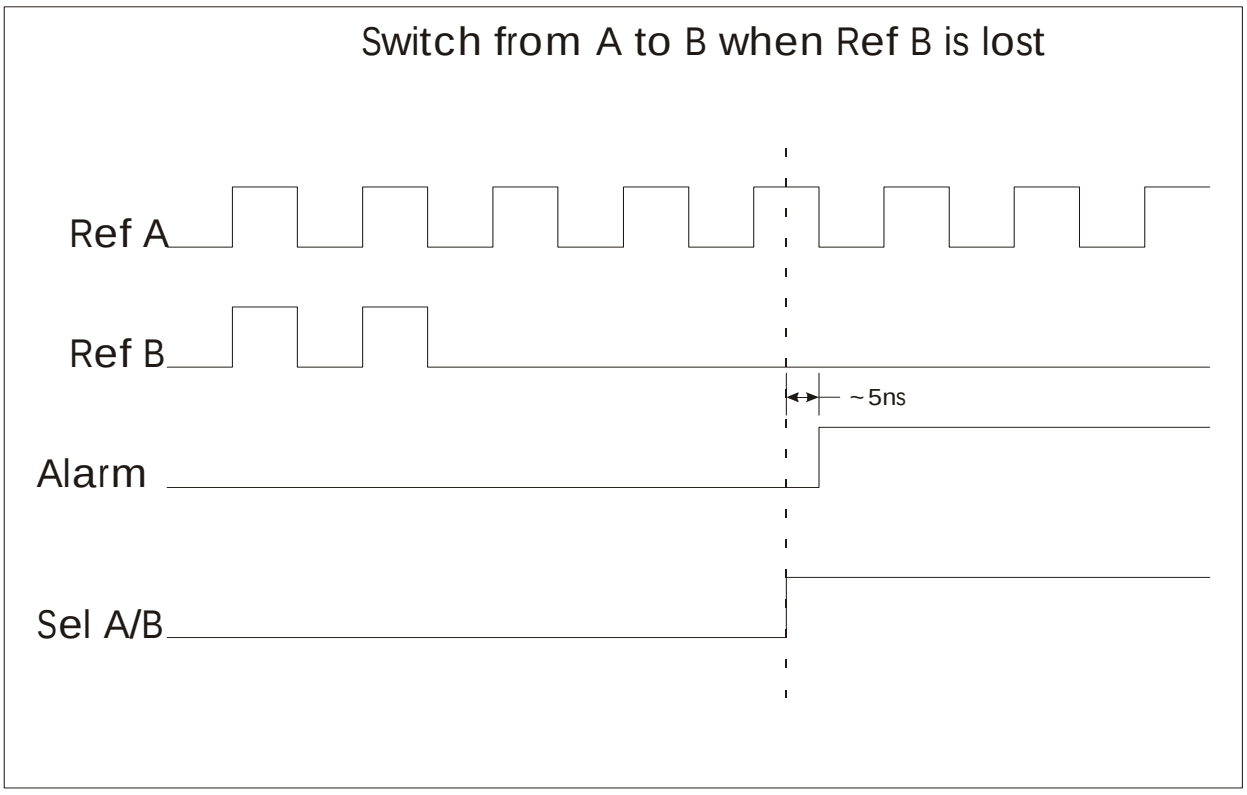
TABLE 5.0 PIN DESCRIPTIONS

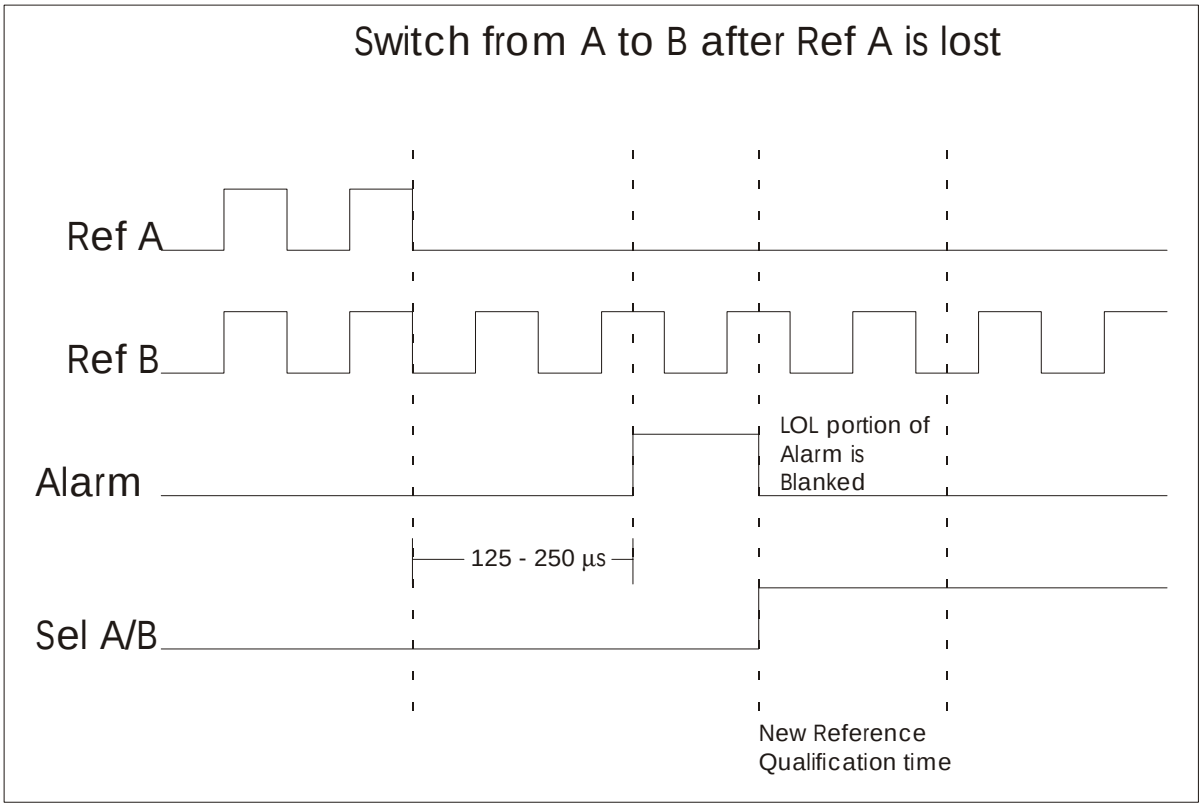
PIN NUMBER	PIN NAME	PIN INFORMATION	NOTE
1	ENABLE	CML Enable / CMOS Tri-State. (Enable=0, Disable=1)	9.0
2	TCK	No Connection, Internal Factory Programming Input.	8.0
3	TDO	No Connection, Internal Factory Programming Input.	8.0
4	REF_A	CMOS Reference Frequency Input.	
5	SEL_{AB}	Input Reference Select Pin. (REFA=0, REFB=1)	9.0
6	RESET	RESET. (RESET=1)	9.0
7	REF_B	CMOS Reference Frequency Input.	
8	GND	Ground.	
9	FR_{status}	Free Run Status. (FR = 1)	
10	V_{cc}	Supply Voltage relative to ground.	
11	N/C	No Connection.	8.0
12	ALARM	Loss of Reference / Lock alarm. (Alarm=1)	
13	FR	Force Free Run. (Phase Lock=0, Free Run=1)	9.0
14	TDI	No Connection, Internal Factory Programming Input.	8.0
15	TMS	No Connection, Internal Factory Programming Input.	8.0
16	QN	Negative Differential CML Output.	10.0
17	GND	Ground.	
18	Q	Positive Differential CML Output.	10.0

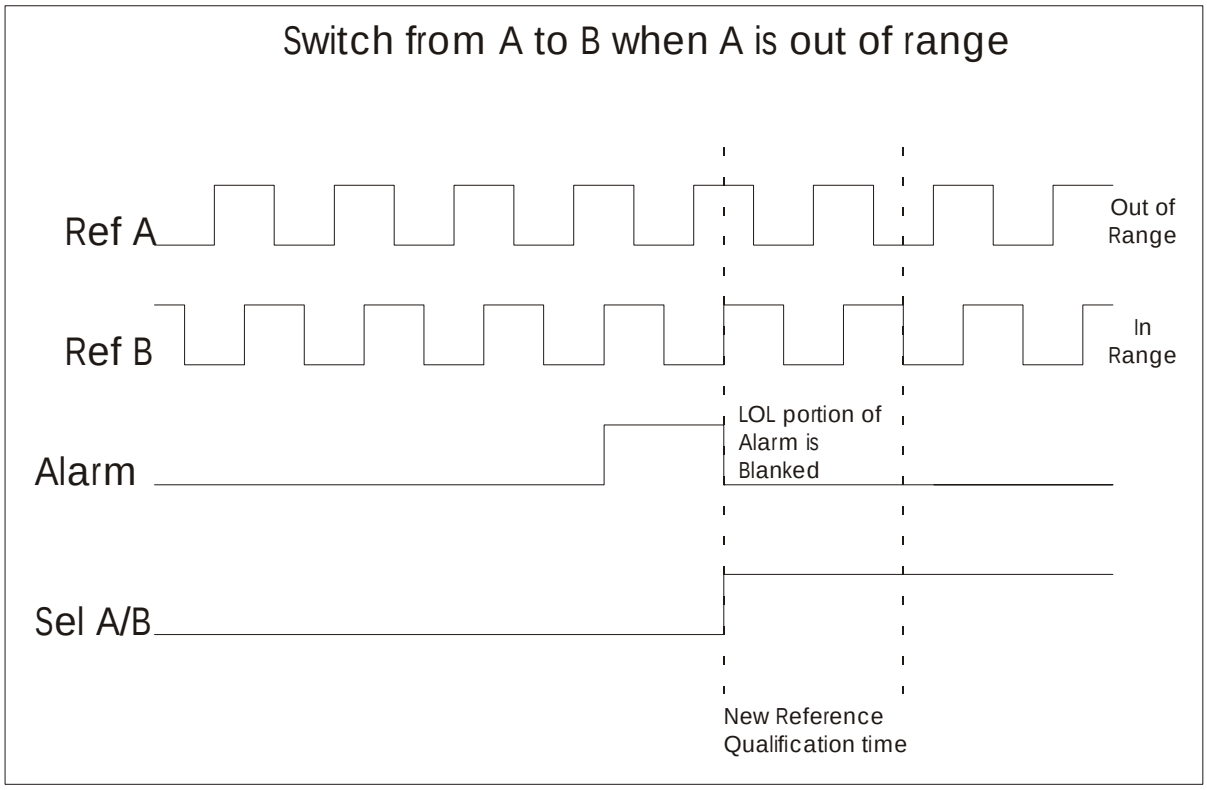
NOTES:

8.0 Do not connect pin.
9.0 Input pulled to ground.
10.0 CML outputs are internally AC coupled.









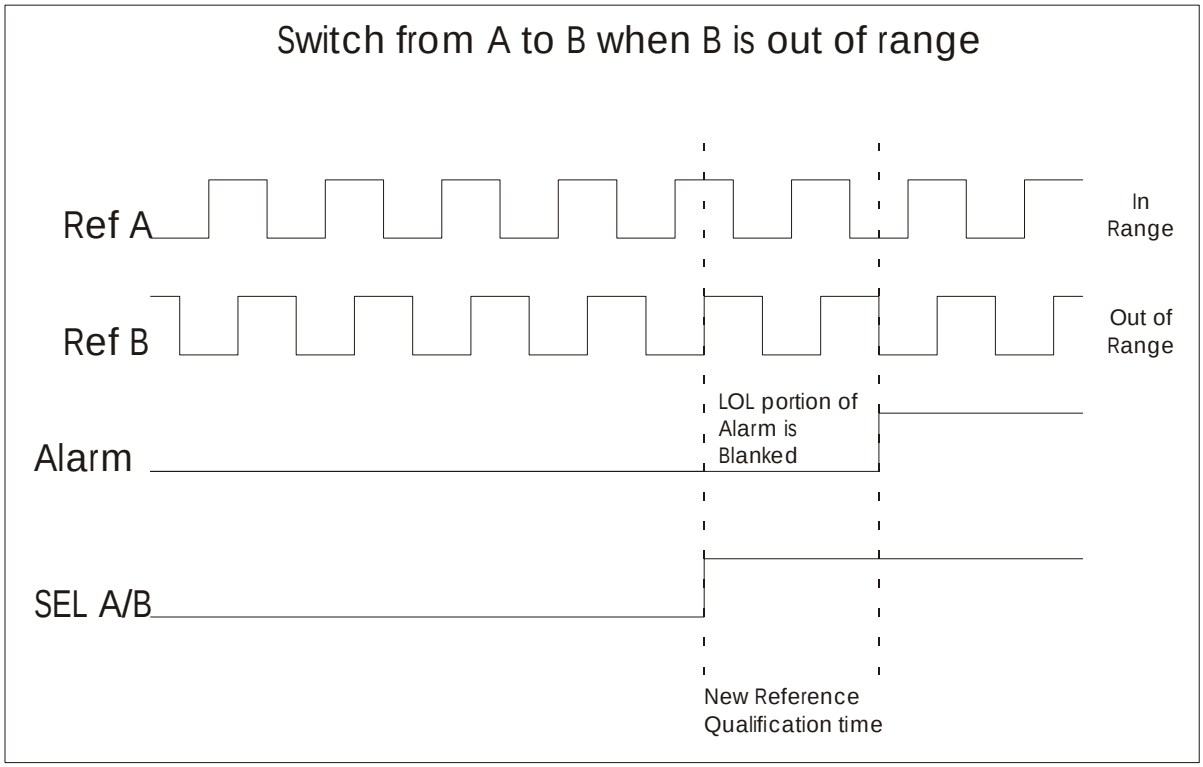


Figure 3 Circuit Board Footprint Recommendations

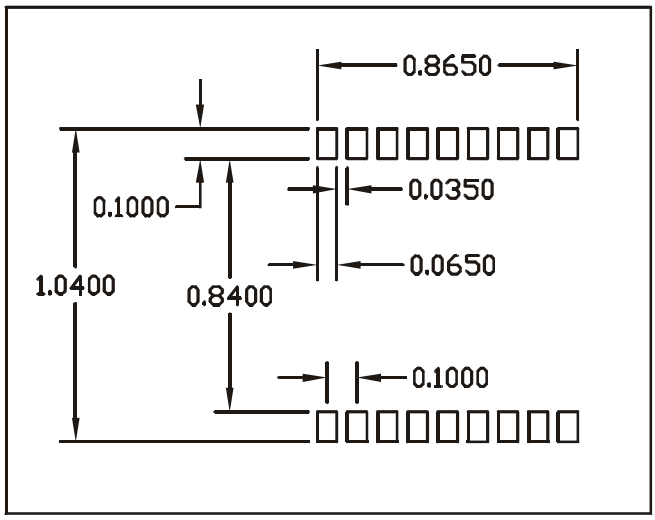


Figure 4.0 Package Dimensions

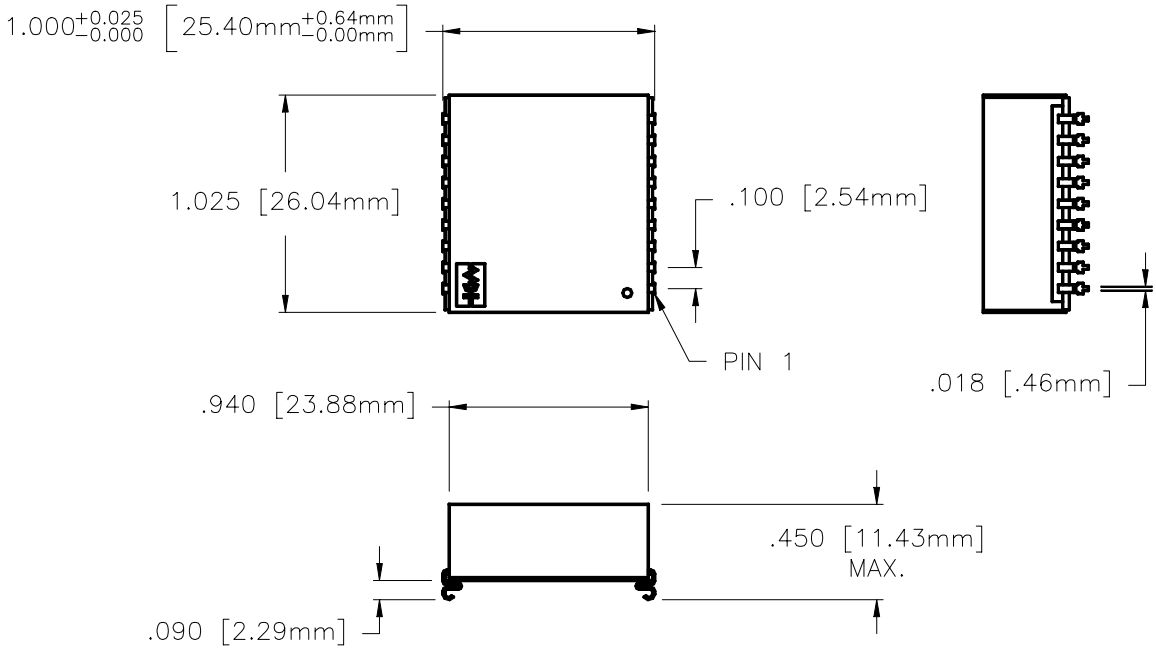


TABLE A: DATA SHEET REVISION HISTORY

REVISION	REVISION DATE	NOTE
P00	01/17/2001	Initial Preliminary Release.