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SCG2500 SYNCHRONOUS CLOCK GENERATOR

FEATURES:

- Phase Locked Ouput Frequency Control.
- Intrinsically Low Jitter Crystal Oscillator.
- Two Selectable References @ 8 kHz.
- Alarm Ouput.
- Tri-Statable Oscillator and Alarm Outputs
- Force Freerun Function.
- Automatic Freerun Operation on LOR Alarm Condition.
- Fast .35 Second Aquisition Time.
- Input Duty Cycle Tolerant.
- 3.3 Volt Power Supply.
- Small Size: .6 Square Inches.
- Surface Mount, DIL Package.

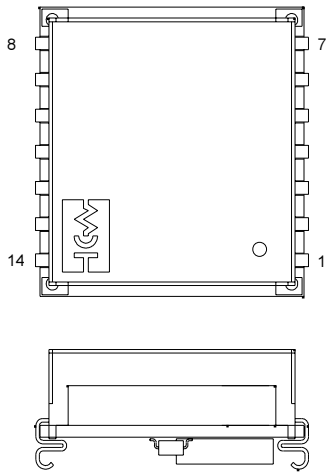


Figure 1: Package Outline

GENERAL DESCRIPTIONS:

The SCG2500 is a digital phase lock loop generating CMOS outputs from an intrinsically low jitter voltage controlled crystal oscillator.

The SCG2500 can lock to one of two possible input reference frequencies at 8 kHz which is selectable using one input select pin. The unit has a fast acquisition time of about .35 seconds and it is tolerant of different reference duty cycles.

Further features include an alarm output to indicate Loss of Reference, LOR, or Loss of Lock, LOL. If only one of the references is lost, the unit will disable its phase detector and will signal an alarm, but will not switch reference automatically. If both references are lost, the SCG2500 will enter a Free Run state which will guarantee a 20 ppm accurate output. Additionally, the Free Run mode may be entered manually by applying a high signal to the Free Run pin. If the unit is in Free Run mode, the Free Run status pin will be high.

The outputs may be put into the tri-state high impedance condition for external testing purposes by applying a high signal to the Reset/Tri-State pin.

The filtered 8 kHz is derived from the oscillator output, but has no phase offset relationship between it and each reference.

The package dimensions are .775" x .8" x .35" on a six layer FR4 board with surface mount pins. Parts are assembled using high temperature solder to withstand surface mount reflow process.

PIN	CONNECTION
1	FILTERED 8kHz OUTPUT
2	TCK
3	TMS
4	GROUND
5	FREE RUN / TDI (1=free run)
6	ALARM OUTPUT (1= alarm)
7	REF B
8	REF A
9	OSCILLATOR OUTPUT
10	FREE RUN STATUS PIN (FR=1)
11	Vcc
12	TDO
13	RESET/ TRI STATE
14	INPUT FREQ. SELECT AB (A=0, B=1)

Table 1: Pin Connections

TABLE 2.0 ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTES
Vcc	Power supply voltage	-0.5		+4.0	Volts	
V_i	Input voltage	-0.5		+5.5	Volts	
T_S	Storage temperature	-65.0		+150.0	deg. C	

TABLE 3.0 SPECIFICATIONS

PARAMETER		NOTES
Voltage	3.3 V ±5%	1.0
Current	136 mA @ 3.46 V	
Oscillator Output Frequencies	1.544, 2.048, 19.44, 20.48, 44.736, 51.84 and 77.76 MHz	
Temperature Range	0 to 70 deg. C.	
Input Frequency Ref 1 and Ref 2	8 kHz	2.0
Input Jitter Tolerance	6.25 us, 10 Hz (0.05 UI @ 8000 Hz)	
Jitter Bandw idth	4 Hz	
Acquisition Time	Approx. 0.35 seconds	3.0
Capture/pull-in range	±25 ppm Minimum	
Output Duty Cycle	40/60 % Min/Max @ 50% Level	
Output Rise And Fall Time	3 nS @ 20% to 80% output level	
Output Load	30 pF	
Alarm	LOR/LOL status signal output	
Free Run Accuracy	±20 ppm	
Package	Fr4 SM 0.765" x 8" x 0.350"	
MTIE @ Synchronization Rearrangement	GR-253-CORE.1999 R5-136	4.0, 4.1

TABLE 4.0 INPUT AND OUTPUT CHARACTERISTICS

SYMBOL	PARAMETER	MINIMUM	NOMINAL	MAXIMUM	UNITS	NOTES
V_{IH}	High level input voltage	2.0		5.5	V	
V_{IL}	Low level input voltage	0		0.8	V	
T_{IO}	I/O to output valid			10	nS	
C_O	Output capacitance			10	pF	
V_{HO}	High level output voltage Ioh = -4mA	2.40				Vcc Minimum
V_{IO}	Low level output voltage Io1 = 8mA			0.4		Vcc Maximum
T_{IR}	Input reference signal pulse width	30			nS	

NOTES:

NOTE 1.0: Requires external regulation.
NOTE 2.0: Externally selectable via Input Select AB.
NOTE 3.0: From a 20 ppm offset in reference frequency.
NOTE 4.0: Entry into Free Run doesn't meet requirement for initial 2.33 seconds of self-timing.
NOTE 4.1: If the selected reference is removed system response to the ALARM must be less than 10µs.

TABLE 5.0 OUTPUT JITTER SPECIFICATIONS

	Jitter BW 10 Hz -1 MHz		SONET Jitter BW 12 kHz - 20 MHz		
FREQUENCY (MHZ)	pS (rms)	mUI	pS (rms)	mUI	Notes
1.544	TBD	TBD	TBD	TBD	
2.048	TBD	TBD	TBD	TBD	
19.44	TBD	TBD	TBD	TBD	
20.48	TBD	TBD	TBD	TBD	
34.368	TBD	TBD	TBD	TBD	
44.736	TBD	TBD	TBD	TBD	
51.84	TBD	TBD	TBD	TBD	
77.76	TBD	TBD	TBD	TBD	

TABLE 6.0 INPUT SELECTION / OUTPUT RESPONSE

INPUTS					OUTPUTS				NOTE
RESET/ TRI-STATE	SEL_{AB}	REF_A	REF_B	FR	FR_{status}	ALARM	Oscillator Output	8 kHz Output	
1	X	X	X	X	TS	TS	TS	TS	
0	X	X	X	1	1	1	FR	FR	
0	0	A	A	0	0	0	LRA	LRAD	
0	1	A	A	0	0	0	LRB	LRBD	
0	0	NA	A	0	0	1	U	U	5.0
0	1	NA	A	0	0	0	LRB	LRBD	
0	1	A	NA	0	0	1	U	U	5.0
0	0	A	NA	0	0	0	LRA	LRAD	
0	X	NA	NA	0	1	1	FR	FR	

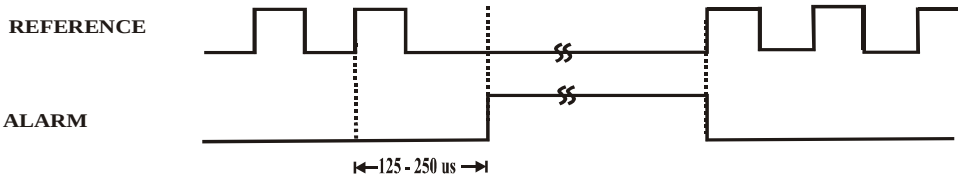
TS = Tri-State
FR = Free Run
LRA = Locked to Ref A
LRB = Locked to Ref B
U = Unstable
LRAD = Locked to Ref A and divided down
LRAB = Locked to Ref B and divided down
X = Don't cart

NOTES:

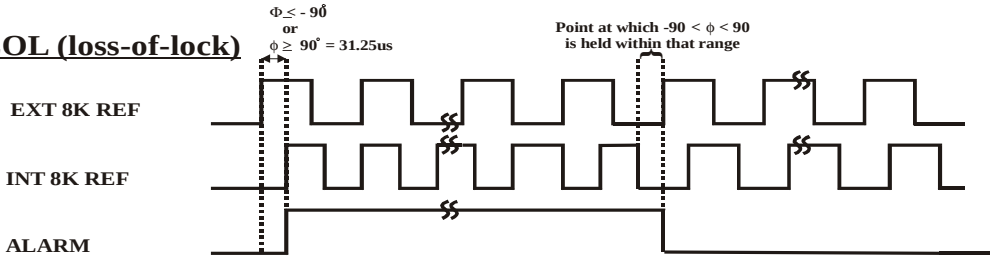
NOTE 5.0: On alarm assertion, switch references. If alarm is still active, force Free Run.

Figure 2.0: SCG2500 Alarm Timing

LOR (loss-of-reference)



LOL (loss-of-lock)



NOTE: LOL is disabled during a reference switch for the time before the 1st rising edge of the new reference + 1ms

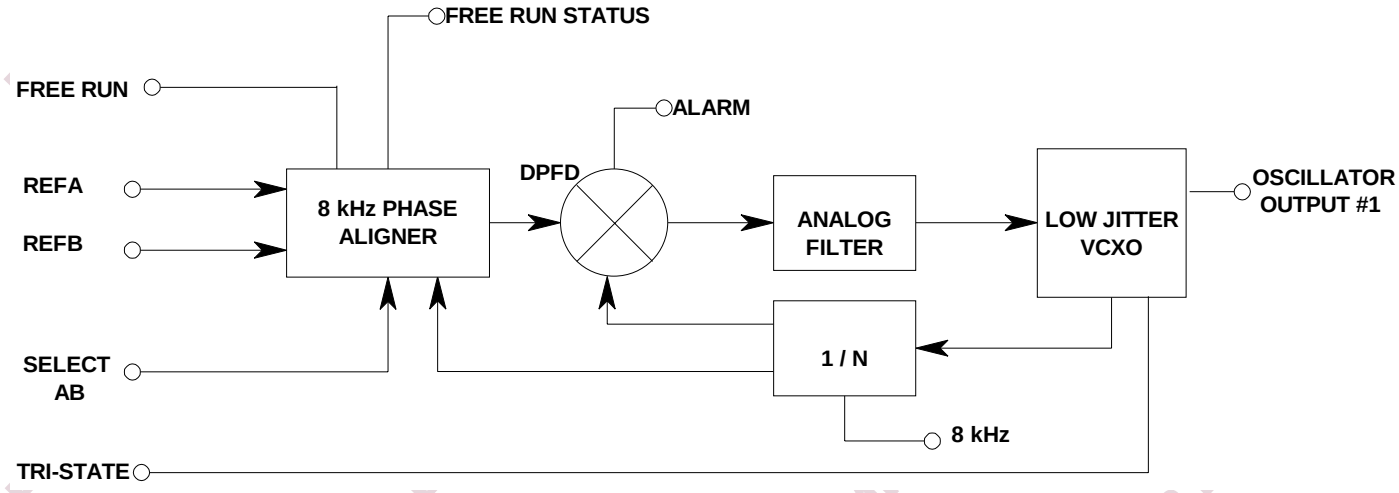
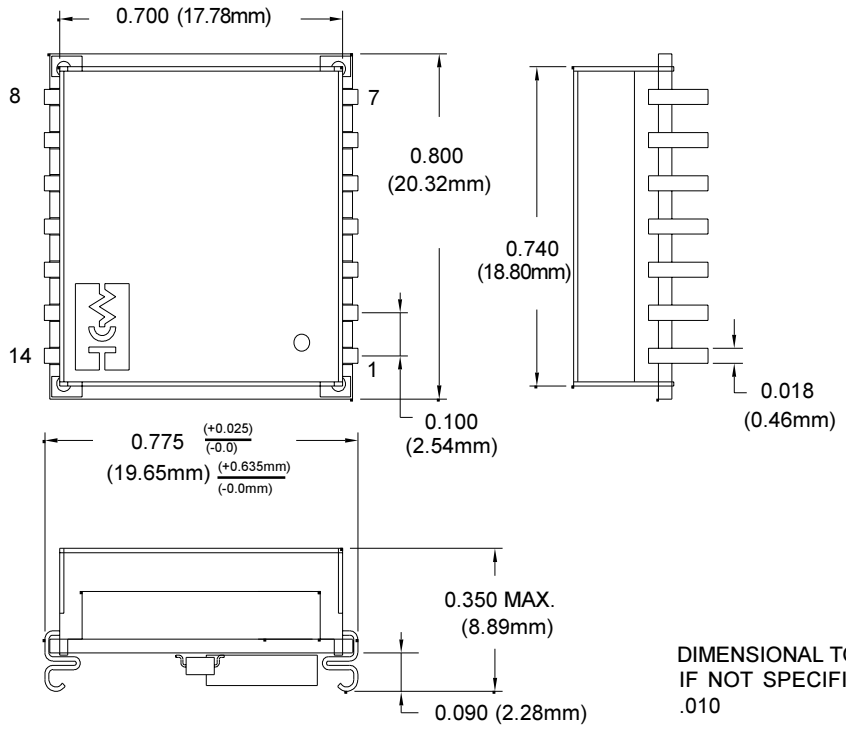


Figure 4.0 - Package Dimensions



ORDERING INFORMATION:

SCG2500 - 1.544

SCG2500 - 2.048

SCG2500 - 19.44

SCG2500 - 20.48

SCG2500 - 34.368

SCG2500 - 44.736

SCG2500 - 51.84

SCG2500 - 77.76

Figure 5.0- Circuit Board Footprint

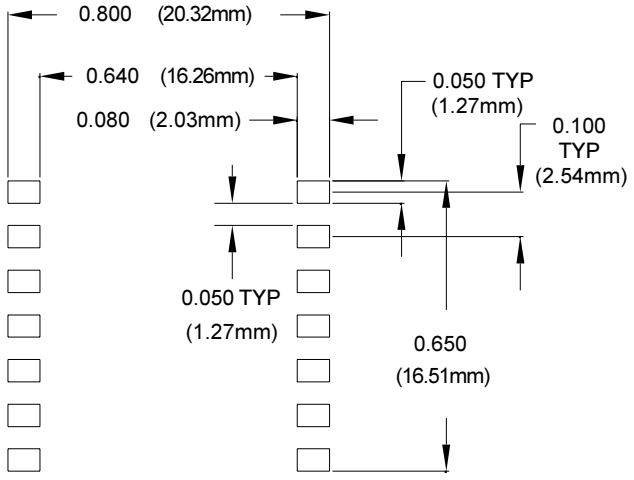


Figure 6.0- Tape and Reel Packaging

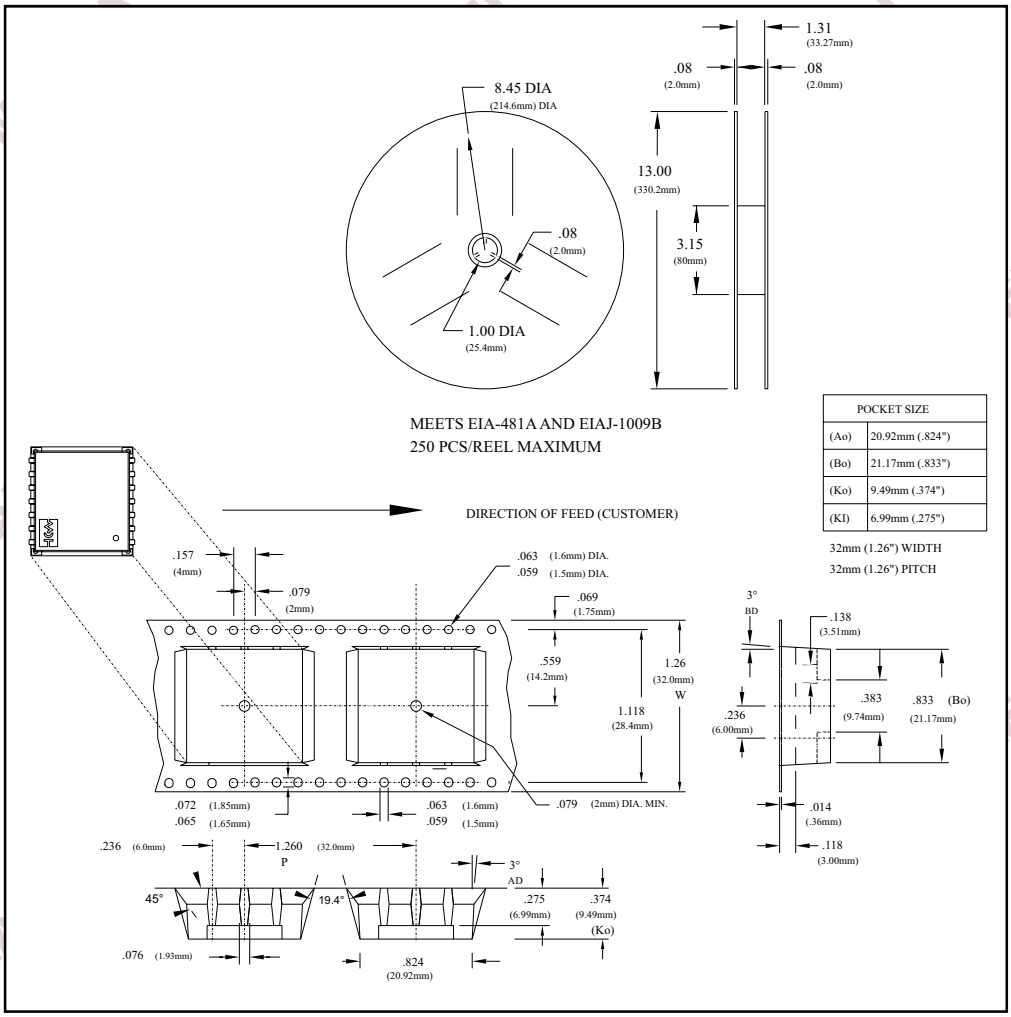
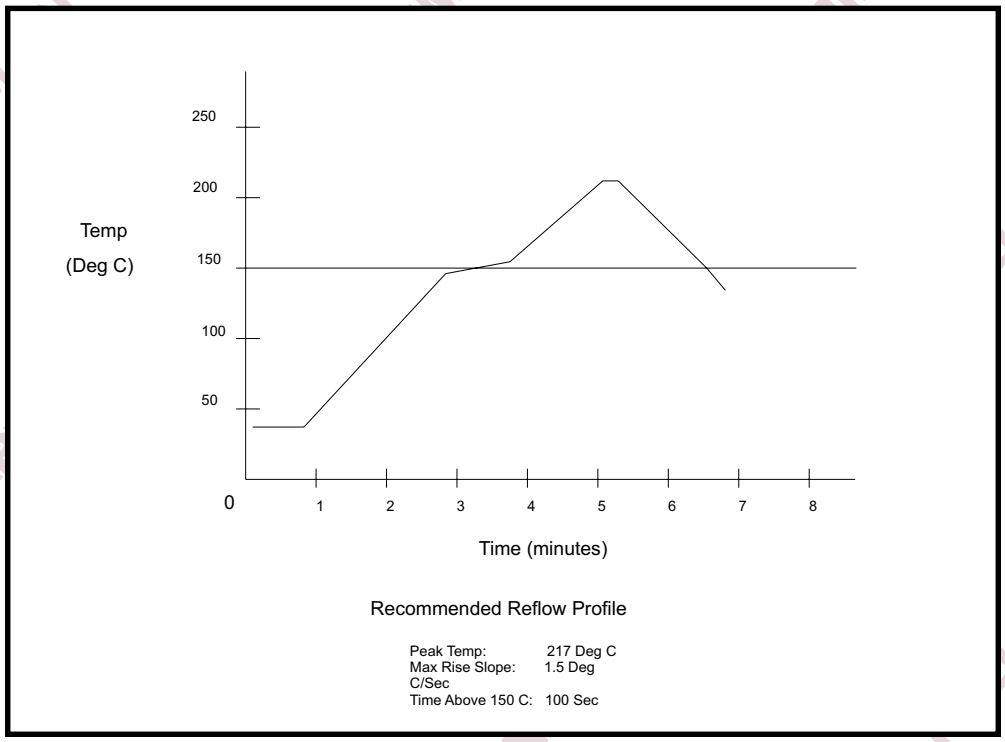


Figure 7.0 Solder Profile



REVISION HISTORY:

P00	3/26/01	-Preliminary Product Release