Using the S39421 as the Primary Control Circuit on a VME Live Insertion Card

High availability is a key feature of many types of systems today. Whether the system is a central office switch, a private branch exchange or a server it is important the system stay up and running while adding new services (add-in cards) or replacing faulty boards. Therefore, a means for inserting and removing cards while the entire system is powered-on (live) is a necessity.

Live insertion poses a number of challenges for the add-in card designer. For live insertion to be trouble free we first need to prevent damage to components on the add-in card due to improper supply sequencing. Secondly, voltage drop on the system power busses must be prevented in order to avoid unwanted system reset condition. Lastly, the integrity of the system's signals needs to be maintained when additional circuitry is connected to the bus.

Based upon the proposed Live Insertion System Requirements the S39421 is an ideal candidate as the add-in card's live insertion controller.

Sequencing the Voltages

The proposed live insertion specification[1] outlines 26 operational steps during the insertion of a card. These are broken down into two major categories; the "Insertion Process" and the "Typical Board Recognition Process."

The first 6 steps have to do with the insertion of the card and sequencing the discharge of any voltage potentials so that by the time the board is ready to make contact with the backplane no ESD discharges will occur. Even though the balance of the actions tend to overlap they can be viewed as two operations: the add-in card/backend logic sequencing and the backplane/add-in card interface sequencing.

Add-in Card/Backend Logic Sequencing

The process of electrical insertion begins with the contact of special ground and voltage pins. These are longer than the signal and power pins and they are physically located at opposite ends of the connector. The voltage pins are labeled Vpc (pre-charge Voltage), this is the backplane's 5 volt supply and the intent is for this voltage to be used to power the sequencing circuitry, any ASICs that interface to the bus and to pre-charge the 'bus-side' lines of the signal transceivers.

The PC board should be laid out so that ground is routed to all circuits, i.e. grounds should not be linked via the PCB connector. Vpc should be tied directly to the VCC5 pin on the S39421 and the device will immediately begin driving its backend circuit control signals [SGNL_VLD, CARD_V_VLD, $\overline{\text{RESET}}$ and RESET] and it will place the voltage ramp control signals [VGATE3, VGATE5 and $\overline{\text{DRVREN}}$] in the off state.

The next step is for the controller to recognize that the board is properly seated in the connector. VME has an optional feature that lends itself ideally to this step of the operation; the ejector handles can be used to activate a switch when they are fully rotated and locked. Switch closure can be used as the $\overline{\text{PND1}}$ and $\overline{\text{PND2}}$ inputs on the S39421. The pull-up resistor used for this implementation must be tied to Vpc because the backend voltages will not yet have been switched on by the S39421.

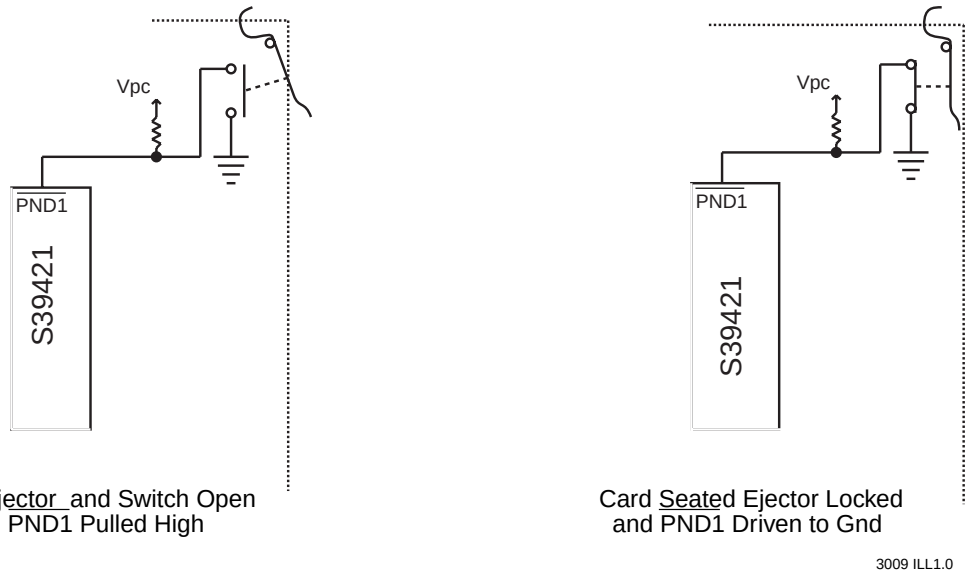

Figure 1: Illustration of Card Injector/Ejector Switch Circuit.

The board's pins should now be mated with the backplane connector which in turn will bring the host LI/I* and RESET* signals to the S39421. These signals should be tied to the device's HST_PWR and $\overline{\text{HST\_RST}}$ inputs respectively. Whenever HST_PWR is low the outputs controlling the backend power on sequencing will be inhibited; it does not impact the reset outputs or reset timer. When low, the $\overline{\text{HST\_RST}}$ input will force the reset outputs active; once it is released the reset timer will be started and it will keep the reset outputs active for t_{PURST}.

At the same time the signal pins are making contact, the backend voltages are applied to the card (3.3V, 5V, +12V and -12V on short pins), but, they are blocked by FETs under the control of the S39421 (see figure 3). Depending upon the state of the VSEL pin, the S39421 will monitor either the bussed +5V only, the bussed +3.3V only or both the bussed +5V and +3.3V. Once the S39421 has determined these supply voltages are at or above Vtrip, (and LI/I* has released HST_PWR) it will release the VGATE outputs and effectively turn them on at a rate equivalent to 250V/second. At the same time it will force $\overline{\text{DRVREN}}$ active thus providing power to the backend circuits.

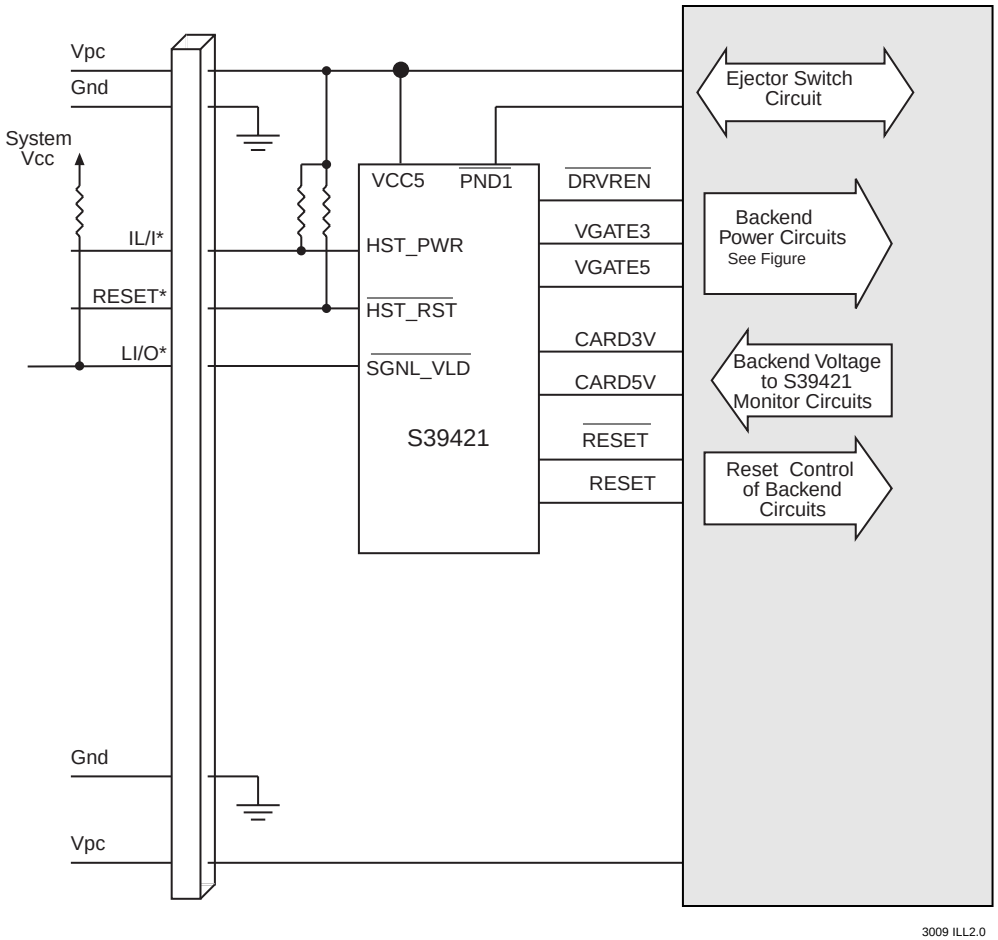

Figure 2: General Block Diagram of S39421 Host Bus Interface and Backend Signal Interface

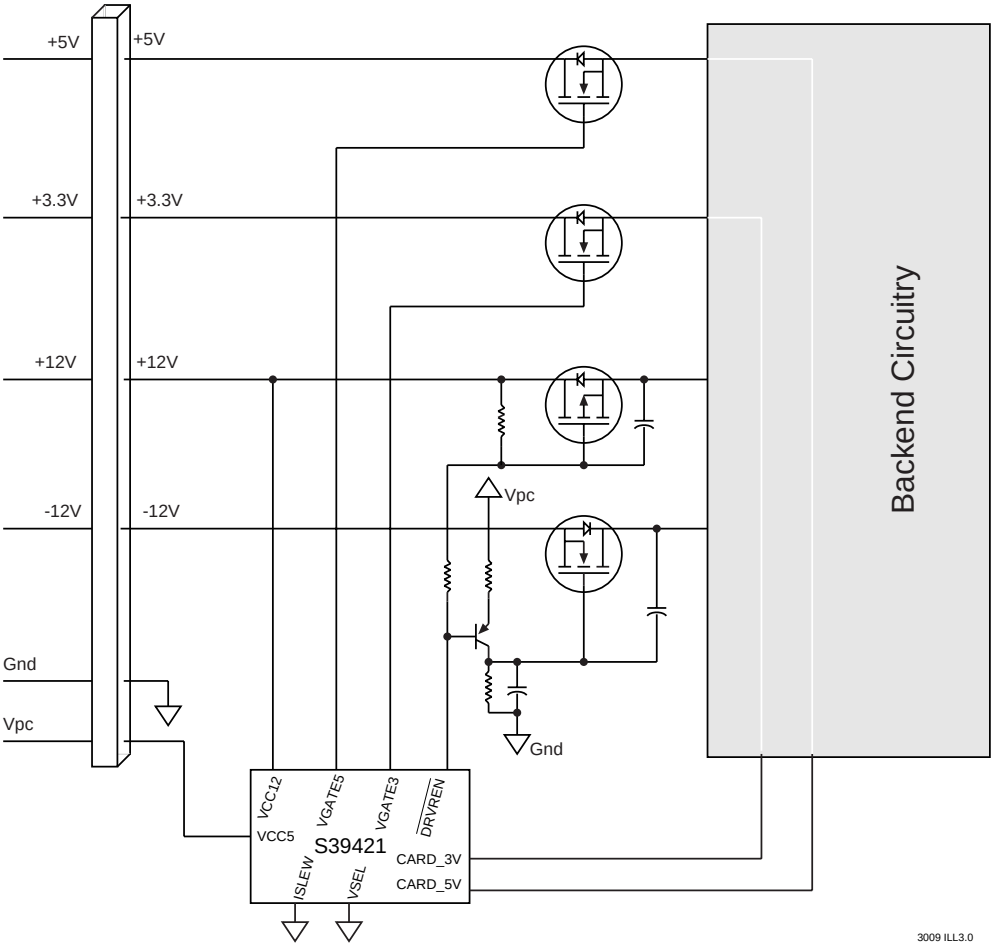

Figure 3: Backend Voltage Control Circuit

The S39421 will now begin monitoring the backend circuit voltages and when they are at or above Vtrip the reset timer will be released to begin the time out period and CARD_V_VLD will be released. After tPURST has expired, the reset outputs will be released and $\overline{\text{SGNL\_VLD}}$ will be driven active. The $\overline{\text{SGNL\_VLD}}$ signal can be tied to the host LI/O* signal pin to indicate the card has been fully powered, cleanly reset and is ready for action.

Backplane/Add-in Card Sequencing

A more complicated problem than the sequencing shown above is the signal bus interface. Inserting unpowered circuits onto the signal bus could lead to a situation of damaging components and much more likely disrupting the signals on the backplane. This will involve a rigorous evaluation and selection process by the design engineer to determine the best solution for the individual application. However, we can examine a product family that should resolve most of the issues the designer might encounter. The proposed VME Live Insertion spec actually helps us narrow this down quickly by recommending the use of ABTE logic. This is available from at least two large manufacturers of semiconductors.

Avoidance of Bus Conflicts

Bus conflicts arise when two or more interface circuits attempt to drive the bus simultaneously with one circuit driving high and the other driving low. The device trying to drive low will most likely not incur damage. But the device trying to drive high will be dropping 5Volts on its output at up to 120mA current. Even for very short periods of time the high temperatures this will generate can either destroy the device or adversely affect the long-term reliability of the device. The best solution is to insure the transceiver's enable input is actively driven before the transceiver is powered-on. Using one of the reset outputs (as shown in figure 4) as a gating signal to a single enable input style transceiver is one solution. With a dual enable transceiver one of the reset outputs can be tied directly to appropriate enable input.

Pre-bias

The switching capacitance of the individual signal lines at the interface must be charged to the instantaneous voltage on the corresponding bus line. These currents distort the signal that is being transmitted at that instant. To address this issue the proposed VME Live Insertion Spec states: “All VME system drivers and receivers SHALL be pre-biased to 1.7 =/-0.2 Vdc with a resistive network powered by the pre-charge +5V. . . before the board signal pins contact the backplane VME64 bus connector(s).” The ABTE logic addresses this issue head-on by providing a separate VCCBias pin that is internally connected to a pre-charge resistor network.

CARD REMOVAL

A clean transition for card removal can be performed either by the opening of the injector/ejector levers which in turn opens the switches that force the $\overline{\text{PND}}$ inputs to ground or by the host driving LI/I* low. Both actions will tell the S39421 to disable the high side drivers and force the reset outputs active.

RECAP

As the board is first inserted into the backplane voltage potentials on are shunted to ground thru the use of various bleed resistors and physical contact with the chassis frame. These are make then break processes so that by the time the card is ready to make contact with the backplane connector the board is electrically isolated from the frame.

The first pins of the connector to make contact with the backplane are ground and Vpc (pre-charge VCC). Vpc should be tied directly to the S39421 and the transceiver BiasVcc input. Once the S39421 detects the presence of Vpc it will begin driving the reset outputs active, shut off all the control signals to the power FETs and begin driving the LI/O* low. The injector/ejector levers will close the switches grounding the $\overline{\text{PND}}$ inputs allowing the S39421 to check the state of the VSEL pin and determine what bus voltages should be monitored. If the bus voltages are at or greater than Vtrip **AND** LI/I* has been released the S39421 will turn on the high side driver outputs VGATE3 and VGATE5 and the $\overline{\text{DRVREN}}$ output.

The voltages to the backend logic are applied with a nominal slew rate of VGATE3 and VGATE5 set at 250V/sec. The backend voltages should also be fed back to the S39421 and as soon as they are at or above their Vtrip level, the CARD_V_VLD will be released. If the host has released its $\overline{\text{RESET}}$ input and LI/I* input, the S39421 will release the timer for its reset circuit. After tPURST the reset outputs to the backend logic will be released and the $\overline{\text{SGNL\_VLD}}$ output will be driven active [backplane signal LI/O]. This is the final step in activating a board for live insertion.

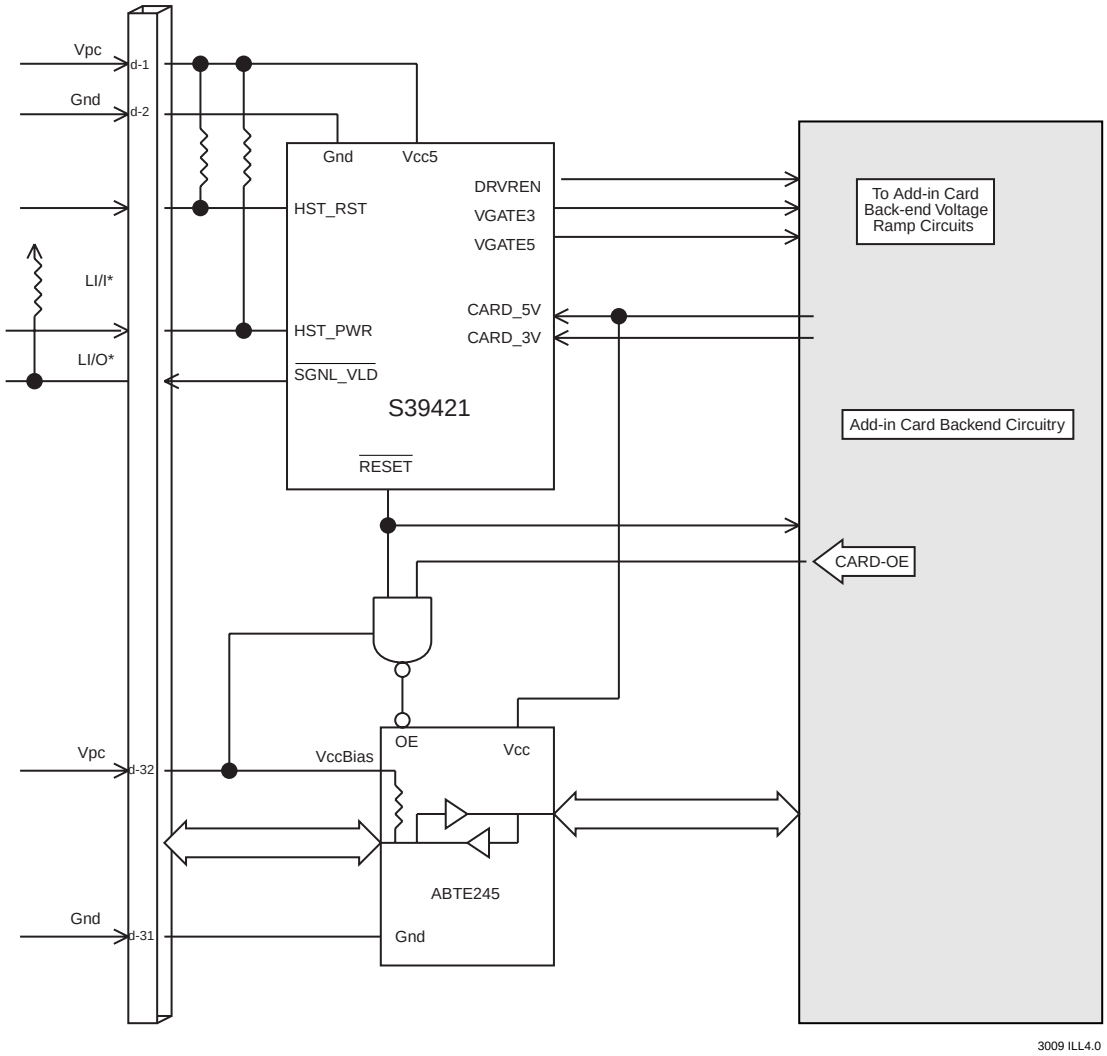

Figure 4: A Bus Interface Solution

Appendix A

MOSFETs suitable for use with the S39421 Hot-Swap Controller Mar-98

N-Channel MOSFETs

Part Number	Manufacturer	$V(BR)_{DSS}$	$R_{DS(on)}$ @ V_{GS}=10V	I_D cont.	Package
IRF7603	Int. Rectifier	30V	35 milliohms max	4.5A	Micro-8
IRF7413	Int. Rectifier	30V	11 milliohms max	9.2A	SO-8
Mi4412	MagePOWER	30V	28 milliohms max	7A	SO-8
Mi4410	MagePOWER	30V	12 milliohms max	7A	SO-8
MTSF3N03HD	Motorola	30V	40 milliohms max	3A	Micro-8
MMSF7N03HD	Motorola	30V	28 milliohms max	8A	SO-8
MTD20N03HDL2	Motorola	30V	35 milliohms max	20A	DPAK
Si6434DQ	Temic	30V	28 milliohms max	5.6A	TSSOP-8
Si6410DQ	Temic	30V	14 milliohms max	7.8A	TSSOP-8
Si4412DY	Temic	30V	28 milliohms max	7A	SO-8
Si4416DY	Temic	30V	18 milliohms max	9A	SO-8

P-Channel MOSFETs

Part Number	Manufacturer	$V(BR)_{DSS}$	$R_{DS(on)}$ @ V_{GS}=10V	I_D cont.	Package
IRF7606	Int. Rectifier	-30V	90 milliohms max	2.9A	Micro-8
IRF7416	Int. Rectifier	-30V	20 milliohms max	7.1A	SO-8
Mi4431DY	MagePOWER	-30V	40 milliohms max	5.8A	SO-8
Mi4435DY	MagePOWER	-30V	20 milliohms max	8A	SO-8
MTSF2P03HD	Motorola	-30V	90 milliohms max	2.4A	Micro-8
MMSF3P02HD	Motorola	-20V	75 milliohms max	3A	SO-8
MTD20P03HDL2	Motorola	-30V	99 milliohms max	19A	DPAK
Si6435DQ	Temic	-30V	90 milliohms max	4.5A	TSSOP-8
Si6415DQ	Temic	-30V	19 milliohms max	6.5A	TSSOP-8
Si4431DY	Temic	-30V	40 milliohms max	5.8A	SO-8
Si4435DY	Temic	-30V	20 milliohms max	8A	SO-8

References:

VITA Standards Organization, November 1997, *VME64x Live Insertion System Requirements Draft Standard*

Summit Microelectronics, Inc. S39421 Data Sheet

Texas Instruments Application Note SDYA012, October 1996, *Live Insertion*