March 11, 1998

TEL:805-498-2111 FAX:805-498-3804 WEB:http://www.semtech.com

Application Information

The SC1131/2/3/4 series of combination Linear and Switching Regulators is aimed at split voltage plane microprocessors having Vcore of 3.5V down to 1.8V. Programming of the output voltage is achieved using a 4-resistor matrix and a DIP switch and allows a 0.1V incremental change over the full voltage range (Fig.3). The switcher section of the SC113X can deliver a maximum current of at least 14A (with adequate air flow).

The linear section is guaranteed for 1.5, 3, 5 and 7.5A for use in systems requiring 3.3V +/-1% with exceptional stability and ripple rejection.

The SC113X was designed as an “embedded solution” for motherboard manufacturers. To assist with this task the evaluation module (Semtech p.n. 17107) was developed, which together with the Dynamic Load (Semtech p.n.17108) provides an excellent means of testing and evaluation of the product.

The schematic diagram for the SC113X Module is shown in Fig.6. The step-down Buck regulator consists of logic-level MOSFET Q1, Schottky Diode D1, Inductor L1, and an output capacitor bank all being PWM controlled by drive pin 1 of the integrated circuit U1.

The SC113X utilizes a fixed frequency voltage-mode controller with triangular oscillator (Fig.1) and internally compensated error amplifier which provides a hassle-free solution for MB designers.

SC113X fits into the 7-lead T0-220 package. This important feature allows for easy heat removal by means of a variety of heatsinks depending on air flow available in the particular system configuration. However, one needs to be aware of the lead length required to mount the T0-220 on the PCB (Fig.2) and to **keep minimal distance to bypassing capacitors, such as C3, C4, C5 and C13.**

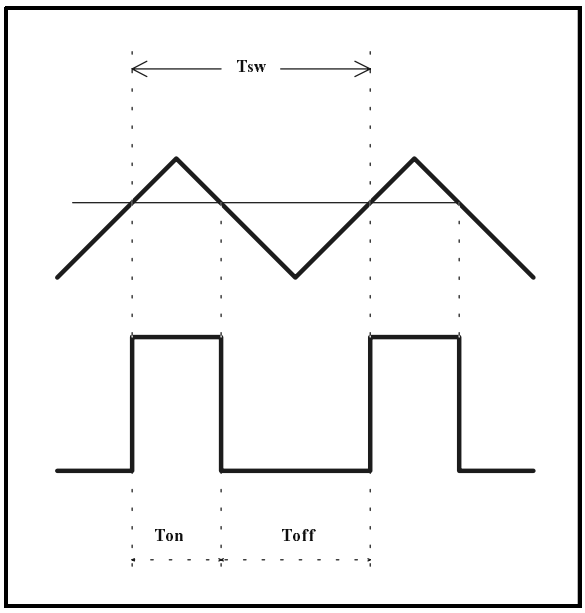

Fig.1

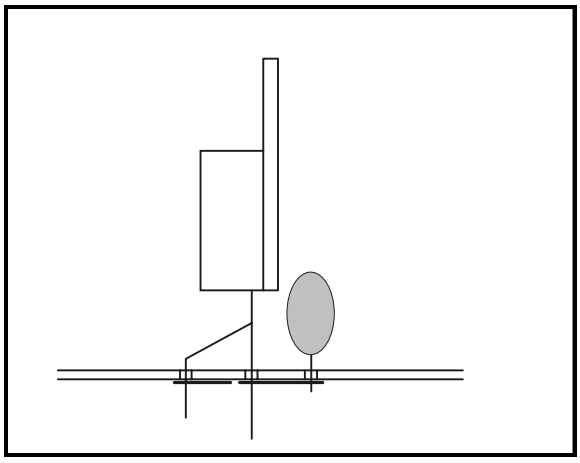

Fig.2

March 11, 1998

Application Information (cont.)

The PCB was designed using 1oz. copper double-sided material (Fig.7 & 8) giving the motherboard designers a first cut approximation of a working layout. Component placement is shown in Fig. 9 and Fig.10.

Switch S1, LED1, connector J1 and the DIP-switch are for demo purposes only. The same applies to the two sets of terminals J2, J3 and J4, J5 which are used on the evaluation board to observe transient response, voltage regulation and output ripple voltage under different load conditions. The waveforms in Fig. 4 and Fig. 5 illustrate actual tests done with SC1133 in the evaluation board.

The number of input (C1, C2) and output (C8, C9, C10, C11) capacitors (1500uF,6.3V) depends on the particular application and load requirements. The application circuit in Fig.6 meets the Intel specification for a slew rate of 30A/usec with a maximum load of greater than 14A.

JP4	JP3	JP2	JP1	Vout
0	0	0	0	1.8
0	0	0	1	1.9
0	0	1	0	2.0
0	0	1	1	2.1
0	1	0	0	2.2
0	1	0	1	2.3
0	1	1	0	2.4
0	1	1	1	2.5
1	0	0	0	2.6
1	0	0	1	2.7
1	0	1	0	2.8
1	0	1	1	2.9
1	1	0	0	3.0
1	1	0	1	3.1
1	1	1	0	3.2
1	1	1	1	3.3

Fig.3

SC1133 Efficiency in Application Circuit

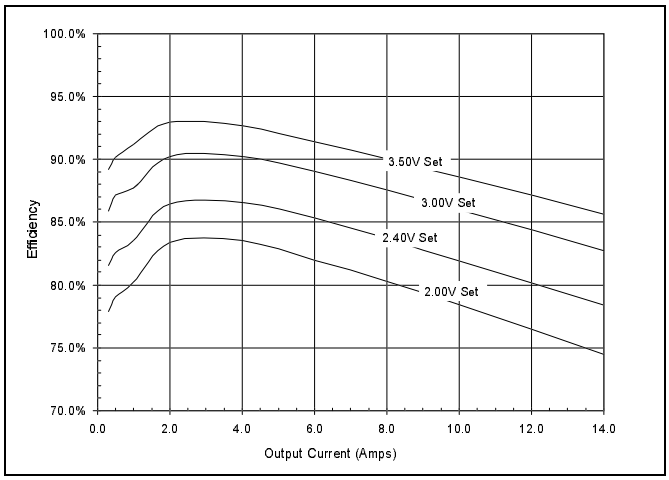

Fig.4

Application Circuit Ripple, 3.1V, 0A out

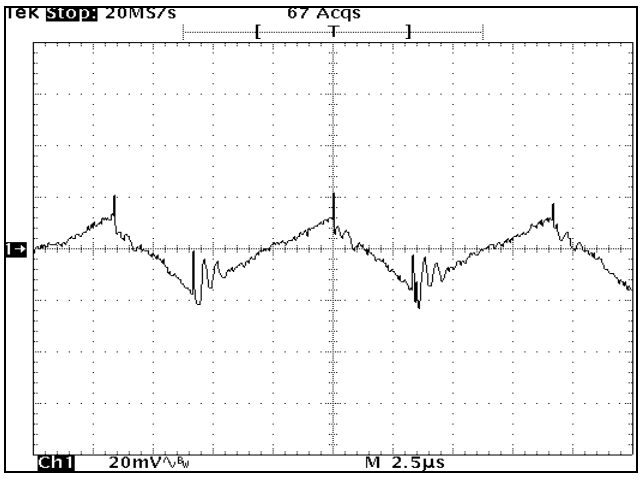

Fig.5

March 11, 1998

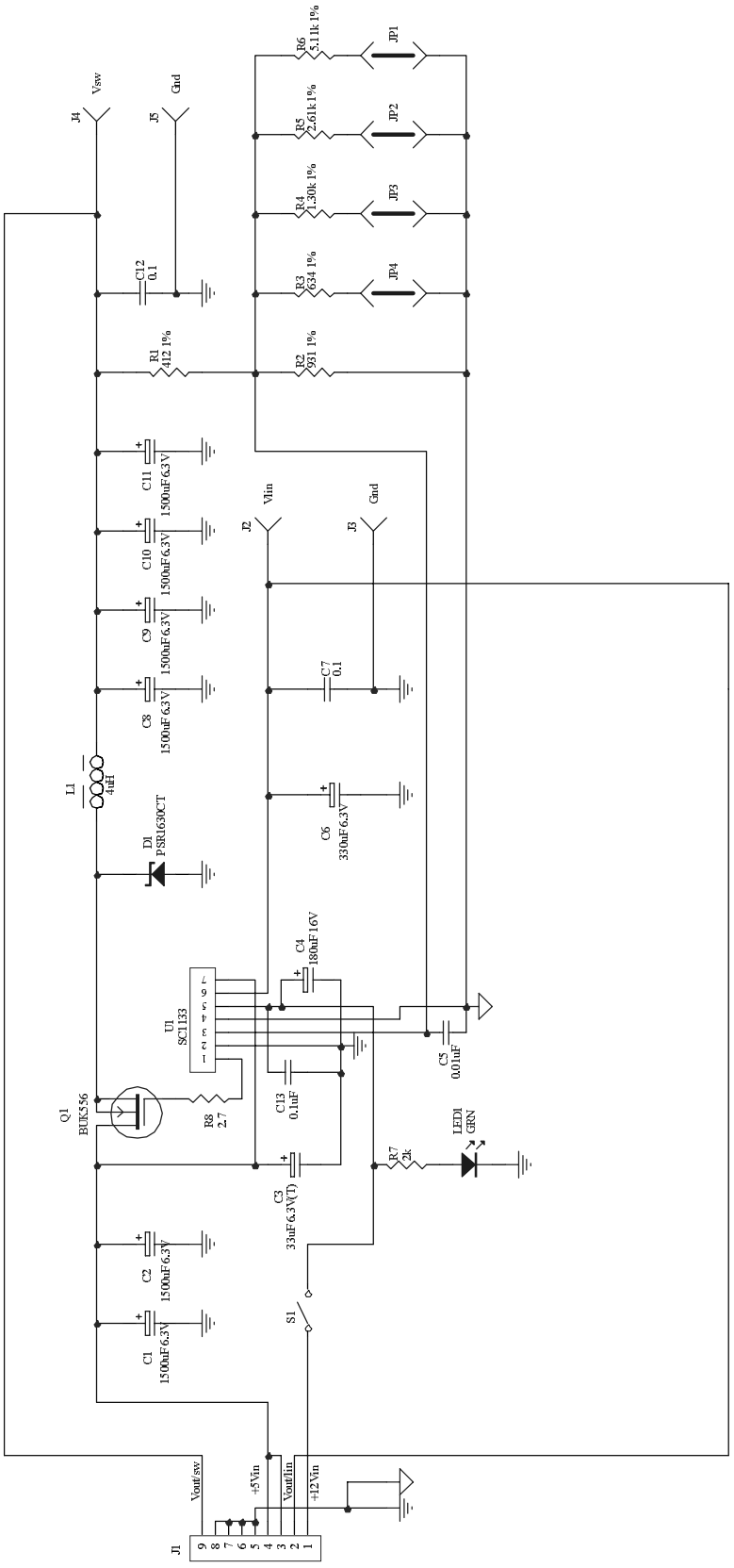

Fig.6

March 11, 1998

Bill of Materials			
Comment	**Pattern**	**Quantity**	**Components**
0.01µF 50V X7R 0805	0805	1	C5
0.1µF 20% 16V X7R	SMT/1206	2	C7, C12
0.1µF 50V X7R	RAD0.1	1	C13
1.30kΩ 1%	1206	1	R4
180µF 16V/P5667	RB0.1/0.25	1	C4
2.61kΩ 1%	1206	1	R5
2.7Ω 5% 1/8W	AXIAL0.3	1	R8
2kΩ 5%	1206	1	R7
330µF 6.3V/P5605	RB0.1/0.25	1	C6
33µF 6.3V/P2016	RB0.1/0.18	1	C3
412Ω 1%	1206	1	R1
5.11kΩ 1%	1206	1	R6
574502B03700/AAVID	HS574X02	3	HS1, HS2, HS3
6.3MV1500GX/SANYO	RB0.2/0.41	6	C1, C2, C8, C9, C10, C11
634Ω 1%	1206	1	R3
8102-14N/LYN-TRON	POST1.00"	4	POST1, POST2, POST3, POST4
931Ω 1%	1206	1	R2
B17059A/SEMTECH	TOR0.8/16AWG	1	L1
BD01/C&K	SW0.3	1	S1
BD04/C&K	SWDIP4	1	JP1-4
BUK556/PHILIPS	TO-220/V	1	Q1
ED1974-ND	TERM3X0.2"	3	J1A, J1B, J1C
ED5014-ND/DIGIKEY	TESTPOINT1	4	J2, J3, J4, J5
LT1080-ND/DK	LED3MM	1	LED1
PSR16C30CT/PHOTRON	TO-220/V	1	D1
SC1133CT/SEMTECH	TO220-7LEAD	1	U1
WIREINS0.8"22AWG	WIRE0.8"	1	W1

March 11, 1998

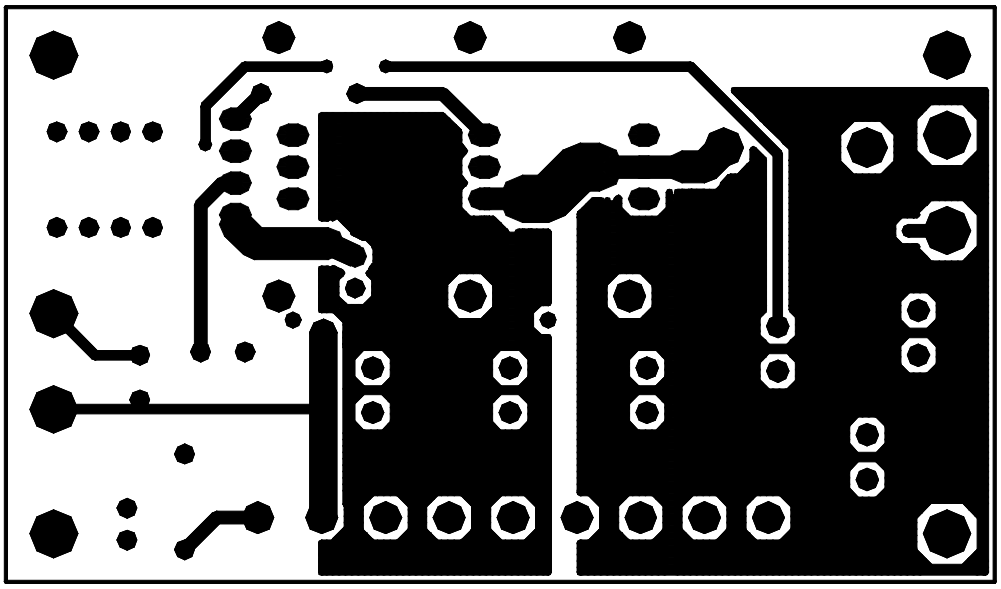

Fig.7

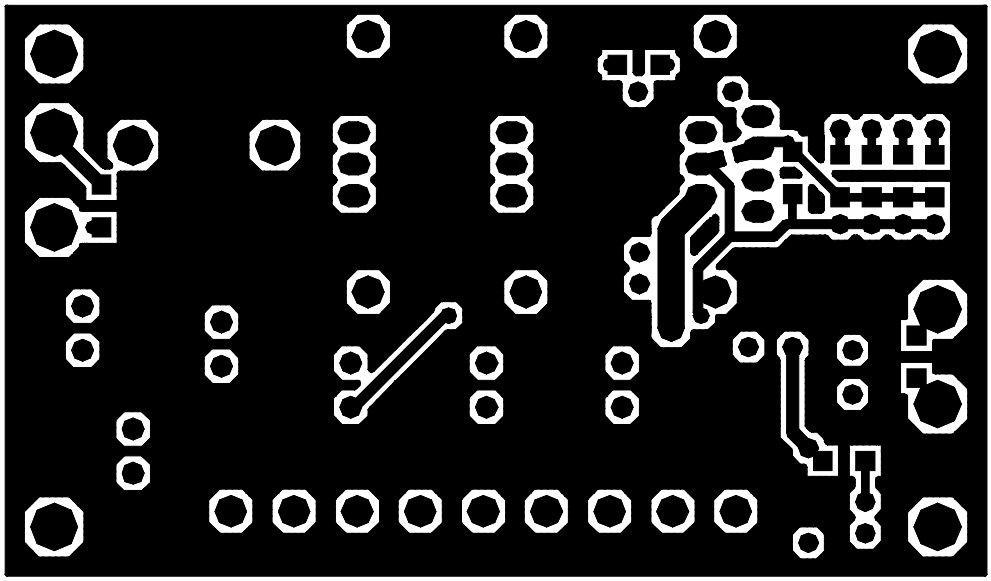

Fig.8

March 11, 1998

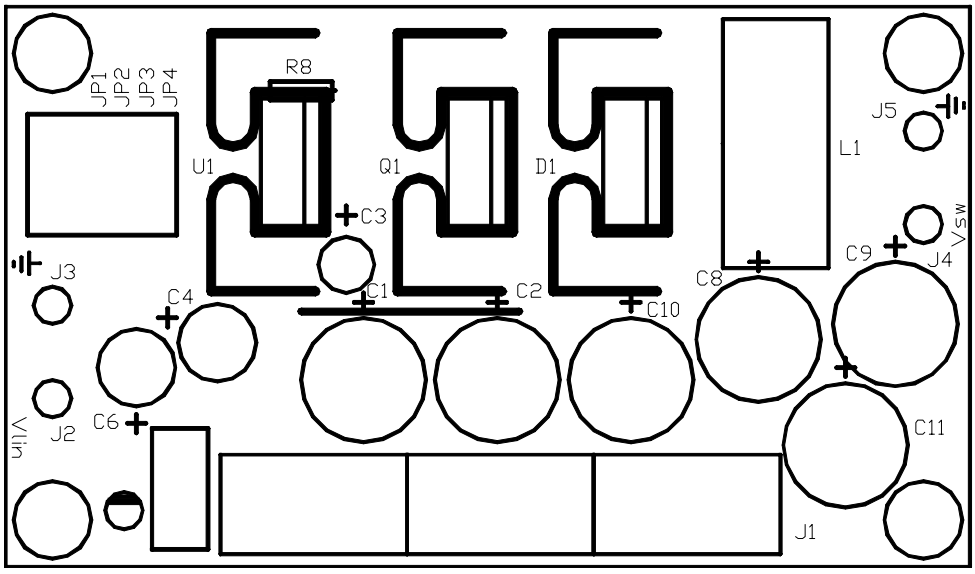

Fig.9

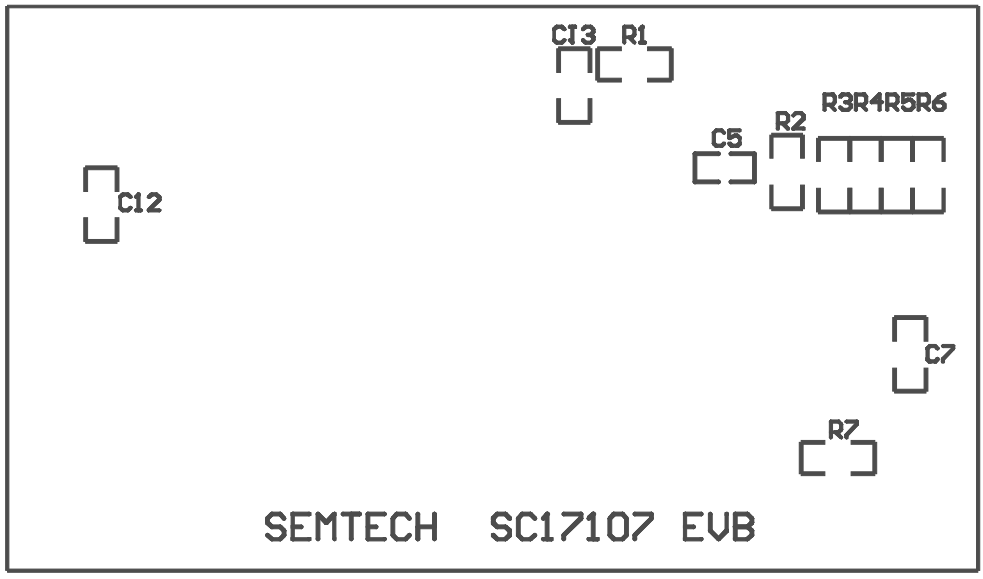

Fig.10