SCIC-DVC-101

16 Channel ISC Integrated Circuit

FEATURES

- 16 Analog Channels
- Independently User Configurable
- Programmable Gain And Offset
- Programmable bypass, 4 or 8 pole filtering
- Over Voltage Protection
- Single 5 Volt Operation
- 160 Lead Thin Quad Flatpack
- Available In Die Form

APPLICATIONS

- Munitions Testing
- General Analog Signal Conditioning
- Sensor Integration
- Industrial Instrumentation
- Patient Monitoring
- System Health Monitoring

GENERAL DESCRIPTION

The 16 Channel Input Signal Conditioner (ISC) IC provides analog signal conditioning that is required for many sensors in today's modern instrumentation systems. The ISC chip has 16 analog input channels that can be independently amplified, offset, and filtered. The 16 channels can be accessed independently or multiplexed into one analog channel for output. The channel gain, offset, and filtering bandwidth are channel independent and digitally controlled through a digital configuration interface.

A detailed drawing of the 16 Channel ISC IC is shown in Figure 1.

Table 1 lists the number of channels and supported bandwidth per channel that can be available using the 16 Channel ISC IC assuming a 120K samples per second rate at the output of the ISC DAC.

Table 1: System Channels vs. Bandwidth		
Number of Channels	**Samples per Second per Channel**	**Bandwidth Supported for 2X oversampling**
1	120K	60 KHz
2	60K	30 KHz
4	30K	15 KHz
16	7.5K	3.75 KHz

The digitally programmable amplifier has a gain range from 1 to 100 in 256 steps. The offset is programmable in 0.014 Volt increments over 3.54 Volts (256 steps) centered about the voltage reference. A channel's filter programmability is based on a 4 bit divisor referenced off the system clock. The following are some possible corner frequencies: 60K, 30K, 15K, 7.5K, 3.75K, 1.875K, 938, 469, 234, 117, and 59.

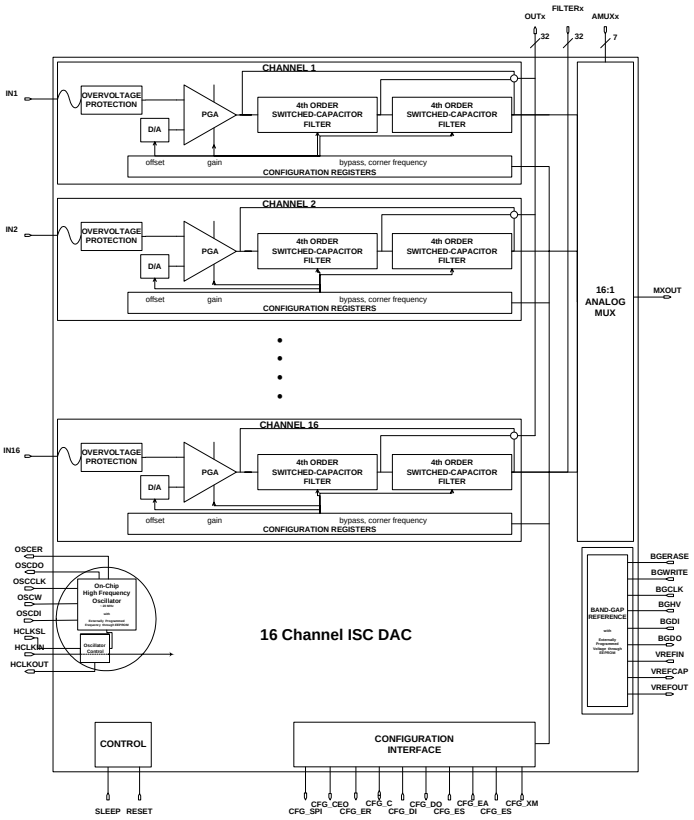

Figure 1: Functional Block Diagram

PROGRAMMING

The 16 Channel ISC IC initializes in a power-up default configuration that is hard-coded in the internal logic. If the chip is in configuration mode, a configuration file is loaded via the configuration interface from an external PROM. The configuration file contains the configuration data for the device(s).

Multiple Devices with different configurations can be connected together in a "daisy chain", and a single combined bit stream used to configure the chain of devices as shown in Figure 2.

The ISC configuration data contains the following:

- Offset for each channel
- Gain for each channel
- Filter Control
  - Bypass
  - Corner Frequency
  - Order (4/8)

Configuration software is available for the PC environment.

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HARDENED SUBMINIATURE TELEMETRY AND SENSOR SYSTEM
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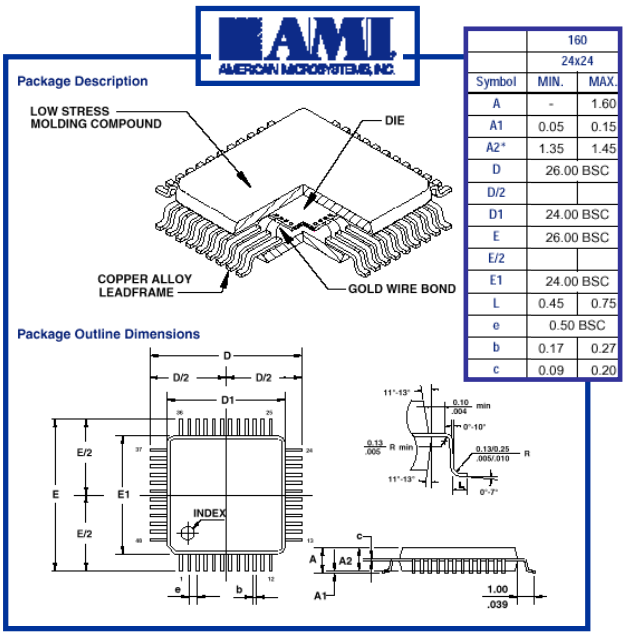

	160
	24x24
Symbol	MIN. / MAX.
A	- / 1.60
A1	0.05 / 0.15
A2*	1.35 / 1.45
D	26.00 BSC
D/2	
D1	24.00 BSC
E	26.00 BSC
E/2	
E1	24.00 BSC
L	0.45 / 0.75
e	0.50 BSC
b	0.17 / 0.27
c	0.09 / 0.20

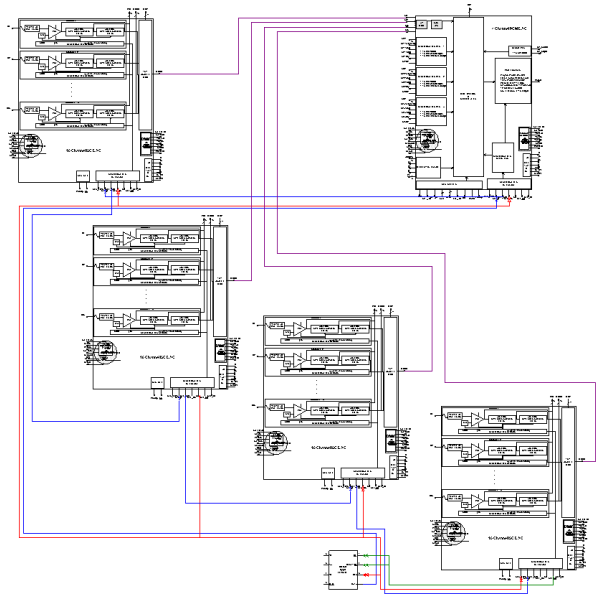

Figure 2: 64 Channel HSTSS PCM DAC System

SPECIFICATIONS

Parameter		Symbol	Min	Typ	Max	Units
Power Requirements						
Supply Voltage	Digital	V_{DDD}	4.5	5.0	5.5	V
	Analog	V_{DDA}	4.5	5.0	5.5	V
Supply Current	Operating	I_{DD}			180	mA
	Low-Power	I_{PD}		TBD		uA
Power Consumption	Operating				900	mW
	Low-Power			TBD		uW
Dynamic Specifications						
Operating Ambient Temperature		T_A	-40	25	85	°C
Voltage Reference		V_{REF}	1.5	2.25	2.5	V
Clock Frequency		F_C		23		MHz
Analog Frequency Response			DC		240K	Hz
Signal to Noise		S/N	54			dB
Total Harmonic Distortion		THD			0.14	%
Interchannel Isolation				60		dB
Interchannel Gain Mismatch					±0.5	dB
Absolute Gain Error				± 1	± 2	%
Gain Drift				100	200	ppm/°C
Analog Inputs						
Signal Input Span		V_{pp}	$0.1*V_{REF}$		$1.8*V_{REF}$	V
Input Capacitance		C_{INA}			15	pF
Input Resistance		R_{INA}	1M			Ω
Analog Outputs						
Signal Output Span		M_{OUT}	$0.1*V_{REF}$		$1.8*V_{REF}$	V
Output Resistance		R_{OA}		600	1K	Ω
External Load Capacitance		C_{LA}			20	pF
External Load Resistance		R_{LA}	10K			Ω
Clock						
Duty Ratio		CLK	45	50	55	%
Clock High Voltage		V_{CLKH}	$0.7xV_{DDD}$		V_{DDD}	V
Clock Low Voltage		V_{CLKL}	0		$0.3xV_{DDD}$	V
Digital Inputs and Outputs						
Input High Voltage		V_{INHD}	2.4		V_{DDD}	V
Input Low Voltage		V_{INLD}	0		0.8	V
Input Current		I_{IND}			± 1	µA
Input Capacitance		C_{IND}			10	pF
Output High Voltage		V_{OHD}	4.0		V_{DDD}	V
Output Low Voltage		V_{OLD}	0		0.4	V

EXAMPLE APPLICATION

The 16 Channel ISC IC was originally developed to support expandability for the 4 Channel PCM IC (PMIC-DVC-101) and the HSTSS PCM DAC architecture. In the architecture shown in Figure 2, four 16 Channel ISC DACs provide 64 signal conditioned channels to be sampled by a single 4 Channel PCM IC.

PACKAGING

The Thin Quad Flatpack (TQFP) plastic package family is a reduced thickness plastic surface mount package. The 160 lead TQFP packages are constructed using the latest wire bonding and molding technology to provide surface mount packages with a body thickness of 1.0 or 1.4mm. This package finds many applications where size and weight are a critical factor.

The 16 Channel ISC IC will be available in die form.

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