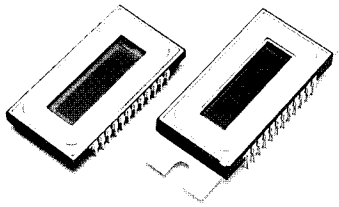
NEW

IMAGE SENSOR

CCD area image sensor
S7960/S7961-1008

Back-thinned FFT-CCDs for high-speed application



S7960/S7961-1008 are FFT-CCD image sensors specifically designed for high speed operation. By employing a wide band width on-chip amplifier and low resistance metal interconnects for the parallel register enables high frame rate. In binning operation, S7960/S7961-1008 can be used as a linear image sensor having a long aperture in the direction of the device length. The binning operation offers significant improvement in signal-to-noise ratio and signal processing speed compared to conventional methods by which signals are digitally added by an external circuit. In area scan operation, S7960/S7961-1008 can be used as a high frame rate camera. S7960/S7961-1008 also feature low dark signal (MPP mode operation). S7960/S7961-1008 have an effective pixel size of 24 × 24 µm and is available in image areas of 24.576 (H) × 6.000 (V) mm.
One-stage peltier cooler is built into the package for thermoelectric cooling (S7961-1008). At room temperature operation, the device can be cooled down to -10 °C (Typ.) without using any other cooling technique. In addition, since both the CCD chip and the peltier cooler are hermetically sealed, no dry air is required, thus allowing easy handling.

Features

- High-speed on-chip amplifier
- Greater than 90 % quantum efficiency
- Wide spectrum range
- Built-in peltier cooler
- MPP operation
- Non-cooled type: S7960-1008
  One-stage TE-cooled type: S7961-1008
  (Two-stage TE-cooled type is optional)

Applications

- High-speed spectrometer
- High-speed UV imaging
- Optical and spectrophotometric analyzer

■Selection and order guide

Type No.	Cooling	Number of total pixels	Number of active pixels	Active area [mm (H) × mm (V)]
S7960-1008	Non-cooled	1044 × 256	1024 × 250	24.576 × 6.000
S7961-1008	One-stage TE-cooled			

A window material can be selected upon need, and the following is available.
AR-coated sapphire (standard): expressed by "S" #
Quart: expressed by "Q" #
Temporary window: expressed by "N" #
This should be added at the end of a type No. when ordered.
ex. S7960-1008S: AR-coated sapphire

■General ratings

Parameter	Specification
CCD structure	Full frame transfer
Fill factor	100 %
Number of active pixels	1024 (H) × 250 (V)
Pixel size	24 (H) × 24 (V) µm
Active area	24.576 (H) × 6.000 (V) mm
Vertical clock phase	2 phase
Horizontal clock phase	2 phase
Output circuit	Two-stage MOSFET source follower
Package	24 pin ceramic package
Window	AR coated sapphire Quartz, temporary window are available upon request

PRELIMINARY DATA
Feb. 2000

SOLID STATE DIVISION

■Absolute maximum ratings (Ta=25 °C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Storage Temperature	Tstg	-50	-	+50	°C
Operating Temperature	Topr	-50	-	+30	°C
OD Voltage	V_{OD}	-0.5	-	+25	V
RD Voltage	V_{RD}	-0.5	-	+18	V
ISV Voltage	V_{ISV}	-0.5	-	+18	V
ISH Voltage	V_{ISH}	-0.5	-	+18	V
IGV Voltage	V_{IG1V}, V_{IG2V}	-10	-	+15	V
IGH Voltage	V_{IG1H}, V_{IG2H}	-10	-	+15	V
SG Voltage	V_{SG}	-10	-	+15	V
OG Voltage	V_{OG}	-10	-	+15	V
RG Voltage	V_{RG}	-10	-	+15	V
TG Voltage	V_{TG}	-10	-	+15	V
Vertical Clock Voltage	V_{P1V}, V_{P2V}	-10	-	+15	V
Horizontal Clock Voltage	V_{P1H}, V_{P2H}	-10	-	+15	V

■Operating conditions (MPP mode, Ta=25 °C)

Parameter		Symbol	Min.	Typ.	Max.	Unit
Output transistor drain voltage		V_{OD}	12	15	18	V
Reset drain voltage		V_{RD}	11.5	12	12.5	V
Output gate voltage		V_{OG}	1	3	5	V
Substrate voltage		V_{SS}	-	0	-	V
Test point (Vertical input source)		V_{ISV}	-	V_{RD}	-	V
Test point (Horizontal input source)		V_{ISH}	-	V_{RD}	-	V
Test point (Vertical input gate)		V_{IG1V}, V_{IG2V}	-8	0	-	V
Test point (Horizontal input gate)		V_{IG1H}, V_{IG2H}	-8	0	-	V
Vertical shift register clock voltage	high	V_{P1VH}, V_{P2VH}	4	6	8	V
	low	V_{P1VL}, V_{P2VL}	-9	-8	-7	
Horizontal shift register clock voltage	high	V_{P1HH}, V_{P2HH}	4	6	8	V
	low	V_{P1HL}, V_{P2HL}	-9	-8	-7	
Summing gate voltage	high	V_{SGH}	4	6	8	V
	low	V_{SGL}	-9	-8	-7	
Reset gate voltage	high	V_{RGH}	4	6	8	V
	low	V_{RGL}	-9	-8	-7	
Transfer gate voltage	high	V_{TGH}	4	6	8	V
	low	V_{TGL}	-9	-8	-7	

■Electrical characteristics (Ta=25 °C)

Parameter	Symbol	Remark	Min.	Typ.	Max.	Unit
Signal output frequency	fc	-	-	1	10	MHz
Reset clock frequency	frg	-	-	1	10	MHz
Vertical shift register capacitance	C_{P1V}, C_{P2V}	-	-	6,400	-	pF
Horizontal shift register capacitance	C_{P1H}, C_{P2H}	-	-	300	-	pF
Summing gate capacitance	C_{SG}	-	-	7	-	pF
Reset gate capacitance	C_{RG}	-	-	7	-	pF
Transfer gate capacitance	C_{TG}	-	-	150	-	pF
Transfer efficiency	CTE	*1	0.99995	0.99999	-	-
DC output level	Vout	*2	7	10	13	V
Output impedance	Zo	*2	-	500	-	Ω
Power dissipation	P	*2, *3	-	100	-	mW

*1: Measured at half of the full well capacity. CTE is defined per pixel.

*2: V_{OD}=15 V, Load resistance=2.2 kΩ

*3: Power dissipation of the on-chip amplifier.

■Electrical and optical characteristics (Ta=25 °C, unless otherwise noted)

Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
Saturation output voltage		Vsat		-	Fw × Sv	-	V
Full well capacity	vertical	Fw	*4	150	300	-	ke⁻
	horizontal			300	600	-	
CCD node sensitivity		Sv	*5	1.8	2.2	-	μV/e⁻
Dark signal (MPP mode)	25 °C	DS	*6	-	4,000	12,000	e⁻/pixel/s
	0 °C			-	200	600	
Readout noise		Nr	*7	-	60	120	e⁻rms
Dynamic range	line binning	DR	*8	-	10,000	-	-
	area scanning			-	5,000	-	
Spectral response range		λ	-	-	200 to 1,100	-	nm
Photo response non-uniformity		PRNU	*9	-	-	±10	%

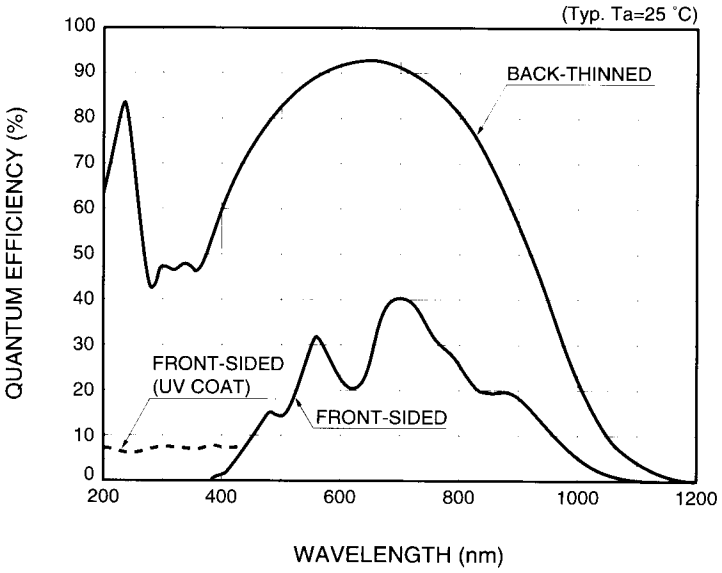
*4: Large horizontal full well for vertical binning operation.
*5: V_{OD}=15 V , Load resistance=2.2 kΩ
*6: Dark signal doubles for every 5 to 7 °C.
*7: -40 °C, operating frequency is 1 MHz.
*8: DR = Fw / Nr
*9: Measured at half of the full well capacity.
PRNU (%) = noise / signal × 100
Noise: fixed pattern noise (peak to peak)

■Pin connections

Pin No.	S7960 series		S7961 series		Remark
	Symbol	Description	Symbol	Description	
1	RD	Reset drain	RD	Reset drain	
2	OS	Output transistor source	OS	Output transistor source	
3	OD	Output transistor drain	OD	Output transistor drain	
4	OG	Output gate	OG	Output gate	
5	SG	Summing gate	SG	Summing gate	same timing as P2H
6	NC		NC		
7	NC		NC		
8	P2H	CCD horizontal register clock-2	P2H	CCD horizontal register clock-2	
9	P1H	CCD horizontal register clock-1	P1H	CCD horizontal register clock-1	
10	IG2H	Test point (Horizontal input gate-2)	IG2H	Test point (Horizontal input gate-2)	shorted to 0 V
11	IG1H	Test point (Horizontal input gate-1)	IG1H	Test point (Horizontal input gate-1)	shorted to 0 V
12	ISH	Test point (Horizontal input source)	ISH	Test point (Horizontal input source)	shorted to RD
13	TG	Transfer gate	TG	Transfer gate	same timing as P2V *10
14	P2V	CCD vertical register clock-2	P2V	CCD vertical register clock-2	
15	P1V	CCD vertical register clock-1	P1V	CCD vertical register clock-1	
16	NC		Th1	Thermistor	
17	NC		Th2	Thermistor	
18	NC		P-	Peltier-	
19	NC		P+	Peltier+	
20	SS	Substrate (GND)	SS	Substrate (GND)	
21	ISV	Test point (Vertical input source)	ISV	Test point (Vertical input source)	shorted to RD
22	IG2V	Test point (Vertical input gate-2)	IG2V	Test point (Vertical input gate-2)	shorted to 0 V
23	IG1V	Test point (Vertical input gate-1)	IG1V	Test point (Vertical input gate-1)	shorted to 0 V
24	RG	Reset gate	RG	Reset gate	

*10: TG is an isolation gate between vertical register and horizontal resister.
In standard operation, the same pulse of P2V should be applied to the TG.

■Spectral response without window



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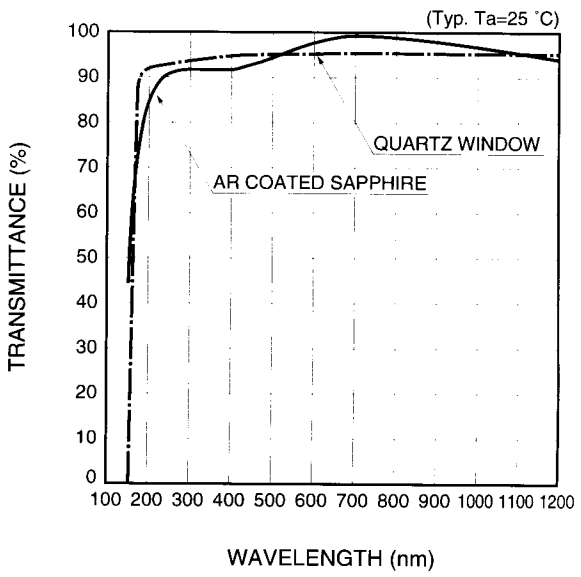
■Spectral transmittance characteristic of window material



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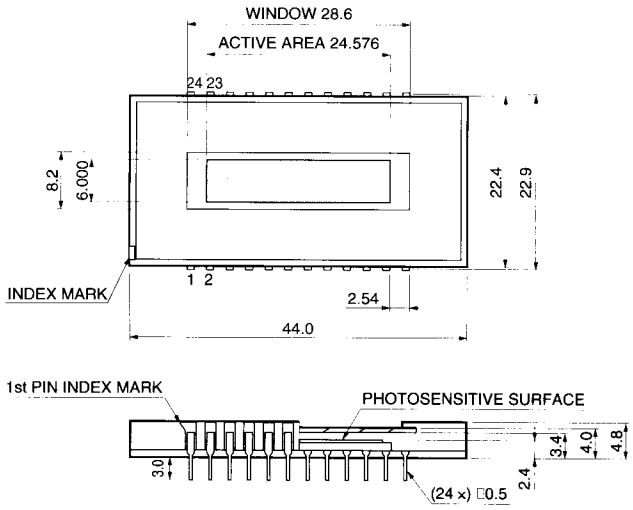
■Dimensional outlines (unit: mm)

S7960-1008



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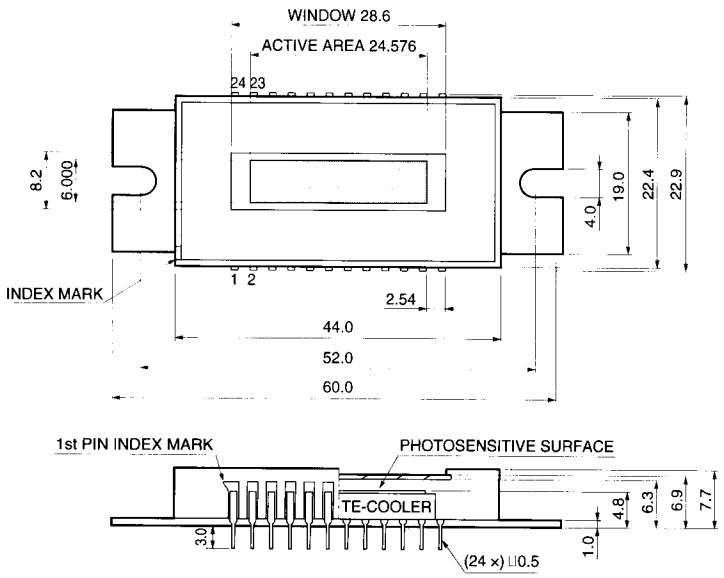

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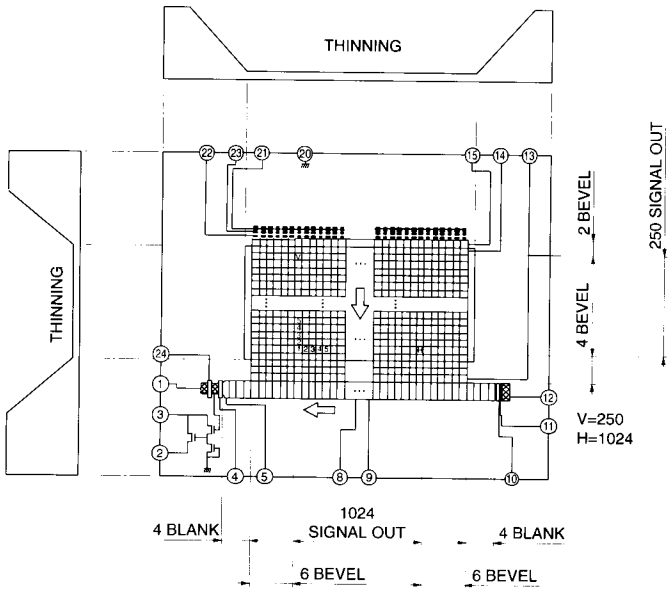
■Device structure, line output format



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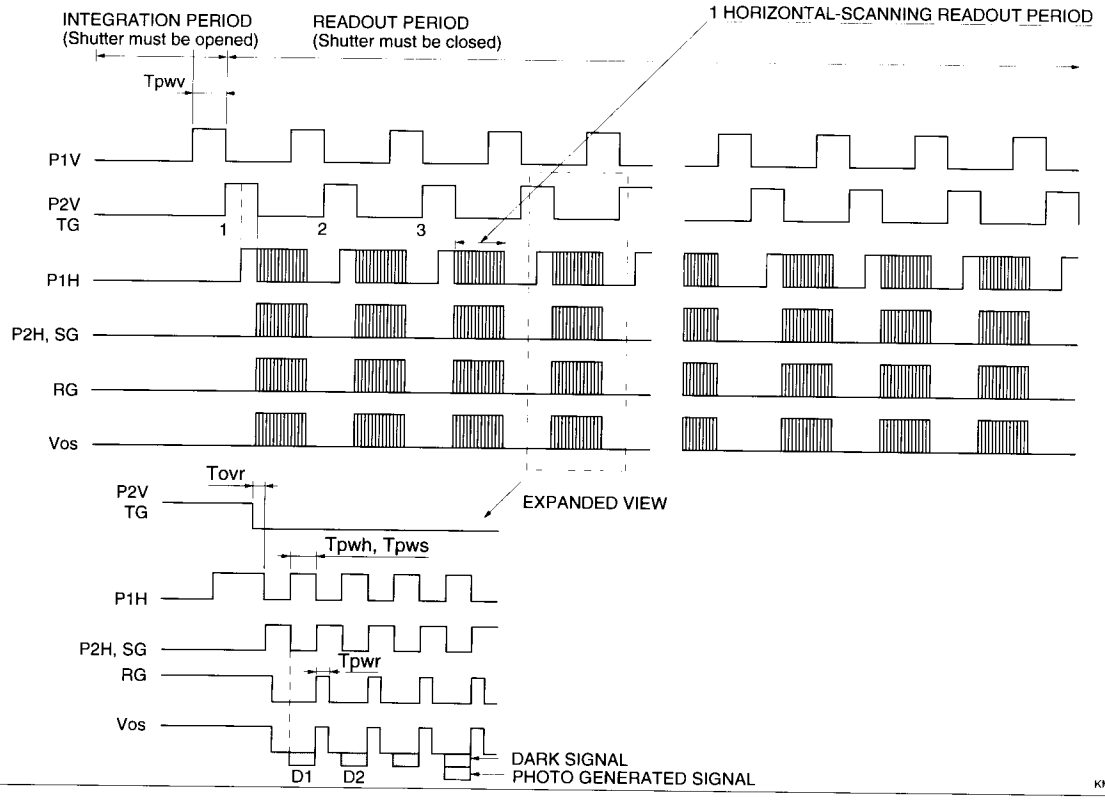
Pixel format

Left ← Horizontal direction → Right				
Blank	**Bevel**	**Effective**	**Bevel**	**Blank**
4	6	1024	6	4

Top ← Vertical direction → Bottom		
Bevel	**Effective**	**Bevel**
2	250	4

■Timing chart

●Area scanning 1 (low dark current mode)



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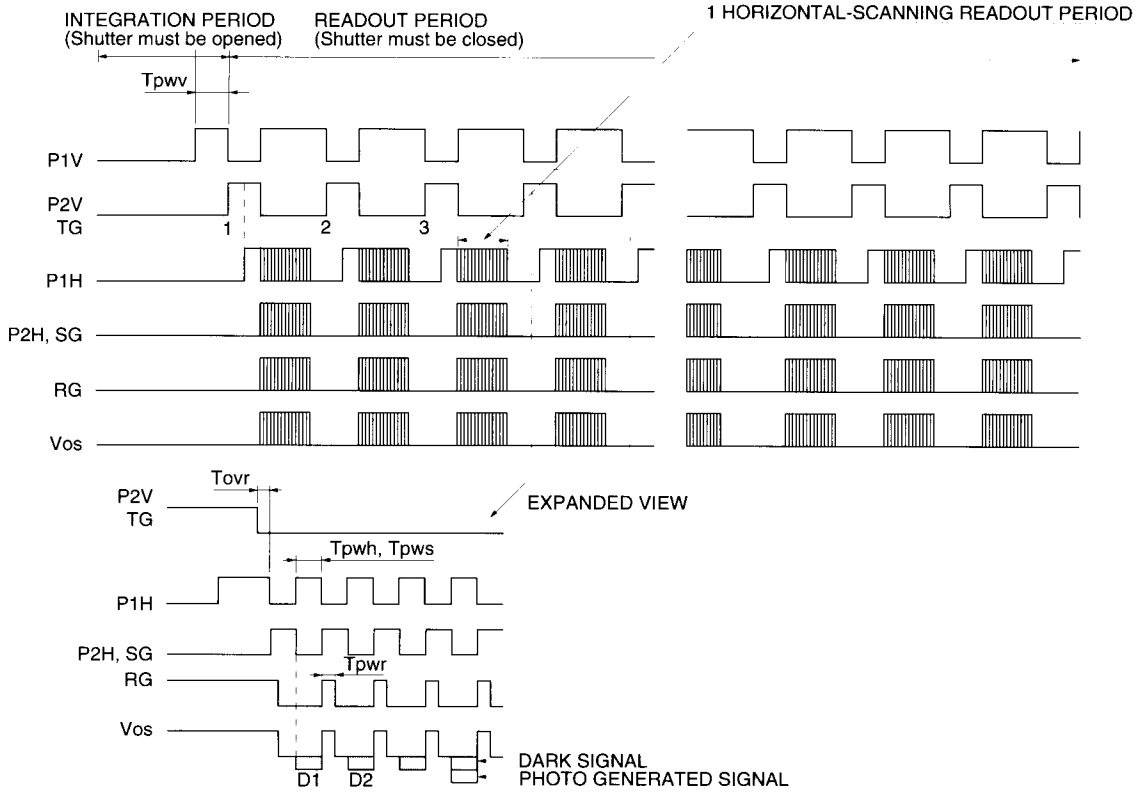
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	pulse width	Tpwv	*11	1	-	-	µs
	rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H	pulse width	Tpwh	*11	50	-	-	ns
	rise and fall time	Tprh, Tpfh		10	-	-	ns
	duty ratio	-		-	50	-	%
SG	pulse width	Tpws	-	50	-	-	ns
	rise and fall time	Tprs, Tpfs		10	-	-	ns
	duty ratio	-		-	50	-	%
RG	pulse width	Tpwr	-	15	-	-	ns
	rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	overlap time	Tovr	-	3	-	-	µs

*11: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■Area scanning 2 (large full well mode)



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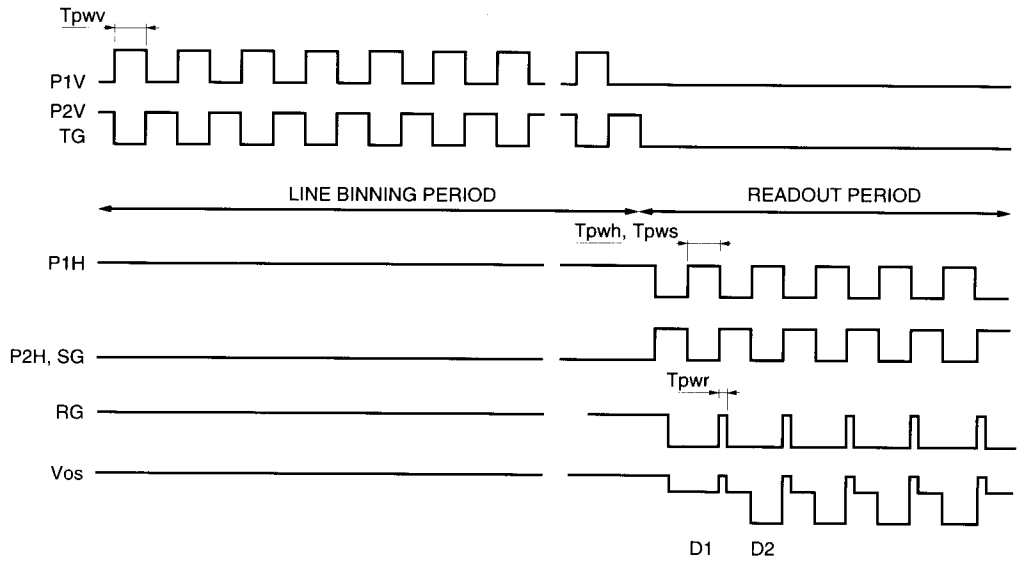
Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	pulse width	Tpwv	*12	1	-	-	µs
	rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H	pulse width	Tpwh	*12	50	-	-	ns
	rise and fall time	Tprh, Tpfh		10	-	-	ns
	duty ratio	-		-	50	-	%
SG	pulse width	Tpws	-	50	-	-	ns
	rise and fall time	Tprs, Tpfs		10	-	-	ns
	duty ratio	-		-	50	-	%
RG	pulse width	Tpwr	-	15	-	-	ns
	rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	overlap time	Tovr	-	3	-	-	µs

*12: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■Line binning



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Parameter		Symbol	Remark	Min.	Typ.	Max.	Unit
P1V, P2V, TG	pulse width	Tpwv	*13	1	-	-	µs
	rise and fall time	Tprv, Tpfv		20	-	-	ns
P1H, P2H	pulse width	Tpwh	*13	50	-	-	ns
	rise and fall time	Tprh, Tpfh		10	-	-	ns
	duty ratio	-		-	50	-	%
SG	pulse width	Tpws	-	50	-	-	ns
	rise and fall time	Tprs, Tpfs		10	-	-	ns
	duty ratio	-		-	50	-	%
RG	pulse width	Tpwr	-	15	-	-	ns
	rise and fall time	Tprr, Tpfr		5	-	-	ns
TG – P1H	overlap time	Tovr	-	3	-	-	µs

*13: Symmetrical pulses should be overlapped at 50 % of maximum amplitude.

■Specifications of built-in TE-cooler (S7961-1008)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Internal resistance	Rint	Ta=27 °C	-	0.7	-	Ω
Maximum current*14	Imax	Th*15=27 °C ΔT*16= ΔTmax	-	-	3.0	A
Maximum voltage	Vmax	Th*15=27 °C ΔT = ΔTmax I = Imax	-	-	2.7	V
Maximum heat absorption*17	Qmax	Tc*18=Th*15=27 °C I=Imax	-	-	5.0	W
Maximum temperature at hot side	-		-	-	70	°C
CCD temperature	-	Ta=25 °C	-	-10	0	°C

*14: If the current is greater than Imax, the heat absorption begins to decrease due to the Joule heat. It should be noted that this value is not a damage threshold. To protect the thermoelectric cooler (Peltier element) and maintain stable operation, the supply current should be less than 60 % of this maximum current.

*15: Temperature at hot side of thermoelectric cooler.

*16: ΔT = Th - Tc

*17: This is a theoretical heat absorption level that offsets the temperature difference in the Peltier element when the maximum current is supplied to the unit.

*18: Temperature at cool side of thermoelectric cooler.

■Specifications of built-in temperature sensor (S7961-1008)

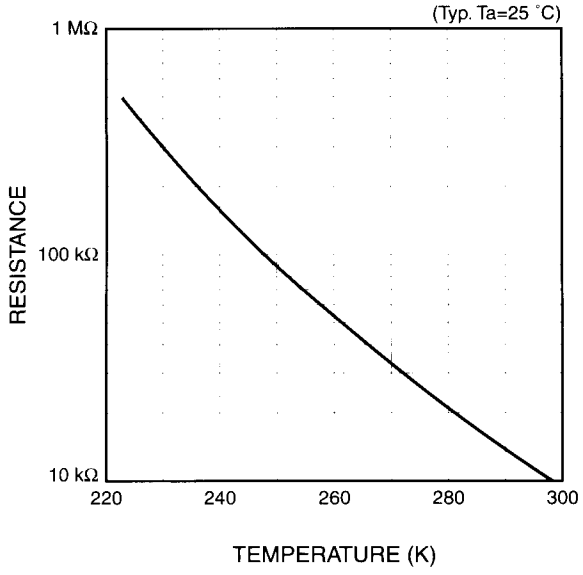
A chip thermistor is built in the same package with a CCD chip, and the CCD chip temperature can be monitored with it. A relation between the thermistor resistance and absolute temperature is expressed by the following equation.

$R1 = R2 \times \exp B\,(1 / T1 - 1 / T2)$

where R1 is the resistance at absolute temperature T1 (K)
R2 is the resistance at absolute temperature T2 (K)
B is so-called the B constant (K)

The characteristics of the thermistor used are as follows.

R (298K) = 10 kΩ
B (298K / 323K) = 3450 K



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■Precaution for use (Electrostatic countermeasures)

- Handle these sensors with bare hands or wearing cotton gloves. In addition, wear anti-static clothing or use a wrist band with an earth ring, in order to prevent electrostatic damage due to electrical charges from friction.
- Avoid directly placing these sensors on a work-desk or work-bench that may carry an electrostatic charge.
- Provide ground lines or ground connection with the work-floor, work-desk and work-bench to allow static electricity to discharge.
- Ground the tools used to handle these sensors, such as tweezers and soldering irons.

It is not always necessary to provide all the electrostatic measures stated above. Implement these measures according to the amount of damage that occurs.

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