



## N-Channel Reduced Qg, Fast Switching MOSFET

### Characteristics

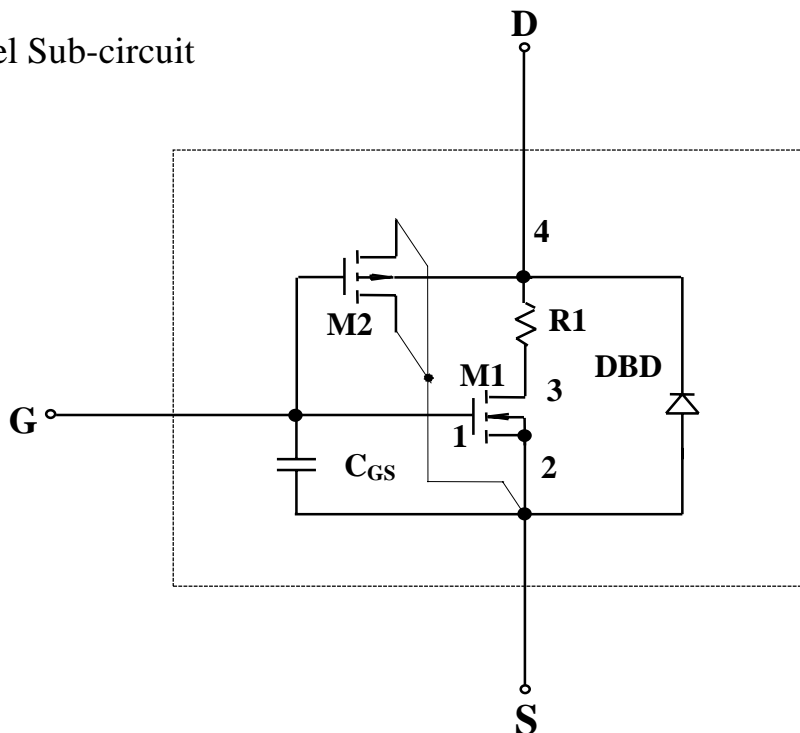
- N-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

### Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 10 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain

feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched  $C_{gd}$  model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

### Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



Model Evaluation

N-Channel Device ( $T_J=25^{\circ}\text{C}$  Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typical	Unit
<b>Static</b>				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	<b>1.73</b>	V
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{DS} \geq 5\text{V}, V_{GS} = 10\text{V}$	<b>508</b>	A
Drain-Source On-State Resistance <sup>a</sup>	$r_{DS(on)}$	$V_{GS} = 10\text{V}, I_D = 12\text{A}$	<b>0.0087</b>	$\Omega$
		$V_{GS} = 4.5\text{V}, I_D = 10\text{A}$	<b>0.0132</b>	
Forward Transconductance <sup>a</sup>	$g_{fs}$	$V_{DS} = 15\text{V}, I_D = 12\text{A}$	<b>34</b>	S
Diode Forward Voltage <sup>a</sup>	$V_{SD}$	$I_S = 2.3\text{A}, V_{GS} = 0\text{V}$	<b>0.74</b>	V
<b>Dynamic <sup>b</sup></b>				
Total Gate Charge	$Q_g$	$V_{DS} = 15\text{V}, V_{GS} = 5\text{V},$ $I_D = 12\text{A}$	<b>15.3</b>	nC
Gate-Source Charge	$Q_{gs}$		<b>5.8</b>	
Gate-Drain Charge	$Q_{gd}$		<b>4.8</b>	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 15\text{V}, R_L = 15\Omega$ $I_D \cong 1\text{A}, V_{GEN} = 10\text{V},$ $R_G = 6\Omega$	<b>10</b>	ns
Rise Time	$t_r$		<b>14</b>	
Turn-Off Delay Time	$t_{d(off)}$		<b>30</b>	
Fall Time	$t_f$		<b>52</b>	
Source-Drain Reverse Recovery Time	$t_{rr}$	$I_F = 2.3\text{A}, di/dt = 100\text{A}/\mu\text{s}$	<b>44</b>	

Notes:

- a) Pulse test: pulse width  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$
- b) Guaranteed by design, not subject to production testing



# SPICE Device Model SI4884DY

Comparison of Model with Measured Data  
( $T_J=25^\circ\text{C}$  Unless Otherwise Noted)

