



P-Channel 20-V (D-S) MOSFET

Characteristics

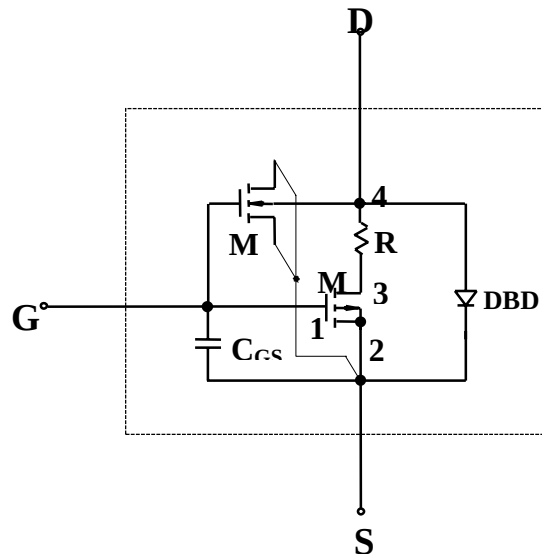
- P-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to -10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback

capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.



Model Evaluation

P-Channel Device ($T_J=25^{\circ}\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	0.87	V
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \leq -5\text{V}, V_{GS} = -4.5\text{V}$	82	A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -4.5\text{V}, I_D = -4.8\text{A}$	0.036	Ω
		$V_{GS} = -2.5\text{V}, I_D = -4.2\text{A}$	0.045	
		$V_{GS} = -1.8\text{V}, I_D = -1.0\text{A}$	0.058	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -10\text{V}, I_D = -4.8\text{A}$	16	S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.1\text{A}, V_{GS} = 0\text{V}$	0.80	V
Dynamic ^b				
Total Gate Charge	Q_g	$V_{DS} = -10\text{V},$ $V_{GS} = -4.5\text{V}, I_D = -4.8\text{A}$	14	nC
Gate-Source Charge	Q_{gs}		3.6	
Gate-Drain Charge	Q_{gd}		2.5	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -10\text{V}, R_L = 10\Omega$ $I_D \cong -1\text{A},$ $V_{GEN} = -4.5\text{V}, R_G = 6\Omega$	24	ns
Rise Time	t_r		27	
Turn-Off Delay Time	$t_{d(off)}$		87	
Fall Time	t_f		39	
Source-Drain Reverse Recovery Time	t_{rr}		35	

Notes:

- a) Pulse test; pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$
- c) Guaranteed by design, not subject to production testing



SPICE Device Model Si5433DC

Comparison of Model with Measured Data
($T_J=25^\circ\text{C}$ Unless Otherwise Noted)

