SPICE Device Model Si5513DC

Complementary 20-V (D-S) MOSFET

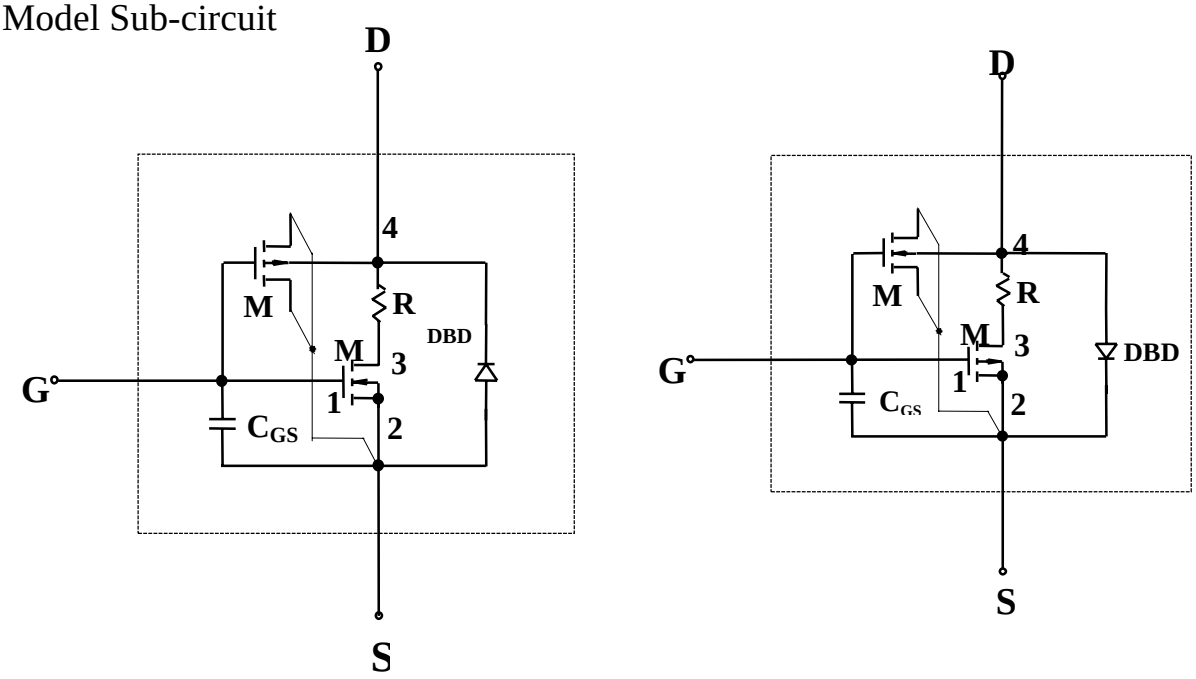
Characteristics

- N- and P- channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n- and p- channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 5 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitance network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation

N- and P- Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions		Typical	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250µA	**N-Ch**	**1.02**	V
		V_{DS} = V_{GS}, I_D = **-**250µA	**P-Ch**	**1.02**	
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} ≥ **5**V, V_{GS} = **4.5**V	**N-Ch**	**32**	A
		V_{DS} ≤ **-5**V, V_{GS} = **-4.5**V	**P-Ch**	**20**	
Drain-Source On-State Resistance [a]	$r_{DS(on)}$	V_{GS} = **4.5**V, I_D = **3.1**A	**N-Ch**	**0.065**	Ω
		V_{GS} = **-4.5**V, I_D = **-2.1**A	**P-Ch**	**0.133**	
		V_{GS} = **2.5**V, I_D = **2.3**A	**N-Ch**	**0.110**	
		V_{GS} = **-2.5**V, I_D = **-1.7**A	**P-Ch**	**0.216**	
Forward Transconductance [a]	g_{fs}	V_{DS} = **10**V, I_D = **3.1**A	**N-Ch**	**7**	S
		V_{DS} = **-10**V, I_D = **-2.1**A	**P-Ch**	**5**	
Diode Forward Voltage [a]	V_{SD}	I_S = **0.9**A, V_{GS} = 0V	**N-Ch**	**0.80**	V
		I_S = **-0.9**A, V_{GS} = 0V	**P-Ch**	**-0.80**	
Dynamic [b]					
Total Gate Charge	Q_g	N-Channel V_{DS} = **10**V, V_{GS} = **4.5**V , I_D = **3.1**A P-Channel V_{DS} = **-10**V, V_{GS} = **-4.5**V, I_D = **-2.1**A	**N-Ch**	**3.2**	nC
			P-Ch	**3**	
Gate-Source Charge	Q_{gs}		**N-Ch**	**0.60**	
			P-Ch	**0.90**	
Gate-Drain Charge	Q_{gd}		**N-Ch**	**1.3**	
			P-Ch	**0.60**	
Turn-On Delay Time	$t_{d(on)}$	N-Channel V_{DD} = **10**V, R_L = **10**Ω I_D ≅ **1**A, V_{GEN} = **4.5**V, R_G = 6Ω P-Channel V_{DD} = **-10**V, R_L = **10**Ω I_D ≅ **-1**A, V_{GEN} = **-4.5**V, R_G = 6Ω	**N-Ch**	**11**	µs
			P-Ch	**16**	
Rise Time	t_r		**N-Ch**	**14**	
			P-Ch	**19**	
Turn-Off Delay Time	$t_{d(off)}$		**N-Ch**	**16**	
			P-Ch	**22**	
Fall Time	t_f		**N-Ch**	**20**	
			P-Ch	**25**	
Source-Drain Reverse Recovery Time	t_r	I_F = **0.9**A, di/dt=100A/µs	**N-Ch**	**40**	ns
		I_F = **-0.9**A, di/dt=100A/µs	**P-Ch**	**36**	

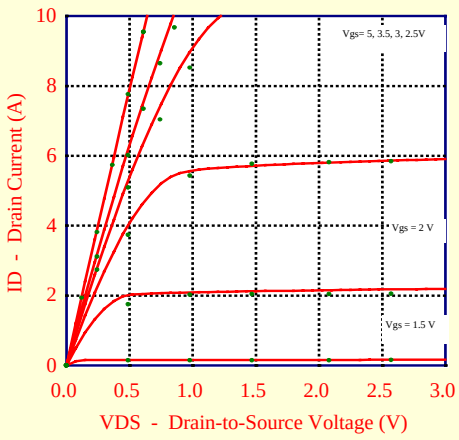
Notes:

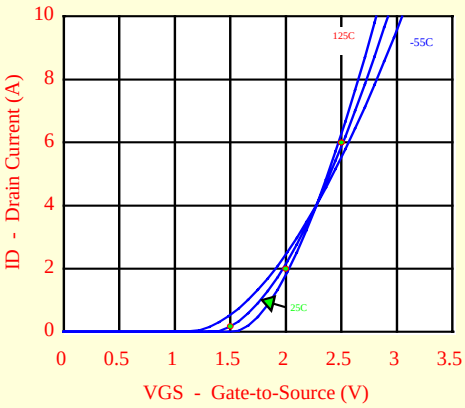
a) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%

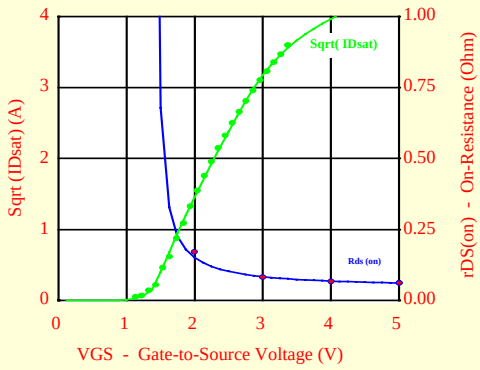
b) Guaranteed by design, not subject to production testing

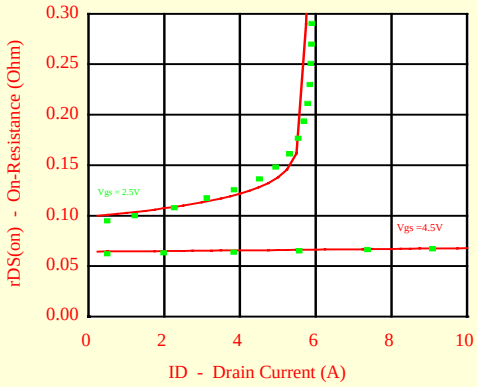
Comparison of Model with Measured Data N-Channel MOSFET

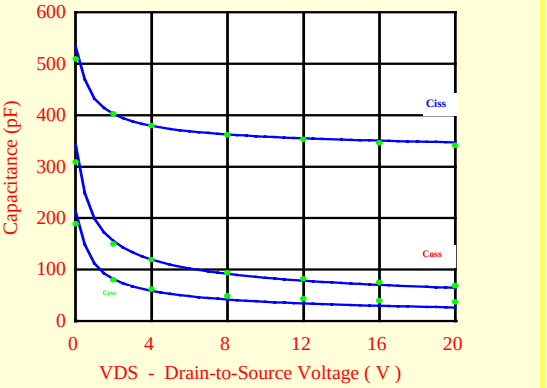
(T_J=25°C Unless Otherwise Noted)

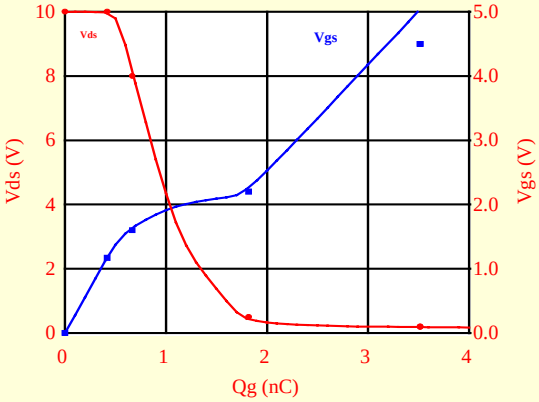


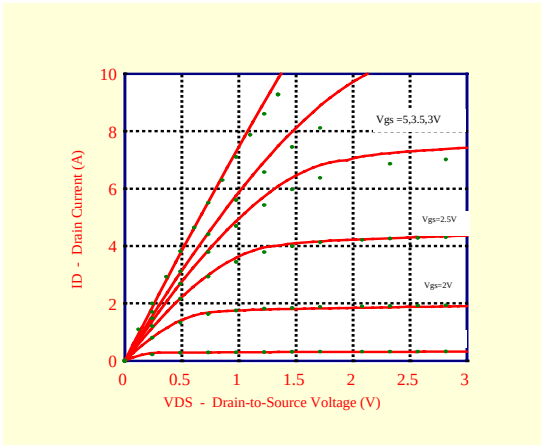


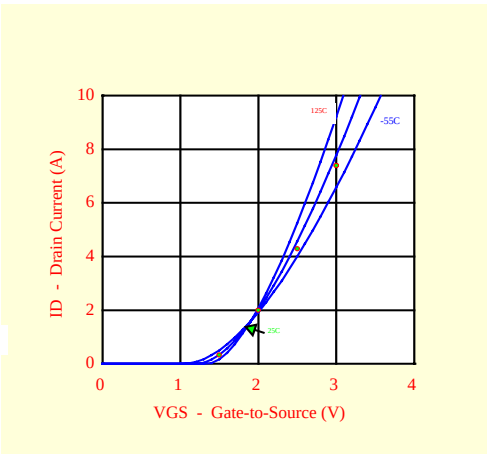


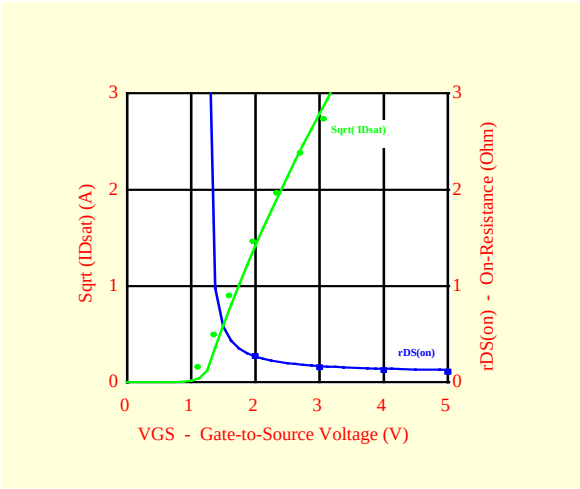


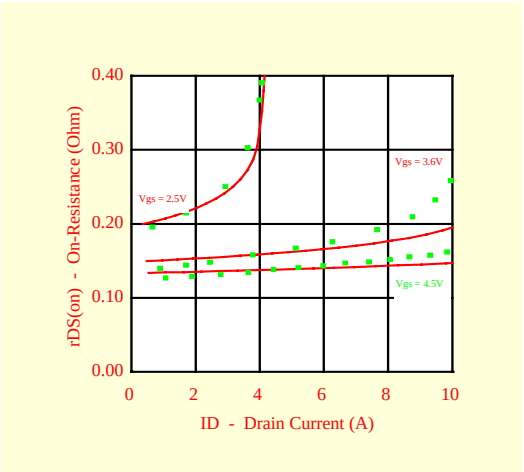


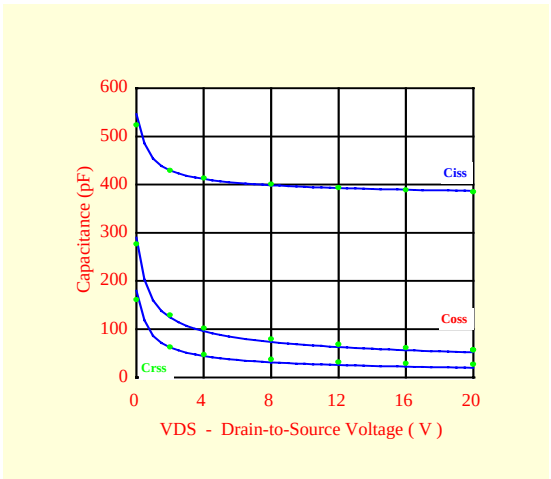


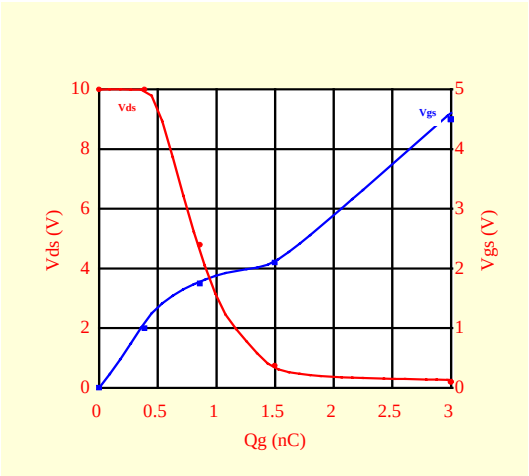

ID - Drain Current (A)
VDS - Drain-to-Source Voltage (V)
Vgs =5,3.5,3V
Vgs=2.5V
Vgs=2V


ID - Drain Current (A)
VGS - Gate-to-Source (V)
125C
-55C
25C


Sqrt (IDsat) (A)
rDS(on) - On-Resistance (Ohm)
VGS - Gate-to-Source Voltage (V)
Sqrt(IDsat)
rDS(on)


rDS(on) - On-Resistance (Ohm)
ID - Drain Current (A)
Vgs = 2.5V
Vgs = 3.6V
Vgs = 4.5V


Capacitance (pF)
VDS - Drain-to-Source Voltage (V)
Ciss
Coss
Crss


Vds (V)
Vgs (V)
Qg (nC)
Vds
Vgs