P-Channel 20-V (D-S) MOSFET with Copper Leadframe

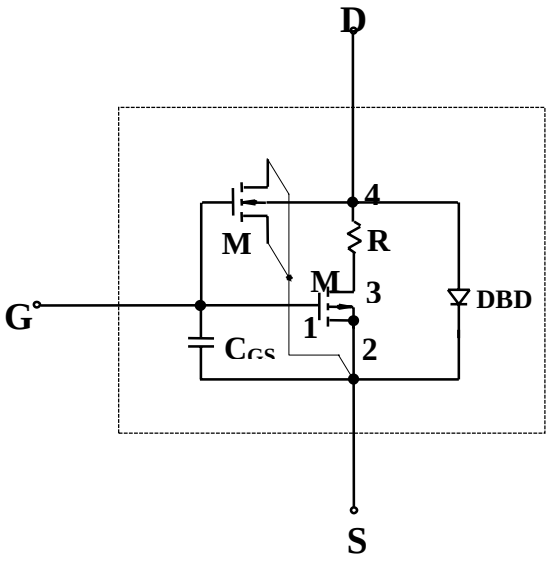
Characteristics

- P-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model was extracted and optimized over a -55°C to 125°C temperature range under pulse conditions for 0 to –5 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold voltage. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation

P-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -100µA	**0.80**		V
On-State Drain Current [a]	$I_{D(on)}$	V_{DS} = **-5**V, V_{GS} = **-4.5**V	**36**		A
Drain-Source On-State Resistance [a]	$r_{DS(on)}$	V_{GS} = **-4.5**V, I_D = **-2.9**A V_{GS} = **-2.5**V, I_D = **-2.4**A V_{GS} = **-1.8**V, I_D = **-1.0**A	**0.098** **0.132** **0.178**	0.095 0.125 0.180	Ω
Forward Transconductance [a]	g_{fs}	V_{DS} = **-10**V, I_D = **-2.9**A	**6.7**	6	S
Diode Forward Voltage [a]	V_{SD}	I_S = **-1.4**A, V_{GS} = 0V	**- 0.80**	- 0.80	V
Dynamic [b]					
Total Gate Charge	Q_g	V_{DS} = **-10**V, V_{GS} = **-4.5**V, I_D = **-2.9**A	**5.6**	5.6	nC
Gate-Source Charge	Q_{gs}		**1.2**	1.2	
Gate-Drain Charge	Q_{gd}		**1.2**	1.2	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = **-10**V, R_L = **10Ω** I_D ≅ **-1**A, V_{GEN} = **-4.5**V, R_G = 6Ω	**1.1**	0.75	ns
Rise Time	t_r		**2.9**	1.6	
Turn-Off Delay Time	$t_{d(off)}$		**9.3**	3.9	
Fall Time	t_f		**15**	3.9	

Notes:
a) Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%
b) Guaranteed by design, not subject to production testing

Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)