Dual P-Channel 12-V (D-S) MOSFET with Copper Leadframe

Characteristics

- P-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode

- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the p-channel vertical DMOS. The sub-circuit model was extracted and optimized over a -55°C to 125°C temperature range under pulse conditions for 0 to –5 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold voltage. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit
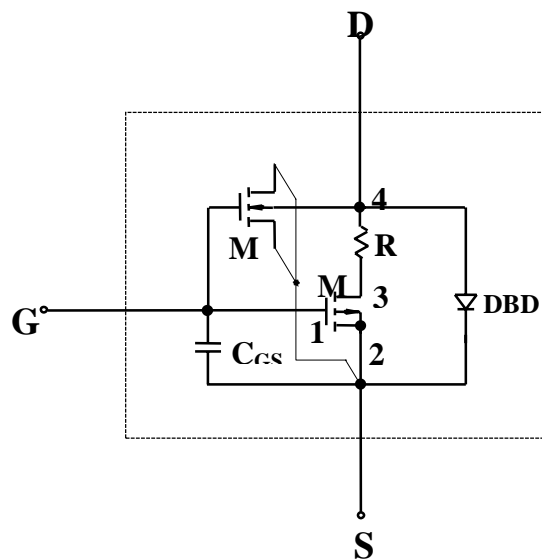
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation

P-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Simulated Data	Measured Data	Unit
Static					
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = -100\mu A$	**0.74**		V
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} = -5V$, $V_{GS} = -4.5V$	**9.2**		A
Drain-Source On-State Resistance [a]	$r_{DS(on)}$	$V_{GS} = -4.5V$, $I_D = -1.0A$	**0.302**	0.300	Ω
		$V_{GS} = -2.5V$, $I_D = -0.81A$	**0.498**	0.470	
		$V_{GS} = -1.8V$, $I_D = -0.20A$	**0.709**	0.660	
Forward Transconductance [a]	g_{fs}	$V_{DS} = -10V$, $I_D = -1.0A$	**1.71**	1.7	S
Diode Forward Voltage [a]	V_{SD}	$I_S = -0.47A$, $V_{GS} = 0V$	**- 0.80**	- 0.85	V
Dynamic [b]					
Total Gate Charge	Q_g	$V_{DS} = -6V$, $V_{GS} = -4.5V$, $I_D = -1.0A$	**1.2**	1.3	nC
Gate-Source Charge	Q_{gs}		**0.31**	0.31	
Gate-Drain Charge	Q_{gd}		**0.31**	0.31	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -6V$, $R_L = 12\Omega$ $I_D \cong -0.5A$, $V_{GEN} = -4.5V$, $R_G = 6\Omega$	**0.34**	0.17	ns
Rise Time	t_r		**1.0**	0.47	
Turn-Off Delay Time	$t_{d(off)}$		**2.5**	0.96	
Fall Time	t_f		**4.8**	1.0	

Notes:

a)   Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%

b)   Guaranteed by design, not subject to production testing

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Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)

Vgs=5,3.5,3V

Vgs=2.5V

Vgs=2V

Vgs=1.5V

ID - Drain Current (A)

VDS - Drain-to-Source Voltage (V)

125C

-55C

25C

ID - Drain Current (A)

VGS - Gate-to-Source Voltage (V)

Sqrt (IDsat)

Rds(on)

Sqrt (IDsat) (A)

Rds(on) - On-Resistance (Ohm)

VGS - Gate-to-Source Voltage (V)

Vgs = 1.8V

Vgs = 2.5V

Vgs = 4.5V

rDS(on) - On-Resistance (Ohm)

ID - Drain Current (A)

Ciss

Coss

Capacitance (pF)

VDS - Drain-to-Source Voltage (V)

Vds

Vgs

Vds (V)

Vgs (V)

Qg (nC)

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