N-Channel Reduced Qg, Fast Switching MOSFET

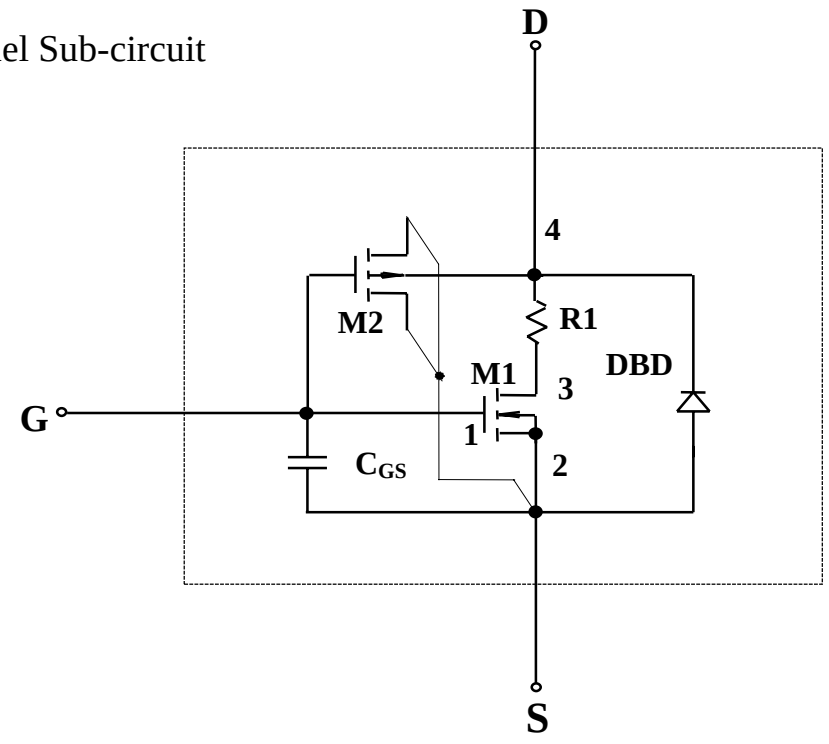
Characteristics

- N-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model was extracted and optimized over a 25°C to 125°C temperature range under pulse conditions for 0 to 10 volt gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation

N-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D= 250µA	**1.95**	V
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \geq$ **5**V, V_{GS} = **10**V	**248**	A
Drain-Source On-State Resistance [a]	$r_{DS(on)}$	V_{GS} = **10**V, I_D = **6**A V_{GS} = **10**V, I_D = **6**A, T_J = 125C V_{GS} = **10**V, I_D = **6**A, T_J = 175C V_{GS} = **4.5**V, I_D = **5.1**A	**0.017** **0.026** **0.032** **0.023**	Ω
Forward Transconductance [a]	g_{fs}	V_{DS} = **15**V, I_D = **6**A	**22**	S
Diode Forward Voltage [a]	V_{SD}	I_S = **1.7**A, V_{GS} = 0V	**0.80**	V
Dynamic [b]				
Total Gate Charge	Q_g	V_{DS} = **30**V, V_{GS} = **10**V, I_D = **6**A	**17.5**	nC
Gate-Source Charge	Q_{gs}		**3.4**	
Gate-Drain Charge	Q_{gd}		**5.3**	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = **30**V, R_L = **30Ω** $I_D \cong$ **1**A, V_{GEN} =**10**V, R_G = 6Ω	**22**	ns
Rise Time	t_r		**25**	
Turn-Off Delay Time	$t_{d(off)}$		**42**	
Fall Time	t_f		**48**	
Source-Drain Reverse Recovery Time	trr	I_F = **1.7**A di/dt = 100A/µs	**39**	

Notes:

a) Pulse test; pulse width ≤ 300 µsec, duty cycle ≤ 2%

b) Guaranteed by design, not subject to production testing

Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)