N-Channel 1.25-W, 2.5-V Rated MOSFET

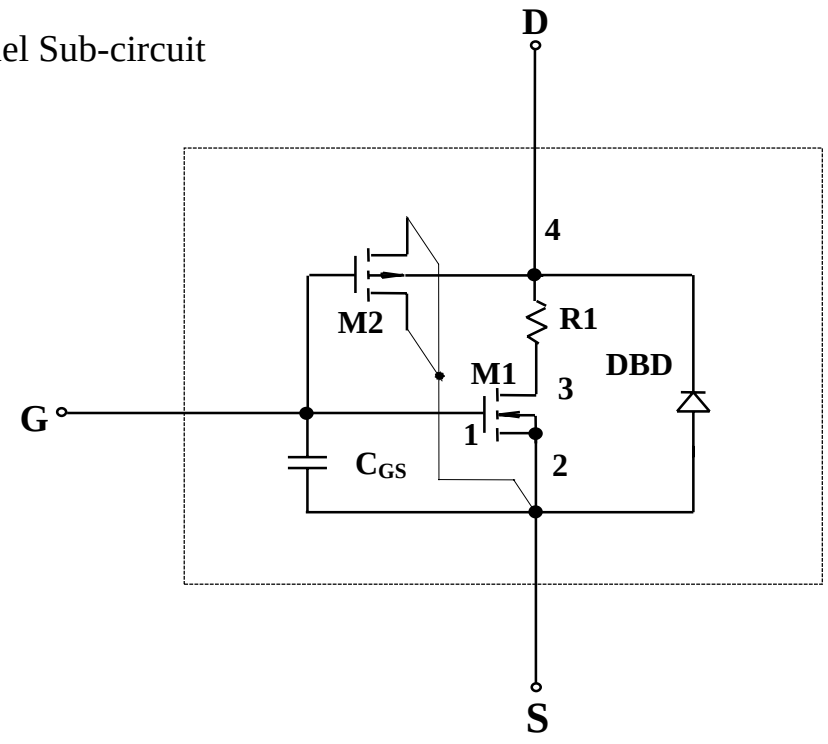
Characteristics

- N-channel Vertical DMOS
- Macro-Model (Sub-circuit)
- Level 3 MOS
- Applicable for Both Linear and Switch Mode
- Applicable Over a -55 to 125°C Temperature Range
- Models Gate Charge, Transient, and Diode Reverse Recovery Characteristics

Description

The attached SPICE Model describes typical electrical characteristics of the n-channel vertical DMOS. The sub-circuit model was extracted and optimized over 25°C to 125°C temperature range under pulse conditions for 0 to 10 volts gate drives. Saturated output impedance model accuracy has been maximized for gate biases near threshold. A novel gate-to-drain feedback capacitor network is used to model gate charge characteristics while avoiding convergence problems of switched C_{gd} model. Model parameter values are optimized to provide a best fit to measure electrical data and are not intended as an exact physical description of a device.

Model Sub-circuit



This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

Model Evaluation

N-Channel Device (T_J=25°C Unless Otherwise Noted)

Parameter	Symbol	Test Conditions	Typical	Unit
Static				
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D= 250µA	**0.91**	V
On-State Drain Current [b]	$I_{D(on)}$	V_{DS} ≥ **5**V, V_{GS} = **4.5**V	**62**	A
		V_{DS} ≥ **5**V, V_{GS} = **2.5**V	**16**	A
Drain-Source On-Resistance [b]	$r_{DS(on)}$	V_{GS} = **4.5**V, I_D = **3.6**A V_{GS} = **2.5**V, I_D = **3.1**A	**0.071** **0.081**	Ω
Forward Transconductance [b]	g_{fs}	V_{DS} = **5**V, I_D = **3.6**A	**11**	S
Diode Forward Voltage [b]	V_{SD}	I_S = **1.6**A, V_{GS} = 0V	**0.79**	V
Dynamic				
Total Gate Charge	Q_g	V_{DS} = **10**V, V_{GS} = **4.5**V, I_D = **3.6**A	**4.9**	nC
Gate-Source Charge	Q_{gs}		**0.65**	
Gate-Drain Charge	Q_{gd}		**1.60**	
Input Capacitance	C_{iss}	V_{DS} = **10**V, V_{GS} = **0**V, F= 1MHz	**336**	pF
Output Capacitance	C_{oss}		**113**	
Reverse Transfer Capacitance	C_{rss}		**40**	
Switching				
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = **10**V, R_L = **5.5**Ω I_D ≅ **3.6**A, V_{GEN} =**4.5**V, R_G = 6Ω	**8**	ns
Rise Time	t_r		**12**	
Turn-Off Delay Time	$t_{d(off)}$		**21**	
Fall Time	t_f		**30**	

Notes:
a) T_A = 25C unless otherwise noted
b) Pulse test; Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2%

Comparison of Model with Measured Data
(T_J=25°C Unless Otherwise Noted)