

# SDC8UL7284-(67/84/100/125)T-S

## 64MByte (8M x 72) CMOS

## Synchronous DRAM Module

### General Description

The SDC8UL7284-(67/84/100/125)T-S is a high performance, 64-megabyte synchronous, dynamic RAM module organized as 8M words by 72 bits, in a 168-pin, dual-in-line memory module (DIMM) package.

The module utilizes nine Fujitsu MB81164842A-(67/84/100/125)LFN CMOS 8Mx8 synchronous dynamic RAMs in surface mount package (TSOP) on an epoxy laminated substrate. Each device is accompanied by a decoupling capacitor for improved noise immunity.

A 256 Byte Serial EEPROM contains the module configuration information.

### Features

- High Density 64MByte
- Cycle Time: 8ns (125MHz), 10ns (100MHz), 12ns (84MHz), 15ns (67MHz)
- Low Power: Active 6.6W (125MHz), 5.8W (100MHz), 5.3W (84MHz), 4.9W (67MHz)
- LVTTTL-compatible inputs and outputs
- Separate power and ground planes to improve noise immunity
- Single power supply of 3.3V±0.3V
- Height: 1.250 inch

### ABSOLUTE MAXIMUM RATINGS

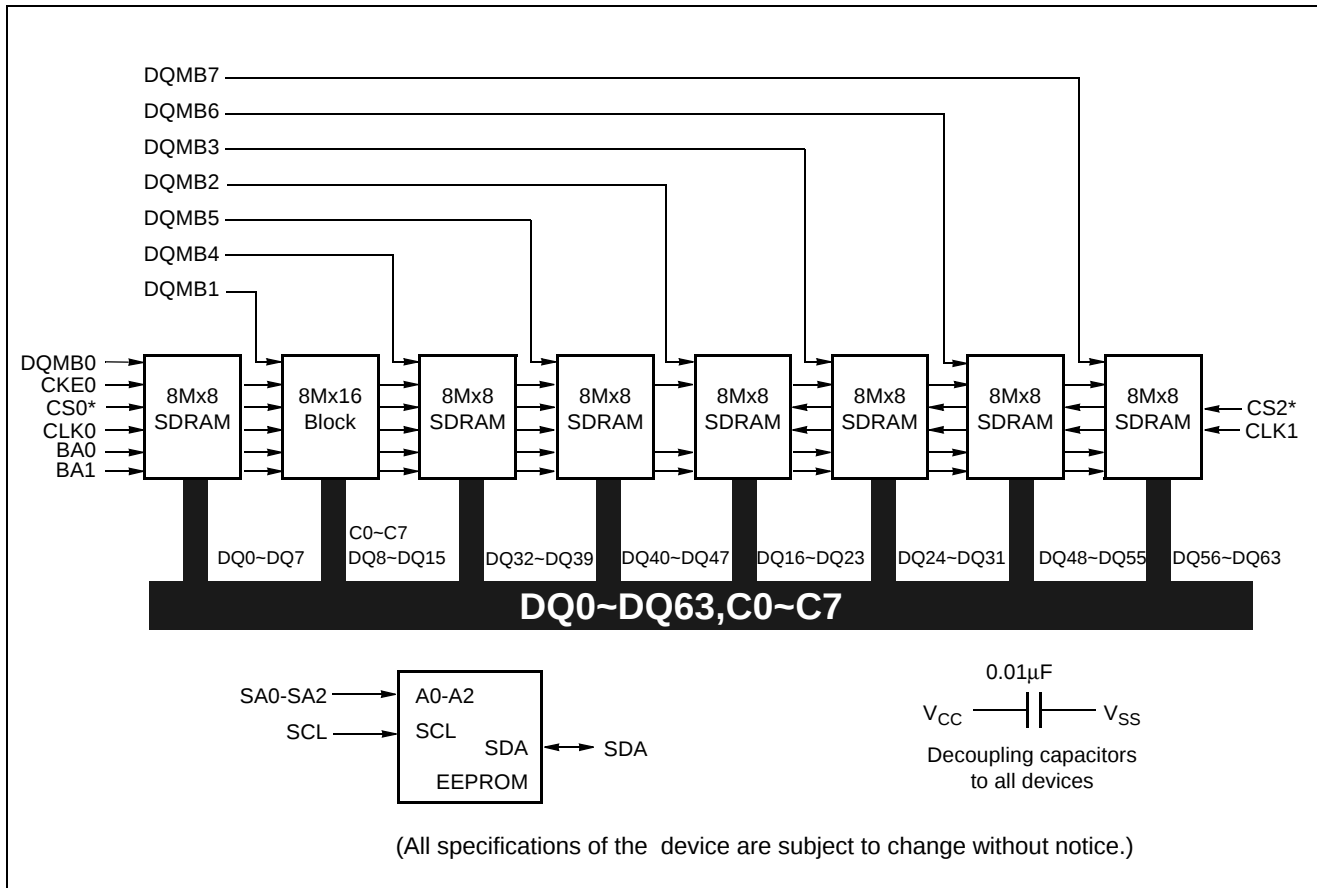
| Item                                           | Symbol           | Ratings      | Unit |
|------------------------------------------------|------------------|--------------|------|
| Voltage on any pin relative to V <sub>SS</sub> | V <sub>T</sub>   | -0.5 to +4.6 | V    |
| Power Dissipation                              | P <sub>T</sub>   | 9.0          | W    |
| Operating Temperature                          | T <sub>opr</sub> | 0 to +70     | °C   |
| Storage Temperature                            | T <sub>stg</sub> | -55 to +125  | °C   |
| Short Circuit Output Current                   | I <sub>OS</sub>  | ±50          | mA   |

### RECOMMENDED DC OPERATING CONDITIONS

(T<sub>A</sub> = 0 to +70 °C)

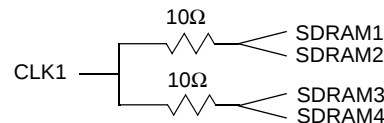
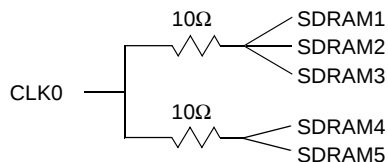
| Symbol          | Parameter          | Min  | Typ | Max                  | Unit |
|-----------------|--------------------|------|-----|----------------------|------|
| V <sub>CC</sub> | Supply Voltage     | 3.0  | 3.3 | 3.6                  | V    |
| V <sub>SS</sub> | Ground             | 0    | 0   | 0                    | V    |
| V <sub>IH</sub> | Input High voltage | 2.0  | -   | V <sub>CC</sub> +0.5 | V    |
| V <sub>IL</sub> | Input Low voltage  | -0.5 | -   | 0.8                  | V    |

### Functional Diagram

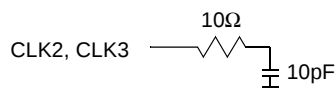


- Notes:
1. A0~A11 to all devices
  2. WE\*, RAS\*, CAS\* to all devices.
  3. Data and CLKs are terminated using 10 ohm series resistors.
  4. 8Mx16 block comprises two 8Mx8 SDRAM devices.
  5. DQMs vs. Data I/Os
    - DQMB0 controls DQ0~DQ7
    - DQMB1 controls DQ8~DQ15, C0~C7
    - DQMB2 controls DQ16~DQ23
    - DQMB3 controls DQ24~DQ31
    - DQMB4 controls DQ32~DQ39
    - DQMB5 controls DQ40~DQ47
    - DQMB6 controls DQ48~DQ55
    - DQMB7 controls DQ56~DQ63

#### 6. Clock Wiring



CLK1



## SDC8UL7284-(67/84/100/125)T-S

### Pin Name

|                 |                        |                 |                          |
|-----------------|------------------------|-----------------|--------------------------|
| A0~A11          | Addresses              | CS0*, CS2*      | Chip Select              |
| BA0, BA1        | Bank Select Address    | WE*             | Write Enable             |
| DQ0~DQ63, C0~C7 | Data Inputs/Outputs    | SA0~SA2         | Decode Input             |
| CLK0~CLK3       | Clock Inputs           | SCL             | Serial Clock             |
| RAS*            | Row Address Strobes    | SDA             | Serial Data Input/Output |
| CAS*            | Column Address Strobes | V <sub>CC</sub> | Power Supply             |
| CKE0            | Clock Enables          | V <sub>SS</sub> | Ground                   |
| DQMB0-DQMB7     | DQ Mask Enables        | NC              | No Connection            |

| Pin No. | Pin Designation | Pin No. | Pin Designation | Pin No. | Pin Designation | Pin No. | Pin Designation |
|---------|-----------------|---------|-----------------|---------|-----------------|---------|-----------------|
| 1       | V <sub>SS</sub> | 43      | V <sub>SS</sub> | 85      | V <sub>SS</sub> | 127     | V <sub>SS</sub> |
| 2       | DQ0             | 44      | NC              | 86      | DQ32            | 128     | CKE0            |
| 3       | DQ1             | 45      | CS2*            | 87      | DQ33            | 129     | NC              |
| 4       | DQ2             | 46      | DQMB2           | 88      | DQ34            | 130     | DQMB6           |
| 5       | DQ3             | 47      | DQMB3           | 89      | DQ35            | 131     | DQMB7           |
| 6       | V <sub>CC</sub> | 48      | NC              | 90      | V <sub>CC</sub> | 132     | NC              |
| 7       | DQ4             | 49      | V <sub>CC</sub> | 91      | DQ36            | 133     | V <sub>CC</sub> |
| 8       | DQ5             | 50      | NC              | 92      | DQ37            | 134     | NC              |
| 9       | DQ6             | 51      | NC              | 93      | DQ38            | 135     | NC              |
| 10      | DQ7             | 52      | C2              | 94      | DQ39            | 136     | C6              |
| 11      | DQ8             | 53      | C3              | 95      | DQ40            | 137     | C7              |
| 12      | V <sub>SS</sub> | 54      | V <sub>SS</sub> | 96      | V <sub>SS</sub> | 138     | V <sub>SS</sub> |
| 13      | DQ9             | 55      | DQ16            | 97      | DQ41            | 139     | DQ48            |
| 14      | DQ10            | 56      | DQ17            | 98      | DQ42            | 140     | DQ49            |
| 15      | DQ11            | 57      | DQ18            | 99      | DQ43            | 141     | DQ50            |
| 16      | DQ12            | 58      | DQ19            | 100     | DQ44            | 142     | DQ51            |
| 17      | DQ13            | 59      | V <sub>CC</sub> | 101     | DQ45            | 143     | V <sub>CC</sub> |
| 18      | V <sub>CC</sub> | 60      | DQ20            | 102     | V <sub>CC</sub> | 144     | DQ52            |
| 19      | DQ14            | 61      | NC              | 103     | DQ46            | 145     | NC              |
| 20      | DQ15            | 62      | NC              | 104     | DQ47            | 146     | NC              |
| 21      | C0              | 63      | NC              | 105     | C4              | 147     | NC              |
| 22      | C1              | 64      | V <sub>SS</sub> | 106     | C5              | 148     | V <sub>SS</sub> |
| 23      | V <sub>SS</sub> | 65      | DQ21            | 107     | V <sub>SS</sub> | 149     | DQ53            |
| 24      | NC              | 66      | DQ22            | 108     | NC              | 150     | DQ54            |
| 25      | NC              | 67      | DQ23            | 109     | NC              | 151     | DQ55            |
| 26      | V <sub>CC</sub> | 68      | V <sub>SS</sub> | 110     | V <sub>CC</sub> | 152     | V <sub>SS</sub> |
| 27      | WE*             | 69      | DQ24            | 111     | CAS*            | 153     | DQ56            |
| 28      | DQMB0           | 70      | DQ25            | 112     | DQMB4           | 154     | DQ57            |
| 29      | DQMB1           | 71      | DQ26            | 113     | DQMB5           | 155     | DQ58            |
| 30      | CS0*            | 72      | DQ27            | 114     | NC              | 156     | DQ59            |
| 31      | NC              | 73      | V <sub>CC</sub> | 115     | RAS*            | 157     | V <sub>CC</sub> |
| 32      | V <sub>SS</sub> | 74      | DQ28            | 116     | V <sub>SS</sub> | 158     | DQ60            |
| 33      | A0              | 75      | DQ29            | 117     | A1              | 159     | DQ61            |
| 34      | A2              | 76      | DQ30            | 118     | A3              | 160     | DQ62            |
| 35      | A4              | 77      | DQ31            | 119     | A5              | 161     | DQ63            |
| 36      | A6              | 78      | V <sub>SS</sub> | 120     | A7              | 162     | V <sub>SS</sub> |
| 37      | A8              | 79      | CLK2            | 121     | A9              | 163     | CLK3            |
| 38      | A10 / AP (Note) | 80      | NC              | 122     | BA0 (Note)      | 164     | NC              |
| 39      | BA1 (Note)      | 81      | NC              | 123     | A11             | 165     | SA0             |
| 40      | V <sub>CC</sub> | 82      | SDA             | 124     | V <sub>CC</sub> | 166     | SA1             |
| 41      | V <sub>CC</sub> | 83      | SCL             | 125     | CLK1            | 167     | SA2             |
| 42      | CLK0            | 84      | V <sub>CC</sub> | 126     | NC              | 168     | V <sub>CC</sub> |

Note : 1. Address A10 / AP : Initiates Auto Precharge  
2. Address BA0,BA1 : Bank select within the SDRAM devices

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## SERIAL PD INFORMATION

| Byte# | Function Described                                            | Function Supported              |         |        |        | Hex Value         |         |        |        |
|-------|---------------------------------------------------------------|---------------------------------|---------|--------|--------|-------------------|---------|--------|--------|
|       |                                                               | 125 Mhz                         | 100 Mhz | 84 Mhz | 67 Mhz | 125 Mhz           | 100 Mhz | 84 Mhz | 67 Mhz |
| 0     | # Bytes Written into serial memory at module mfr              | 128 bytes                       |         |        |        | 80h               |         |        |        |
| 1     | Total # bytes of SPD memory device                            | 256 bytes                       |         |        |        | 08h               |         |        |        |
| 2     | Fundamental memory type                                       | SDRAM                           |         |        |        | 04h               |         |        |        |
| 3     | # Row Address on this assembly                                | 12                              |         |        |        | 0Ch               |         |        |        |
| 4     | # Column Addresses on this assembly                           | 9                               |         |        |        | 09h               |         |        |        |
| 5     | # Module Banks on this assembly                               | 1                               |         |        |        | 01h               |         |        |        |
| 6     | Data Width of this assembly                                   | x72                             |         |        |        | 48h               |         |        |        |
| 7     | Data Width of this assembly (continued)                       |                                 |         |        |        | 00h               |         |        |        |
| 8     | Voltage interface standard of this assembly                   | LVTTTL                          |         |        |        | 01h               |         |        |        |
| 9     | SDRAM cycle time at CL=3 (tCLK)                               | 8ns                             | 10ns    | 12ns   | 15ns   | 80h               | A0h     | C0h    | F0h    |
| 10    | SDRAM Access from Clock at CL=3 (tAC)                         | 7.5ns                           | 8.5ns   | 8.5ns  | 9.0ns  | 75h               | 85h     | 85h    | 90h    |
| 11    | DIMM configuration type                                       | ECC                             |         |        |        | 02h               |         |        |        |
| 12    | Refresh Rate/Type                                             | S/R, Normal 15.6 ms             |         |        |        | 80h               |         |        |        |
| 13    | SDRAM Width Primary DRAM                                      | x8                              |         |        |        | 08h               |         |        |        |
| 14    | ECC SDRAM Data Width                                          | x8                              |         |        |        | 08h               |         |        |        |
| 15    | Min. clock delay, Back to Back Random Column Addresses (ICCD) | 1CLK                            |         |        |        | 01h               |         |        |        |
| 16    | Burst Length Supported                                        | 1, 2, 4, 8 & Full Page          |         |        |        | 8Fh               |         |        |        |
| 17    | # Banks on each SDRAM device                                  | 4                               |         |        |        | 04h               |         |        |        |
| 18    | CAS# Latency                                                  | 2, 3                            |         |        |        | 06h               |         |        |        |
| 19    | CS# Latency                                                   | 0                               |         |        |        | 01h               |         |        |        |
| 20    | Write Latency                                                 | 0                               |         |        |        | 01h               |         |        |        |
| 21    | SDRAM Module Attribute                                        | Non-Buffered/Registered,Non-PLL |         |        |        | 00h               |         |        |        |
| 22    | SDRAM Device Attribute                                        | Vcc +/-10%, B/R, S/W, P/A, A/P  |         |        |        | 0Eh               |         |        |        |
| 23    | Min Clock cycle Time at CL=2 (tCLK)                           | 12ns                            | 15ns    | 17ns   | 20ns   | C0h               | F0h     | 20h    | 50h    |
| 24    | Max. Data Access Time from clock at CL=2 (tAC)                | 9.0ns                           | 9.0ns   | 10ns   | 10ns   | 90h               | 90h     | A0h    | A0h    |
| 25    | Min Clock cycle Time at CL=1 (tCLK)                           | N/A                             |         |        |        | FFh               |         |        |        |
| 26    | Max. Data Access Time from clock at CL=1 (tAC)                | N/A                             |         |        |        | FFh               |         |        |        |
| 27    | Min. Row Precharge Time (tRP)                                 | 29ns                            | 30ns    | 35ns   | 40ns   | 1Dh               | 1Eh     | 23h    | 28h    |
| 28    | Min. Row Active Delay (tRRD)                                  | 16ns                            | 20ns    | 20ns   | 20ns   | 10h               | 14h     | 14h    | 14h    |
| 29    | Min. RAS to CAS Delay (tRCD)                                  | 24ns                            | 30ns    | 30ns   | 30ns   | 18h               | 1Eh     | 1Eh    | 1Eh    |
| 30    | Min. RAS Pulse Width (tRAS)                                   | 48ns                            | 60ns    | 65ns   | 70ns   | 30h               | 3Ch     | 41h    | 46h    |
| 31    | Module Bank Density                                           | 64MB                            |         |        |        | 10h               |         |        |        |
| 32-61 | Superset Information                                          |                                 |         |        |        | FFh               |         |        |        |
| 62    | SPD Revision                                                  | Rev. 1                          |         |        |        | 01h               |         |        |        |
| 63    | Checksum for bytes 0-62                                       | JEDEC Calculation               |         |        |        | JEDEC Calculation |         |        |        |

## SDC8UL7284-(67/84/100/125)T-S

### SERIAL PD INFORMATION (CONTINUED)

| Byte#   | Function Described                       | Function Supported |         |        |        | Hex Value         |         |        |        |
|---------|------------------------------------------|--------------------|---------|--------|--------|-------------------|---------|--------|--------|
|         |                                          | 125 Mhz            | 100 Mhz | 84 Mhz | 67 Mhz | 125 Mhz           | 100 Mhz | 84 Mhz | 67 Mhz |
| 64      | Manufacturers JEDEC ID code per JEP-106E | Continuation code  |         |        |        | 7Fh               |         |        |        |
| 65      | Manufacturers JEDEC ID code per JEP-106E | SMART's ID         |         |        |        | 94h               |         |        |        |
| 66-71   | Manufacturers JEDEC ID code per JEP-106E | None               |         |        |        | FFh               |         |        |        |
| 72      | Manufacturing location                   | Mfr Specific Data  |         |        |        |                   |         |        |        |
| 73      | Manufacturer's Part Number               | S                  |         |        |        | 53h               |         |        |        |
| 74      | Manufacturer's Part Number               | D                  |         |        |        | 44h               |         |        |        |
| 75      | Manufacturer's Part Number               | C                  |         |        |        | 43h               |         |        |        |
| 76      | Manufacturer's Part Number               | 8                  |         |        |        | 38h               |         |        |        |
| 77      | Manufacturer's Part Number               | U                  |         |        |        | 55h               |         |        |        |
| 78      | Manufacturer's Part Number               | L                  |         |        |        | 4Ch               |         |        |        |
| 79      | Manufacturer's Part Number               | 7                  |         |        |        | 37h               |         |        |        |
| 80      | Manufacturer's Part Number               | 2                  |         |        |        | 32h               |         |        |        |
| 81      | Manufacturer's Part Number               | 8                  |         |        |        | 38h               |         |        |        |
| 82      | Manufacturer's Part Number               | 4                  |         |        |        | 34h               |         |        |        |
| 83      | Manufacturer's Part Number               | 1                  | 1       | 8      | 6      | 31h               | 31h     | 38h    | 36h    |
| 84      | Manufacturer's Part Number               | 2                  | 0       | 4      | 7      | 32h               | 30h     | 34h    | 37h    |
| 85      | Manufacturer's Part Number               | 5                  | 0       | T      | T      | 35h               | 30h     | 54h    | 54h    |
| 86      | Manufacturer's Part Number               | T                  | T       | S      | S      | 54h               | 54h     | 53h    | 53h    |
| 87      | Manufacturer's Part Number               | S                  | S       | None   | None   | 53h               | 53h     | FFh    | FFh    |
| 88      | Manufacturer's Part Number               | None               |         |        |        | FFh               |         |        |        |
| 89      | Manufacturer's Part Number               | None               |         |        |        | FFh               |         |        |        |
| 90      | Manufacturer's Part Number               | None               |         |        |        | FFh               |         |        |        |
| 91      | Revision Code                            | Mfr Specific Data  |         |        |        | Mfr Specific Data |         |        |        |
| 92      | Revision Code                            | None               |         |        |        | FFh               |         |        |        |
| 93      | Manufacturing Date                       | DATE               |         |        |        | DATE              |         |        |        |
| 94      | Manufacturing Date                       | DATE               |         |        |        | DATE              |         |        |        |
| 95-98   | Assembly Serial Number                   | Serial Number      |         |        |        | S.No.             |         |        |        |
| 99      | Manufacturer Specific Data               | S                  |         |        |        | 53h               |         |        |        |
| 100     | Manufacturer Specific Data               | M                  |         |        |        | 4Dh               |         |        |        |
| 101     | Manufacturer Specific Data               | A                  |         |        |        | 41h               |         |        |        |
| 102     | Manufacturer Specific Data               | R                  |         |        |        | 52h               |         |        |        |
| 103     | Manufacturer Specific Data               | T                  |         |        |        | 54h               |         |        |        |
| 104     | Manufacturer Specific Data               | M                  |         |        |        | 4Dh               |         |        |        |
| 105     | Manufacturer Specific Data               | o                  |         |        |        | 6Fh               |         |        |        |
| 106     | Manufacturer Specific Data               | d                  |         |        |        | 64h               |         |        |        |
| 107     | Manufacturer Specific Data               | u                  |         |        |        | 75h               |         |        |        |
| 108     | Manufacturer Specific Data               | l                  |         |        |        | 6Ch               |         |        |        |
| 109     | Manufacturer Specific Data               | a                  |         |        |        | 61h               |         |        |        |
| 110     | Manufacturer Specific Data               | r                  |         |        |        | 72h               |         |        |        |
| 111     | Manufacturer Specific Data               | T                  |         |        |        | 54h               |         |        |        |
| 112     | Manufacturer Specific Data               | e                  |         |        |        | 65h               |         |        |        |
| 113     | Manufacturer Specific Data               | c                  |         |        |        | 63h               |         |        |        |
| 114     | Manufacturer Specific Data               | h                  |         |        |        | 68h               |         |        |        |
| 115     | Manufacturer Specific Data               | n                  |         |        |        | 6Eh               |         |        |        |
| 116     | Manufacturer Specific Data               | o                  |         |        |        | 6Fh               |         |        |        |
| 117     | Manufacturer Specific Data               | l                  |         |        |        | 6Ch               |         |        |        |
| 118     | Manufacturer Specific Data               | o                  |         |        |        | 6Fh               |         |        |        |
| 119     | Manufacturer Specific Data               | g                  |         |        |        | 67h               |         |        |        |
| 120     | Manufacturer Specific Data               | i                  |         |        |        | 69h               |         |        |        |
| 121     | Manufacturer Specific Data               | e                  |         |        |        | 65h               |         |        |        |
| 122     | Manufacturer Specific Data               | s                  |         |        |        | 73h               |         |        |        |
| 123     | Manufacturer Specific Data               | None               |         |        |        | FFh               |         |        |        |
| 124     | Manufacturer Specific Data               | None               |         |        |        | FFh               |         |        |        |
| 125     | Manufacturer Specific Data               | None               |         |        |        | FFh               |         |        |        |
| 126 (*) | INTEL specification frequency            | 66 Mhz             |         |        |        | 66h               |         |        |        |
| 127 (*) | INTEL specification CAS# Latency Support | 2,3                |         |        |        | 06h               |         |        |        |
| 128-255 | Open for CPQ Use for Read & Write        | None               |         |        |        | FFh               |         |        |        |

(\*) INTEL specification extension: These bytes are required for compatibility with previously released systems.

# SDC8UL7284-(67/84/100/125)T-S

## DC CHARACTERISTICS

( $V_{CC} = 3.3V \pm 0.3V$ ,  $V_{SS} = 0V$ ,  $T_A = 0$  to  $+70^\circ C$ )

| Parameter                 | Symbol    | Test Condition                                                             | 125  |      | 100  |      | 84   |      | 67   |      | Unit    | Note |
|---------------------------|-----------|----------------------------------------------------------------------------|------|------|------|------|------|------|------|------|---------|------|
|                           |           |                                                                            | Min. | Max. | Min. | Max. | Min. | Max. | Min. | Max. |         |      |
| Operating Current         | $I_{CC1}$ | No Burst, $t_{CK} = \min.$<br>$t_{RC} = \min.$                             | -    | 810  | -    | 720  | -    | 675  | -    | 630  | mA      | 1, 2 |
|                           |           | No Burst, $t_{CK} = \min.$ ,<br>$t_{RC} = \min.$<br>All Banks Active       | -    | 1440 | -    | 1260 | -    | 1170 | -    | 1080 | mA      | 1, 2 |
| Precharge Standby Current | $I_{CC2}$ | CKE - $V_{IL}$ , $t_{CK} = \min.$<br>All Banks Idle                        | -    | 9    | -    | 9    | -    | 9    | -    | 9    | mA      | 1, 2 |
|                           |           | CKE = $V_{IH}$ , $t_{CK} = \min.$<br>All Banks Idle                        | -    | 180  | -    | 180  | -    | 180  | -    | 180  | mA      | 1.2  |
| Active Standby Current    | $I_{CC3}$ | CKE = $V_{IL}$ , $t_{CK} = \min.$<br>Any Bank Active                       | -    | 27   | -    | 27   | -    | 27   | -    | 27   | mA      | 1, 2 |
|                           |           | CKE = $V_{IH}$ , $t_{CK} = \min.$<br>Any Bank Active                       | -    | 225  | -    | 225  | -    | 225  | -    | 225  | mA      | 1, 2 |
| Burst Mode Current        | $I_{CC4}$ | $t_{CK} = \min.$                                                           | -    | 1620 | -    | 1350 | -    | 1170 | -    | 960  | mA      | 1, 2 |
| Refresh Current           | $I_{CC5}$ | $t_{CK} = \min.$ , $t_{RC} = \min.$ ,<br>$t_{RRD} = \min.$<br>Auto Refresh | -    | 1845 | -    | 1620 | -    | 1485 | -    | 1350 | mA      | 1, 2 |
| Self Refresh Current      | $I_{CC6}$ | CKE - $V_{IL}$                                                             | -    | 4.5  | -    | 4.5  | -    | 4.5  | -    | 4.5  | mA      | 1, 2 |
| Input Leakage             | $I_{LI}$  | $0V \leq V_{in} \leq V_{CC}$                                               | -90  | 90   | -90  | 90   | -90  | 90   | -90  | 90   | $\mu A$ |      |
| Output Leakage Current    | $I_{LO}$  | $0V \leq V_{out} \leq V_{CC}$<br>$D_{out} = \text{Disable}$                | -10  | 10   | -10  | 10   | -10  | 10   | -10  | 10   | $\mu A$ |      |
| Output High Voltage       | $V_{OH}$  | High $I_{out} = -2mA$                                                      | 2.4  | -    | 2.4  | -    | 2.4  | -    | 2.4  | -    | V       |      |
| Output Low Voltage        | $V_{OL}$  | Low $I_{out} = 2 mA$                                                       | -    | 0.4  | -    | 0.4  | -    | 0.4  | -    | 0.4  | V       |      |

$\dagger CL = CAS^*$  Latency

- Notes:
- $I_{CC}$  depends on output load condition when the device is selected  $I_{CC} (\max.)$  is specified at the output open condition.
  - An initial pulse of 200 $\mu s$  is required after power-up followed by a minimum of eight Auto-Refresh-Cycles.

## CAPACITANCE

( $T_A = +25^\circ C$ ,  $V_{CC} = 3.3V \pm 0.3V$ )

| Parameter                                          | Symbol    | Max. | Unit | Note |
|----------------------------------------------------|-----------|------|------|------|
| Input Capacitance (Address, WE*, CKE0, RAS*, CAS*) | $C_{I1}$  | 50   | pF   | 1    |
| Input Capacitance (DQMB0,DQMB2-DQMB7)              | $C_{I2}$  | 13   | pF   | 1    |
| Input Capacitance (DQMB1)                          | $C_{I3}$  | 15   | pF   | 1    |
| Input Capacitance (CS0*,CLK0)                      | $C_{I4}$  | 30   | pF   | 1    |
| Input Capacitance (CS2*,CLK1)                      | $C_{I5}$  | 25   | pF   | 1    |
| Input Capacitance (CLK2,CLK3)                      | $C_{I6}$  | 15   | pF   | 1    |
| Input/Output Capacitance (DQ0-DQ63)                | $C_{I/O}$ | 12   | pF   | 1, 2 |

- Notes:
- Capacitance is measured with Boonton Meter or effective capacitance method.
  - CAS\* -  $V_{IH}$  to disable  $D_{out}$ .

## SDC8UL7284-(67/84/100/125)T-S

### AC CHARACTERISTICS

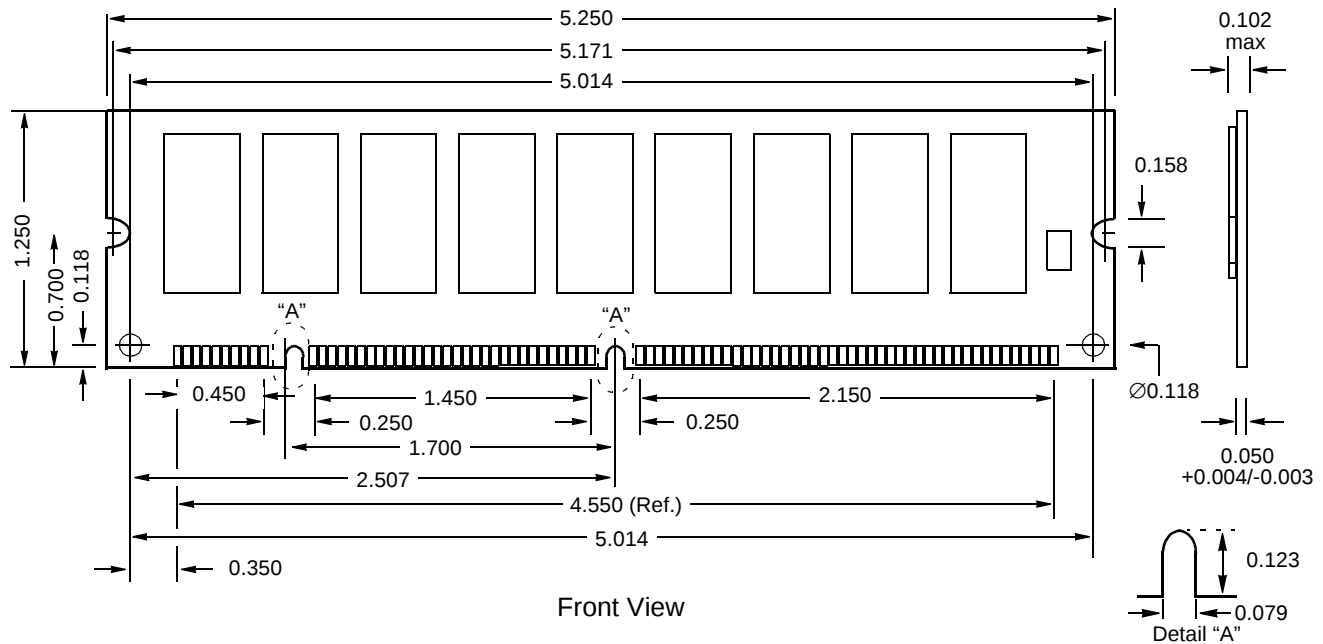
(TA = 0 to +70°C, V<sub>CC</sub> = 3.3V±0.3V, V<sub>SS</sub> = 0V)

| Parameter                                    |      | Symbol           | Unit  | 125 |        | 100 |        | 84  |        | 67  |        | Notes      |
|----------------------------------------------|------|------------------|-------|-----|--------|-----|--------|-----|--------|-----|--------|------------|
| Clock Period                                 | CL=3 | t <sub>CK</sub>  | ns    | 8   | -      | 10  | -      | 12  | -      | 15  | -      | 1, 2, 3, 6 |
|                                              | CL=2 |                  |       | 12  | -      | 15  | -      | 17  | -      | 20  | -      |            |
| Transition Time                              |      | t <sub>T</sub>   | ns    | 0.5 | 2      | 0.5 | 2      | 0.5 | 2      | 0.5 | 2      | 1, 2, 3    |
| Clock High Time                              |      | t <sub>CH</sub>  | ns    | 3.5 | -      | 3.5 | -      | 4   | -      | 4   | -      | 1, 2, 3    |
| Clock Low Time                               |      | t <sub>CL</sub>  | ns    | 3.5 | -      | 3.5 | -      | 4   | -      | 4   | -      | 1, 2, 3    |
| Input Setup Time                             |      | t <sub>SI</sub>  | ns    | 2.5 | -      | 3.0 | -      | 3.0 | -      | 3.0 | -      | 1, 2, 3    |
| Input Hold Time                              |      | t <sub>HI</sub>  | ns    | 1.0 | -      | 1.0 | -      | 1.0 | -      | 1.0 | -      | 1, 2, 3    |
| Output Valid from Clock                      | CL=3 | t <sub>AC</sub>  | ns    | -   | 7.5    | -   | 8.5    | -   | 8.5    | -   | 9.0    | 1, 2, 3    |
|                                              | CL=2 |                  |       | -   | 9      | -   | 9      | -   | 10     | -   | 10     |            |
| Output In Low-Z                              |      | t <sub>OLZ</sub> | ns    | 2   | -      | 3   | -      | 3   | -      | 3   | -      | 1, 2, 3    |
| Output in High-Z                             |      | t <sub>OHZ</sub> | ns    | 2   | -      | 3   | -      | 3   | -      | 3   | -      | 1, 2, 3, 4 |
| Output Hold Time                             |      | t <sub>OH</sub>  | ns    | 2   | -      | 3   | -      | 3   | -      | 3   | -      | 1, 2, 3    |
| Time between Refresh                         |      | t <sub>REF</sub> | ms    | -   | 65.6   | -   | 65.6   | -   | 65.6   | -   | 65.6   | 1, 2, 3    |
| RAS Cycle Time                               |      | t <sub>RC</sub>  | ns    | 77  | -      | 90  | -      | 100 | -      | 110 | -      | 1, 2, 3, 5 |
| RAS Access Time                              |      | t <sub>RAC</sub> | ns    | -   | 45     | -   | 54     | -   | 56     | -   | 60     | 1, 2, 3    |
| CAS Access Time                              |      | t <sub>CAC</sub> | ns    | -   | 21     | -   | 24     | -   | 26     | -   | 30     | 1, 2, 3    |
| RAS Precharge Time                           |      | t <sub>RP</sub>  | ns    | 29  | -      | 30  | -      | 35  | -      | 40  | -      | 1, 2, 3    |
| RAS Active Time                              |      | t <sub>RAS</sub> | ns    | 48  | 100000 | 60  | 100000 | 65  | 100000 | 70  | 100000 | 1, 2, 3    |
| RAS to CAS Delay Time                        |      | t <sub>RCD</sub> | ns    | 24  | -      | 30  | -      | 30  | -      | 30  | -      | 1, 2, 3    |
| Write Recovery Time                          |      | t <sub>WR</sub>  | ns    | 8   | -      | 10  | -      | 12  | -      | 15  | -      | 1, 2, 3    |
| RAS to RAS Delay Time                        |      | t <sub>RRD</sub> | ns    | 16  | -      | 20  | -      | 20  | -      | 20  | -      | 1, 2, 3    |
| Power-down Exit Time                         |      | t <sub>PDE</sub> | ns    | 3   | -      | 3   | -      | 4   | -      | 5   | -      | 1, 2, 3    |
| CKE to Clock Disable                         |      | t <sub>CKE</sub> | cycle | 1   |        | 1   |        | 1   |        | 1   |        |            |
| DQM to Output in High-Z                      |      | t <sub>DQZ</sub> | cycle | 2   |        | 2   |        | 2   |        | 2   |        |            |
| DQM to Input Data Delay                      |      | t <sub>DQD</sub> | cycle | 0   |        | 0   |        | 0   |        | 0   |        |            |
| Last Output to Write Command Delay           |      | t <sub>OWD</sub> | cycle | 2   |        | 2   |        | 2   |        | 2   |        |            |
| Write Command to Input Data Delay            |      | t <sub>DWD</sub> | cycle | 0   |        | 0   |        | 0   |        | 0   |        |            |
| Precharge to Output in High-Z Delay          | CL=3 | t <sub>ROH</sub> | cycle | 3   |        | 3   |        | 3   |        | 3   |        |            |
|                                              | CL=2 |                  |       | 2   |        | 2   |        | 2   |        | 2   |        |            |
| Burst Stop Command to output in High-Z Delay | CL=3 | t <sub>BSH</sub> | cycle | 3   |        | 3   |        | 3   |        | 3   |        |            |
|                                              | CL=2 |                  |       | 2   |        | 2   |        | 2   |        | 2   |        |            |
| Mode Register Access to Bank Active (min.)   |      | t <sub>MRD</sub> | cycle | 2   |        | 2   |        | 2   |        | 2   |        |            |
| CAS to CAS Delay                             |      | t <sub>CCD</sub> | cycle | 1   |        | 1   |        | 1   |        | 1   |        |            |
| CAS Bank Delay                               |      | t <sub>CBD</sub> | cycle | 1   |        | 1   |        | 1   |        | 1   |        |            |
| Write to Precharge Read Delay                | CL=3 | t <sub>RWL</sub> | cycle | 1   |        | 1   |        | 1   |        | 1   |        |            |
|                                              | CL=2 |                  |       | 1   |        | 1   |        | 1   |        | 1   |        |            |

- Notes:
1. An initial pulse of at least 200μs is required after power-up followed by a minimum of eight auto refresh cycles.
  2. AC characteristics assume t<sub>T</sub> = 1ns and 50pF capacitive load. If t<sub>T</sub> is longer than 1ms, reference level for measuring time of input signal is V<sub>IH</sub> (min.) and V<sub>IL</sub> (max.).
  3. 1.4V is the reference level for measuring timing of input signals.
  4. t<sub>HZ</sub> and t<sub>OH</sub> defines the time at which the outputs achieve ±200mV.
  5. Actual clock output of t<sub>RC</sub> will be sum clock of t<sub>RAS</sub> and t<sub>RP</sub>.
  6. 20ns is not supported in SPD.

## Physical Dimensions

168-pin (84x2) DIMM



- Notes:
1. All dimensions are in inches.
  2. Pin 85 is behind pin 1 on the back side.

## SDC8UL7284-(67/84/100/125)T-S

### Ordering Information

S D C 8 U L 72 8 4 - 100 T - S

(1) (2) (3) (4) (5) (6) (7) (8) (8a) (9) (10) (11) (12) (13) (14)

(1) **Memory Type**

S : SDRAM  
G : SGRAM

(2) **Module Shape**

S : SIMM  
D : DIMM  
O : Small Outline DIMM

(3) **Module Pin Count**

A : 72-pin  
B : 144-pin  
C : 168-pin  
D : 200-pin

(4) **Word Depth**

1 : 1M  
2 : 2M  
4 : 4M  
8 : 8M  
256 : 256K  
512 : 512K

(5) **Buffer Type**

B : Buffered  
U : Unbuffered

(6) **Operating Voltage & Power Consumption**

V : 3.3V & Standard Power  
L : 3.3V & Low Power

(7) **Data Width**

(ex. 64=x64, 72=x72 etc.)

(8) **Device Configuration**

4 : x4  
8 : x8  
1 : x16  
3 : x32

(8a) **Refresh**

2 : 2krf  
4 : 4krf

(9) **Interface Level**

Blank : LVTTTL  
S : SSTL

(10) **Module Revision / Applied "Standard" \*1**

Blank : Rev. 0  
A : Rev. 1  
B : Rev. 2 (etc.)

\*1 When DRAM device or PCB is revised, the revision is changed

(11) **Clock Frequency**

67 : 67Mhz  
84 : 84Mhz  
100 : 100Mhz  
125 : 125Mhz

(12) **Package of Component**

J : SOJ  
T : TSOP

(13) **Private Brand Name \*2**

Blank : Common Products  
G : FMG Brand

\*2 This column is applicable to custom modules, NOT applicable to JEDEC standard commodity products

(14) **Assembly & Test Site**

S : Smart Modular Technologies

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