

SAM9755

Mobil Phone Synthesizer

OVERVIEW

The SAM9755 integrates into a single chip a SAM97xx core (64 slots DSP + 16bit processor), a 32k x 16 RAM and glue logic. With addition of an external ROM or FLASH and a stereo DAC, a complete MIDI sound unit can be built, including reverb and chorus effects, parametric equalizer and surround effects. The SAM9755 is housed in a CBGA 100 package.

KEY FEATURES

- 28MHz built-in 16 bit micro-controller
- 64 voices synthesizer & effects processor DSP
- High quality Wavetable sound synthesis
- Audio effects: Reverb, Chorus, Surround, Equalizer
- Memory Management Unit allows the DSP & the μ processor to share internal & external ROM/RAM
- On chip 32K*16 RAM
- Up to 16Mega x 16 external ROM/RAM
- 2 stereo audio output

- 27.16875 kHz nominal sampling rate
- 2.7V power supply
- Power-down mode
- Single 6.9552 MHz crystal operation, built-in PLL minimizes RFI
- Serial host interface (MIDI in)

- Compatible with SAM97xx sounds and firmware
- Existing SAM97xx tools available for sound and sound banks developments
- Sample sets available under special licensing conditions

PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10
A										
	WA3	WA7	VCC	WA12	WA17	WA19	WA21	CS1_	WR_	WD1
B										
	VCC	WA4	WA8	WA10	WA14	VCC	WA22	VCC	WD0	WD2
C										
	TEST1	WA0	WA2	WA6	WA11	WA16	VCC	WA20	RD_	WD4
D										
	PDWN_	TEST2	TEST0	WA1	WA5	WA13	WA15	WA18	CS0_	VCC
E										
	DAAD	DEBUG_	RESET_	TEST3	GND	WA9	GND	GND	WD5	WD9
F										
	DACLK	MIDI_OUT	DABD0	WSBD	CLBD	GND	GND	WD3	WD7	WD10
G										
	X1	X2	MIDI_IN	DABD1	VCC	GND	WD6	WD8	WD12	WD11
H										
	LFT	VCC	VCC	GND	GND	GND	GND	WD13	WD14	WD15
J										
	GND	VCC	VCC	GPIO4	RUN	GND	GND	GND	GND	VCC
K										
	GND	GPIO2	GPIO3	N.C.	VCC	GND	GND	VCC	GND	VCC

PIN DESCRIPTION

Pin numbers

Pin #	Name	Ref	Pin #	Name	Ref	Pin #	Name	Ref
1	WA4	B2	34	VCC	K5	67	GND	E7
2	VCC	B1	35	RUN	J5	68	WA15	D7
3	WA0	C2	36	GND	H5	69	VCC	D10
4	WA2	C3	37	VCC	G5	70	CS0/	D9
5	TEST1	C1	38	CLBD	F5	71	WA18	D8
6	TEST2	D2	39	GND	K6	72	WD4	C10
7	PWDN/	D1	40	GND	J6	73	RD/	C9
8	TEST0	D3	41	GND	H6	74	WD2	B10
9	DAAD	E1	42	GND	G6	75	WD1	A10
10	DEBUG/	E2	43	WD6	G7	76	WD0	B9
11	RESET/	E3	44	GND	K7	77	WR/	A9
12	TEST3	E4	45	GND	J7	78	VCC	B8
13	GND	E5	46	GND	H7	79	WA20	C8
14	DACLK	F1	47	VCC	K8	80	CS1/	A8
15	MIDI_OUT	F2	48	GND	J8	81	WA22	B7
16	DABD0	F3	49	GND	K9	82	WA21	A7
17	WSBD	F4	50	VCC	K10	83	VCC	C7
18	DABD1	G4	51	GND	J9	84	WA19	A6
19	X1	G1	52	VCC	J10	85	VCC	B6
20	X2	G2	53	WD14	H9	86	WA16	C6
21	MIDI_IN	G3	54	WD13	H8	87	WA13	D6
22	LFT	H1	55	WD15	H10	88	WA9	E6
23	VCC	H2	56	WD12	G9	89	WA17	A5
24	GND	J1	57	WD11	G10	90	WA14	B5
25	GND	K1	58	WD8	G8	91	WA11	C5
26	VCC	J2	59	WD10	F10	92	WA5	D5
27	GPIO2	K2	60	WD7	F9	93	WA1	D4
28	VCC	J3	61	WD3	F8	94	WA12	A4
29	VCC	H3	62	GND	F7	95	WA10	B4
30	GPIO3	K3	63	GND	F6	96	WA6	C4
31	GPIO4	J4	64	WD9	E10	97	VCC	A3
32	N.C.	K4	65	WD5	E9	98	WA8	B3
33	GND	H4	66	GND	E8	99	WA7	A2
						100	WA3	A1

Power supply

PIN NAME	PIN Cnt	TYPE	FUNCTION
GND	19	PWR	DIGITAL GROUND (All pins should be connected to a ground plane)
VCC	15	PWR	POWER SUPPLY, 2.7V (All pins should be connected to a VCC plane)

Power supply decoupling note : like all high speed HCMOS ICs proper decoupling is mandatory for reliable operation and RFI reduction. The recommended decoupling is 100nF at each corner of the IC with an additional 10μFT bulk capacitor close to the X1, X2 pins.

Serial MIDI

PIN NAME	PIN Cnt	TYPE	FUNCTION
MIDI_IN	1	IN	SERIAL MIDI IN
MIDI_OUT	1	OUT	SERIAL MIDI OUT

External PCM ROM/RAM/IO

PIN NAME	PIN Cnt	TYPE	FUNCTION
WA0-WA22	23	OUT	External memory / IO Address, up to 16 Mega x 16 for direct ROM/RAM connection.
WD0-WD15	16	I/O	External memory/ IO data. Data is read (input) when RD/ is low, written (output) when WR/ is low.
RD/	1	OUT	External ROM/RAM/peripherals read
WR/	1	OUT	External RAM/peripherals write
CS0/-CS1/	2	OUT	Programmable chip selects. Can be configured to handle several ROMs or mixed RAM/ROM/FLASH

Digital audio group

The SAM9755 connects to a variety of stereo DACs or Codecs from 16 to 20 bits, with Japanese or I2S format. This includes AD1857JRS, PCM1718, PCM3001, TDA1305, TDA1543, TDA1545, TDA1311. When Japanese format is used, only 16 bits is supported without external circuitry.

PIN NAME	PIN Cnt	TYPE	FUNCTION
DACLK	1	OUT	Master clock for Σ/Δ DAC (256 x Fs)
DABD0-DABD1	2	OUT	Serial data for 2 stereo output channels.
DAAD	1	IN	Serial data for 1 stereo input channel
CLBD	1	OUT	Digital audio bit clock
WSBD	1	OUT	Digital audio left/right select

Miscellaneous group

PIN NAME	PIN Cnt	TYPE	FUNCTION
GPIO2-GPIO4	3	I/O	see note
DEBUG/	1	IN	Configuration pin, low for codeview debugging/. Should be tied to VCC for normal operation.
RESET/	1	IN	Reset input, active low. This is a Schmitt trigger input, allowing direct connection of a RC network.
RUN	1	OUT	Indicates that the DSP is up and running. Can be used as external DAC reset.
PDWN/	1	IN	Power down, active low. When power down is active, all output pins will be floated. The crystal oscillator will be stopped. To exit from power down mode, PDWN/ should be high and RESET/ applied.
X1-X2	2	-	6.9552 MHz (nominal) crystal connection (11.2896 MHz max) . An external clock can also be used at X1
TEST0-TEST3	4	IN	Test pins, should be grounded
LFT	1	-	PLL external RC network

Note : These pins can be individually used as general purpose I/Os or as alternate functions. When used as general purpose I/O they can be individually configured as inputs or outputs. When used as alternate functions their meaning changes as follows :

- GPIO2 = DBCLK (input)
- GPIO3 = DBACK (output)
- GPIO4 = DBDATA (I/O)
- DBCLK, DBACK, DBDATA are used for debugging or external flash memory programming when DEBUG/ is low

ABSOLUTE MAXIMUM RATINGS

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	-0.5	-	4.5	V
Voltage on all Inputs	-	-0.5	-	VCC+0.5	V
Operating temperature	-	-40	-	85	°C
Storage temperature	-	-65	-	150	°C
IOL per I/O pin	-	-	-	10	mA

DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

(-15°C ≤ T_A ≤ 70°C ; VC3 = +2.7V ±10%)

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Supply Voltage	VCC	2.4	2.7	3.5	V
Input Low Level Voltage	VIL	-0.5	-	0.8	V
Input High Level Voltage	VIH	2.0	-	VCC+0.5	V
Output Low Level Voltage (IOL = 3.2mA)	VOL	-	-	0.45	V
Output High Level Voltage (IOH = -0.8mA)	VOH	2.4	-	-	V
Power Supply Current (See note 1)	ICC	-	35	45	mA
Power Down Supply Current	-	-	500	700	µA

Note : 1. Crystal frequency = 6.9552 MHz

EXTERNAL ROM/SRAM READ CYCLE

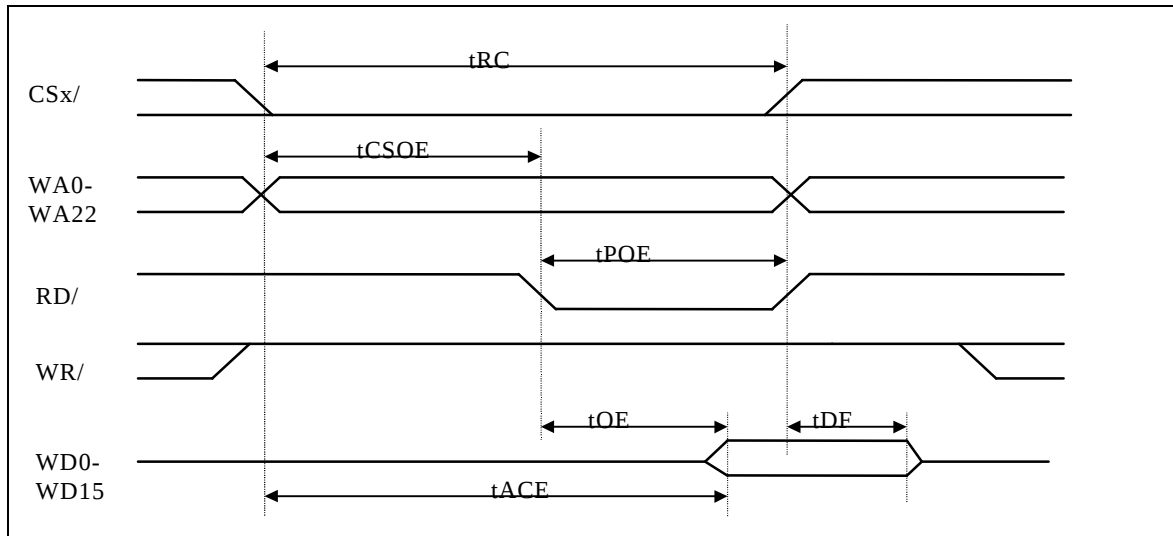


Figure 1
External ROM/SAM Read Cycle

Timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Read cycle time	tRC	180	-	216	ns
CSx/ low / address valid to RD/ low	tCSOE	67	-	113	ns
Output enable pulse width	tPOE	-	108	-	ns
Chip select/address access time	tACE	175	-	-	ns
Output enable access time	tOE	103	-	-	ns
Chip select or RD/ high to input data Hi-Z	tDF	0	-	67	ns

EXTERNAL SRAM WRITE CYCLE

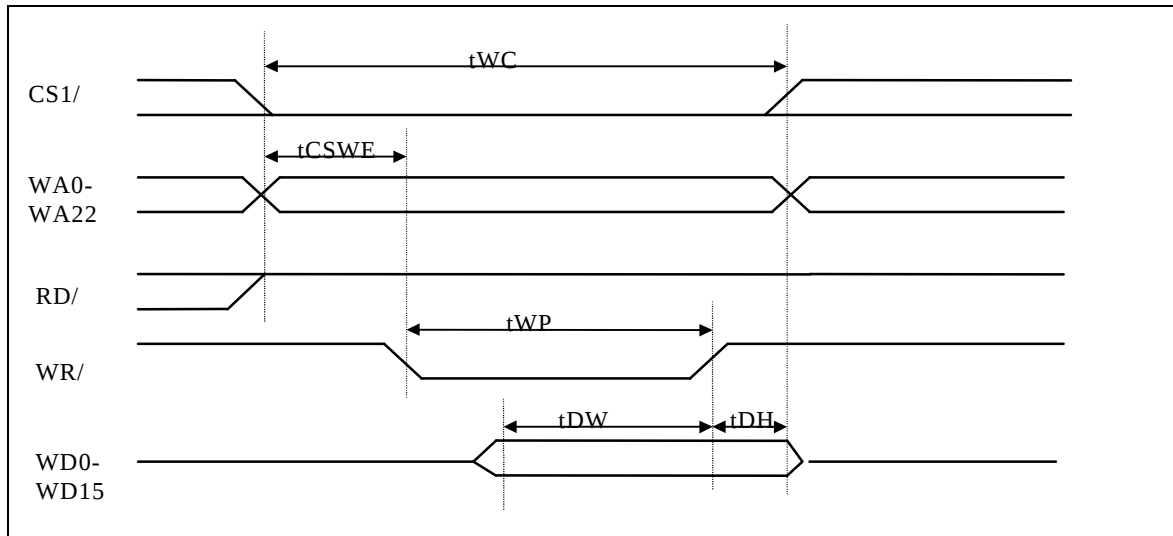


Figure 2
External SRAM Write Cycle

Timing parameters

Parameter	Symbol	Min	Typ	Max	Unit
Write pulse width	t_{WP}	-	144	-	ns
Data out setup time	t_{DW}	134	-	-	ns
Data out hold time	t_{DH}	10	-	-	ns

Reset

During power-up, the RESET/ input should be held low until oscillator and PLL are stabilized, which can take about 20 ms. The RESET / signal is normally derived from the microprocessor power supervisor or reset circuit. However, a typical RC/diode power-up network can also be used for some applications.

DIGITAL AUDIO

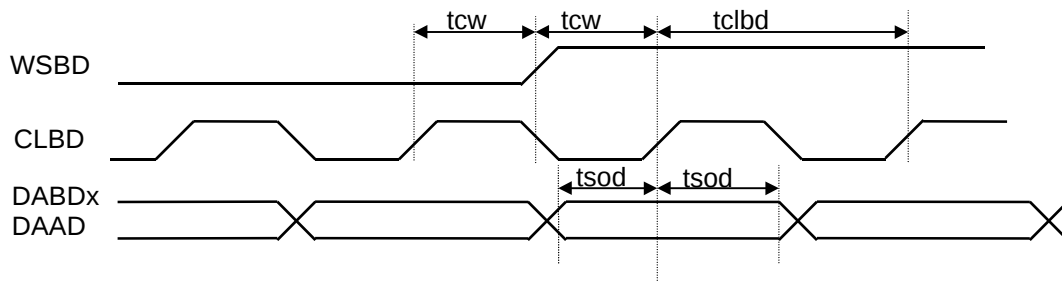


Figure 3
Digital Audio Timing

DIGITAL AUDIO FRAME

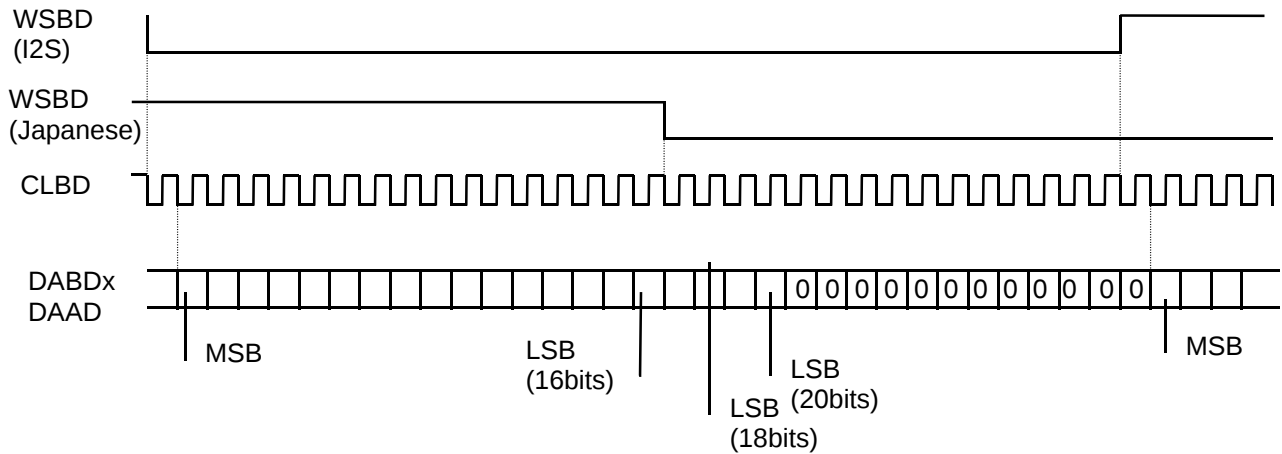
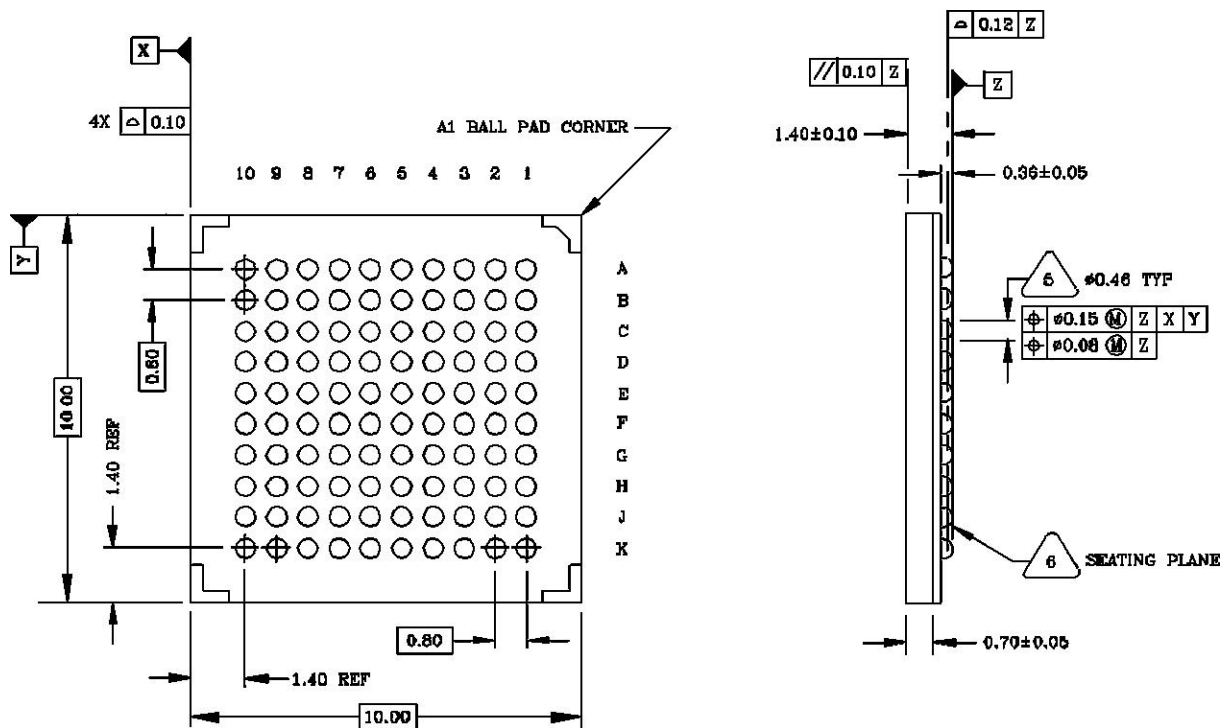


Figure 4
Digital Audio Frame Format

Timing Parameters

Parameter	Symbol	Min	Typ	Max	Unit
CLBD rising to WSBD change	tcw	278	-	-	ns
DABDx valid prior/after CLBD rising	tsod	278	-	-	ns
CLBD cycle time	tclbd	-	576	-	ns

MECHANICAL DIMENSIONS



Package outline - CABGA 100
10.00mm x 10.00mm, 2 layer,
0.80mm pitch, Laminate Substrate, AAP

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