16M X 64 Bits (128MB) 144-Pin Flash SO-DIMM (3.3V Only)

FEATURES

- Access Time of 150ns
- TTL compatible inputs and outputs
- 3.3V only power supply
- JEDEC standard components
- Tin (option “T”) or gold (option “G”) edge connectors
- Three power on reset options
  - No power on reset: /RST tied to V_{CC} (Option “V”)
  - Power on reset: /RST tied to power supervisor circuit (Option “R”)
  - System control of power on reset: /RST tied to pin 118 (Option “S”)
- Intel Part Number RC28F128J3A flash memory components
- Minimum 12,800,000 total write/erase cycles

GENERAL DESCRIPTION

This SiliconTech product is a 16M x 64 bits flash Small Outline Duel In-line Memory Module (SO-DIMM). This module consists of eight 16M x 8 bits CMOS flash memory in Easy BGA packages mounted on a 144-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are also mounted.

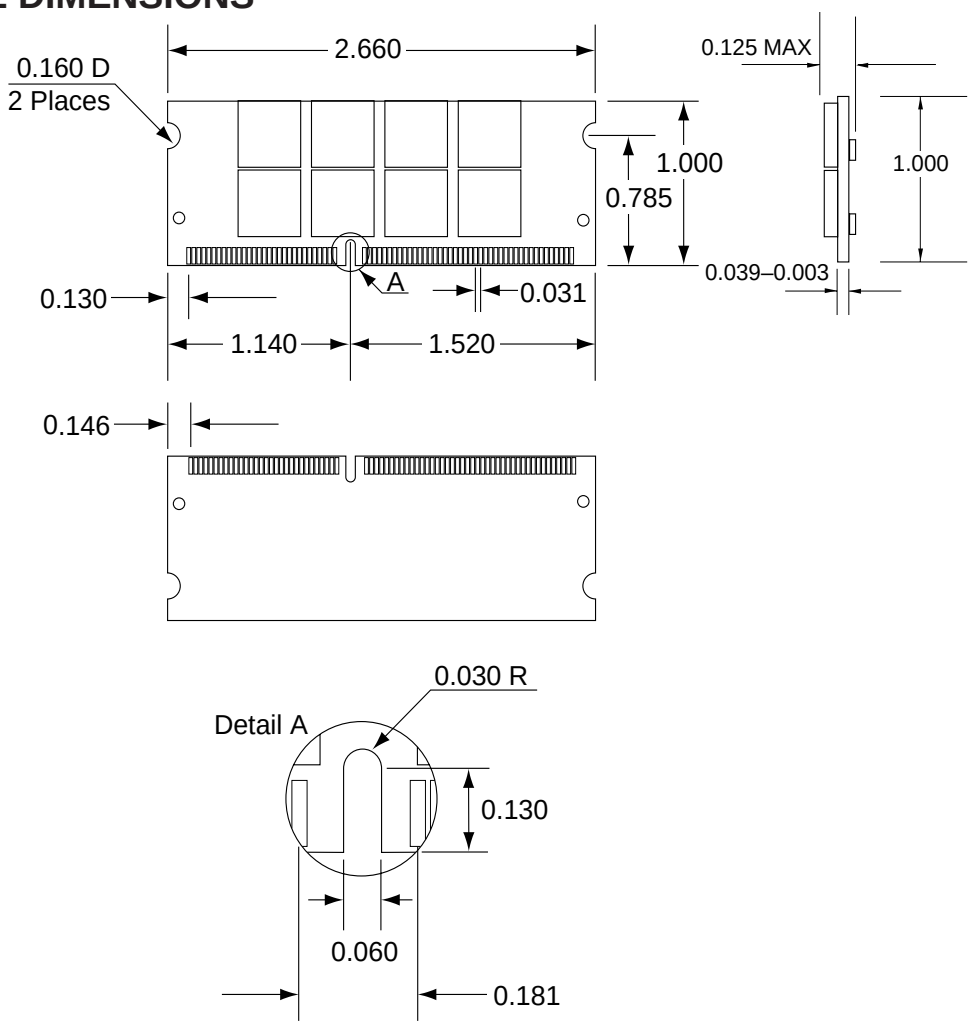
Option “T” provides tin edge connectors and option “G” provides gold edge connectors. Option “R” provides power on reset through a power supervisor circuit; option “S” provides system control of power on reset by connecting the reset signals to Pin 118; and, option “V” provides no power on reset.

The module is intended for mounting into 144-pin SO-DIMM edge connector sockets keyed for 3.3V power supply. The module uses the standard programming algorithms for Intel RC28F128J3A StrataFlash memory components.

† “Advanced” indicates that this product is in design engineering and that it may or may not be moved into production. Parameters may change.

PACKAGE DIMENSIONS

Units: Inches



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TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	21	V_{SS}	41	DQ_{10}	61	A_{15}	81	V_{DD}	101	V_{DD}	121	DQ_{24}	141	PD_1
2	V_{SS}	22	V_{SS}	42	DQ_{42}	62	A_{18}	82	V_{DD}	102	V_{DD}	122	DQ_{56}	142	3/5*
3	DQ_0	23	$/OE_0$	43	DQ_{11}	63	V_{DD}	83	DQ_{16}	103	A_6	123	DQ_{25}	143	V_{DD}
4	DQ_{32}	24	$/OE_2$	44	DQ_{43}	64	V_{DD}	84	DQ_{48}	104	A_7	124	DQ_{57}	144	V_{DD}
5	DQ_1	25	$/WE_0$	45	V_{DD}	65	A_{16}	85	DQ_{17}	105	A_8	125	DQ_{26}		
6	DQ_{33}	26	$/WE_2$	46	V_{DD}	66	A_{19}	86	DQ_{49}	106	A_{11}	126	DQ_{58}		
7	DQ_2	27	V_{DD}	47	DQ_{12}	67	A_{23}	87	DQ_{18}	107	V_{SS}	127	DQ_{27}		
8	DQ_{34}	28	V_{DD}	48	DQ_{44}	68	A_{20}	88	DQ_{50}	108	V_{SS}	128	DQ_{59}		
9	DQ_3	29	A_0	49	DQ_{13}	69	$/CE_0$	89	DQ_{19}	109	A_9	129	V_{DD}		
10	DQ_{35}	30	A_3	50	DQ_{45}	70	$/CE_1$*	90	DQ_{51}	110	A_{12}	130	V_{DD}		
11	V_{DD}	31	A_1	51	DQ_{14}	71	A_{25}***	91	V_{SS}	111	A_{10}	131	DQ_{28}		
12	V_{DD}	32	A_4	52	DQ_{46}	72	V_{PP}*	92	V_{SS}	112	A_{13}	132	DQ_{60}		
13	DQ_4	33	A_2	53	DQ_{15}	73	A_{24}**	93	DQ_{20}	113	V_{DD}	133	DQ_{29}		
14	DQ_{36}	34	A_5	54	DQ_{47}	74	A_{22}	94	DQ_{52}	114	V_{DD}	134	DQ_{61}		
15	DQ_5	35	V_{SS}	55	V_{SS}	75	V_{SS}	95	DQ_{21}	115	$/OE_1$	135	DQ_{30}		
16	DQ_{37}	36	V_{SS}	56	V_{SS}	76	V_{SS}	96	DQ_{53}	116	$/OE_3$	136	DQ_{62}		
17	DQ_6	37	DQ_8	57	/RST	77	A_{21}	97	DQ_{22}	117	$/WE_1$	137	DQ_{31}		
18	DQ_{38}	38	DQ_{40}	58	/WP*	78	PD_2	98	DQ_{54}	118	/WE3	138	DQ_{63}		
19	DQ_7	39	DQ_9	59	A_{14}	79	RY/BY*	99	DQ_{23}	119	V_{SS}	139	V_{SS}		
20	DQ_{39}	40	DQ_{41}	60	A_{17}	80	PD_3	100	DQ_{55}	120	V_{SS}	140	V_{SS}		

* No Connection (Not Used).

** Address A_{24} is only valid on 256-Mbit densities and above, otherwise, it is a no connect.

*** Address A_{25} is only valid on 512-Mbit densities. A_{25} is pre-assigned to pin 71. A_{25} is not yet defined on the StrataFlash BGA per Intel; therefore, A_{25} is added to this specification only, and is not yet routed on the PCB.

Pin Functions

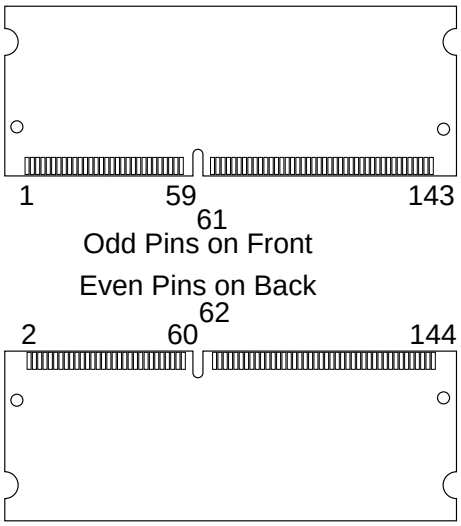
Pin Symbol	Pin Function
A_0-A_{23}	Address Inputs
DQ_0-DQ_{63}	Data In/Out
$/CE_0$	Chip Enable
$/WE_0$-$/WE_3$	Write Enable
$/OE_0$-$/CE_3$	Output Enable
PD_1-PD_3	Presence Detect
/RST	Reset
V_{DD}	Power (+3.3V)
V_{SS}	Ground

Presence Detect Pins*

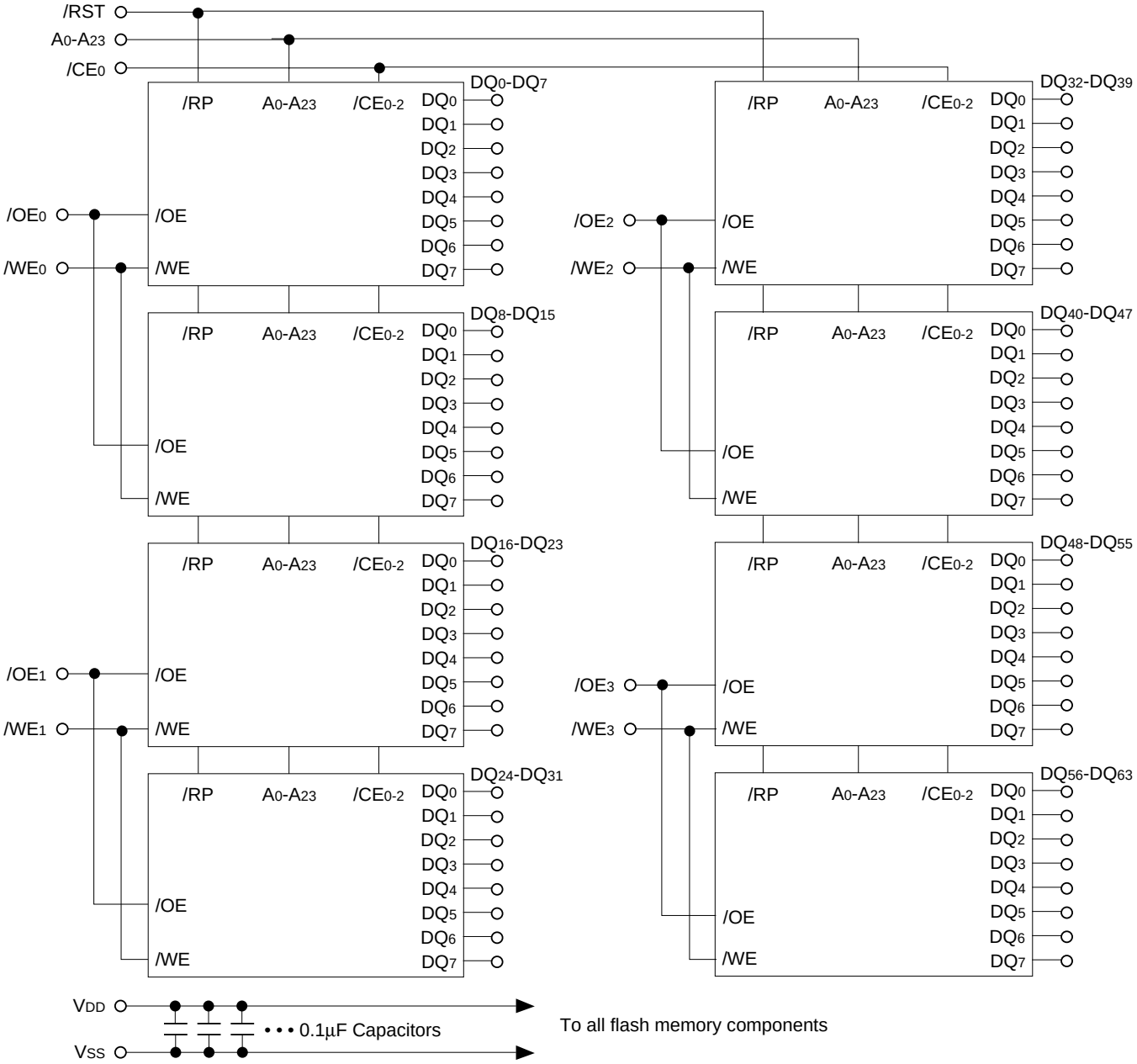
Module Capacity	Chip Used	Max. Access	Pin Symbol		
			PD_1	PD_2	PD_3
128 MB	28F128J3A	150 ns	0	0	1
1=Open Circuit (No Connection) 0=Connected to V_{SS}					

* Pin Connection Changing Available.

Pin Locations



FUNCTIONAL BLOCK DIAGRAM



NOTE: /RST optionally tied to VDD, pin 118 of module edge connector, or a power supervisor circuit.

/BYTE of all flash memory components is tied to VSS.

STS of all flash memory components is tied to VDD through a pull-up resistor.

/CE0, /CE1, and /CE2 of all flash memory components are tied together.

VPEN of all flash memory is tied to VDD.