32M X 32 Bits (128MB) DRAM 72-Pin SIMM with Extended Data Out (EDO)

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- Extended Data Out (EDO) Mode operation (called Hyper Page)
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V $\pm$ 10% power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Gold or Tin edge connectors

GENERAL DESCRIPTION

The SiliconTech SL32(S/T)4F32M4E-A60C is a 32M x 32 bits Dynamic RAM (DRAM) Single In-line Memory Module (SIMM). This module consists of eight CMOS 16M x 8 bits DRAM stacks mounted on a 72-pin glass epoxy substrate using the SiliconTech patented IC Tower stacking technology (Patent Number 5,514,907). Each stack consists of two 16M x 4 bits DRAMs in 400-mil 32-pin TSOP-II packages. Decoupling capacitors of 0.1µF are also mounted on the substrate.

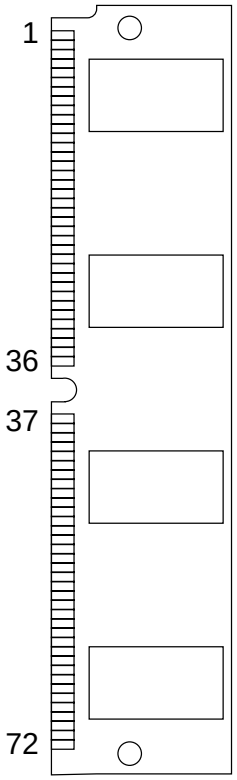
A 5.0V to 3.3V convertor supplies power to the 3.3V components, and bus switches convert the signals to the 3.3V components from 5.0V to 3.3V

The SL32S4F32M4E-A60C has gold edge connectors and the SL32T4F32M4E-A60C has tin edge connectors and are intended for mounting into 72-pin SIMM edge connector sockets with the same lead (i.e. gold or tin).

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{22}	49	DQ_8
2	DQ_0	26	DQ_7	50	DQ_{24}
3	DQ_{16}	27	DQ_{23}	51	DQ_9
4	DQ_1	28	A_7	52	DQ_{25}
5	DQ_{17}	29	A_{11}	53	DQ_{10}
6	DQ_2	30	V_{CC}	54	DQ_{26}
7	DQ_{18}	31	A_8	55	DQ_{11}
8	DQ_3	32	A_9	56	DQ_{27}
9	DQ_{19}	33	$\overline{RAS}_3$	57	DQ_{12}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{28}
11	NC	35	NC	59	V_{CC}
12	A_0	36	NC	60	DQ_{29}
13	A_1	37	NC	61	DQ_{13}
14	A_2	38	NC	62	DQ_{30}
15	A_3	39	V_{SS}	63	DQ_{14}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{31}
17	A_5	41	$\overline{CAS}_2$	65	DQ_{15}
18	A_6	42	$\overline{CAS}_3$	66	NC
19	A_{10}	43	$\overline{CAS}_1$	67	PD_1
20	DQ_4	44	$\overline{RAS}_0$	68	PD_2
21	DQ_{20}	45	$\overline{RAS}_1$	69	PD_3
22	DQ_5	46	NC	70	PD_4
23	DQ_{21}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}



Pin Functions

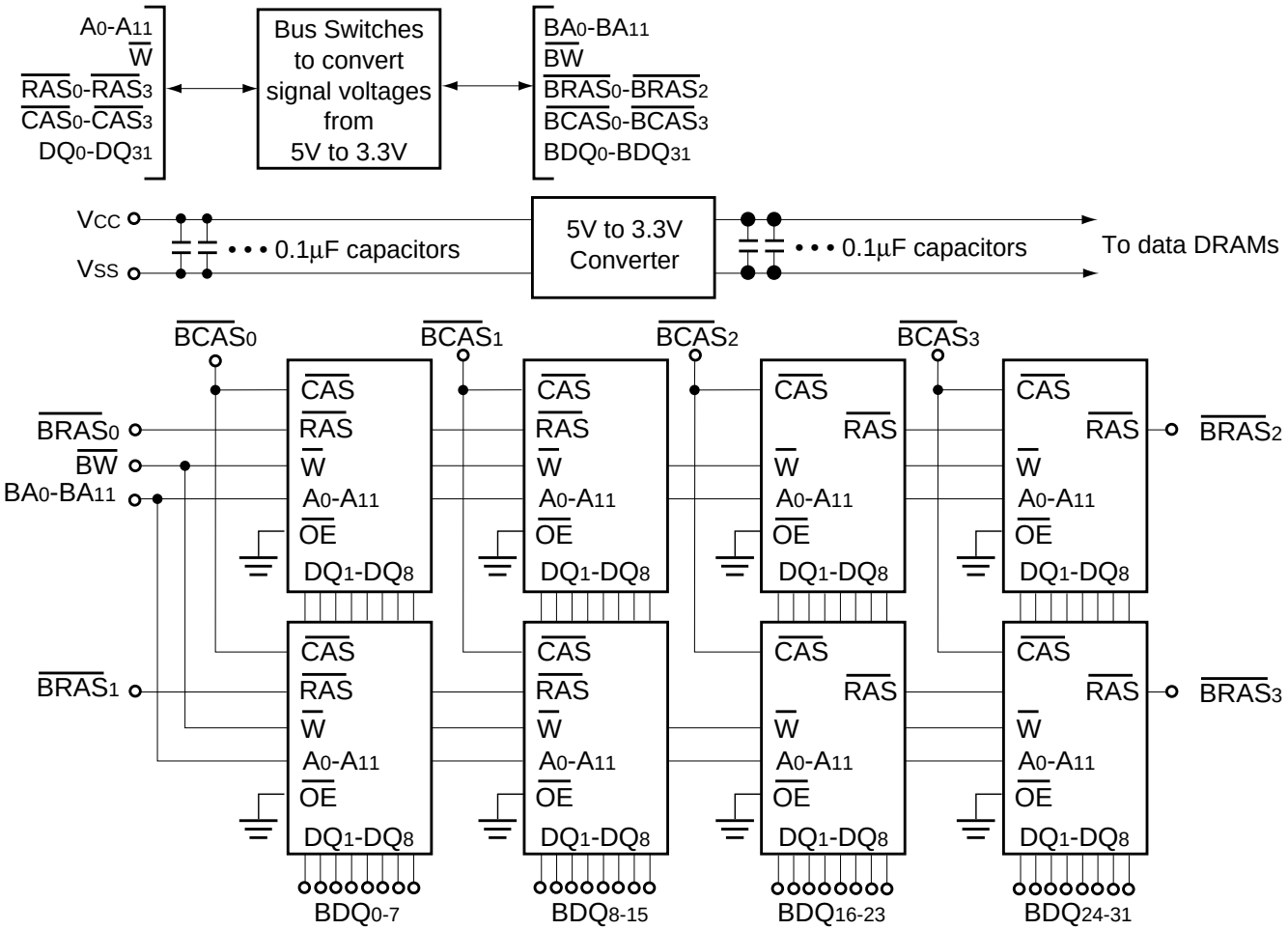
Pin Symbol	Pin Function
A_0-A_{11}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$-$\overline{RAS}_3$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

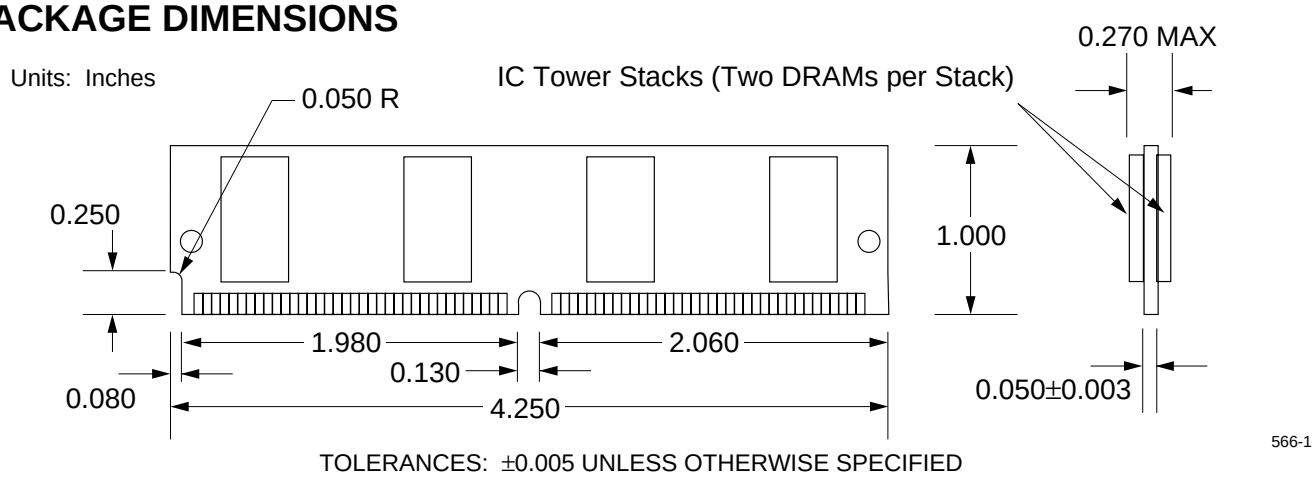
PD_1=NC, PD_2=V_{SS}, PD_3=NC, PD_4=NC

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED