32M X 36 Bits DRAM 72-Pin SIMM with Extended Data Out (EDO) and Parity

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- Extended Data Out (EDO) operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V ± 10% power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Parity
- Gold or tin edge connections

GENERAL DESCRIPTION

The SiliconTech SL36(S/T)8L32M4K-A60C is a 32M x 36 bits Dynamic RAM (DRAM) Single In-line Memory Module (SIMM). The module consists of eight 16M x 8 bits and four 32M x 4 bits IC Towers. Each IC tower consists of two CMOS 16M x 4 bits 3.3V DRAMs in 32-pin 400-mil TSOP-II packages. The SiliconTech IC Tower stacking technology is patented with Patent Number 5,514,907. The parity DRAMs use only one of the available four DQs.

A 5V to 3.3V voltage converter converts the 5V power supply from the host to 3.3V for the data DRAMs. Bus switches switch the signal voltages from 5V on the host side to 3.3V on the data DRAMs side.

The components are mounted on a 72-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are also mounted.

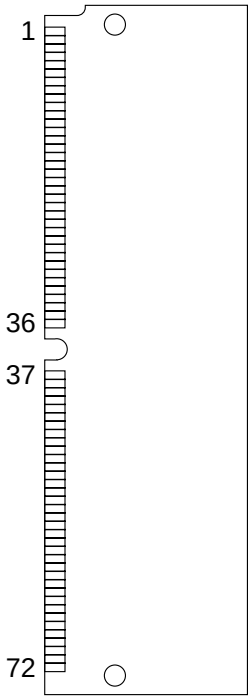
The SL36S8L32M4K-A60C has gold edge connections The SL36T8L32M4K-A60C has tin edge connections. The module is intended for mounting into 72-pin SIMM edge connector sockets with 5V power supply and the same lead, i.e. gold or tin.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	A_{11}	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	A_9	56	DQ_{30}
9	DQ_{21}	33	$\overline{RAS}_3$	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{31}
11	NC	35	DQ_{26}	59	V_{CC}
12	A_0	36	DQ_8	60	DQ_{32}
13	A_1	37	DQ_{17}	61	DQ_{14}
14	A_2	38	DQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{34}
17	A_5	41	$\overline{CAS}_2$	65	DQ_{16}
18	A_6	42	$\overline{CAS}_3$	66	NC
19	A_{10}	43	$\overline{CAS}_1$	67	PD_1
20	DQ_4	44	$\overline{RAS}_0$	68	PD_2
21	DQ_{22}	45	$\overline{RAS}_1$	69	PD_3
22	DQ_5	46	NC	70	PD_4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}

Pin Locations



Pin Functions

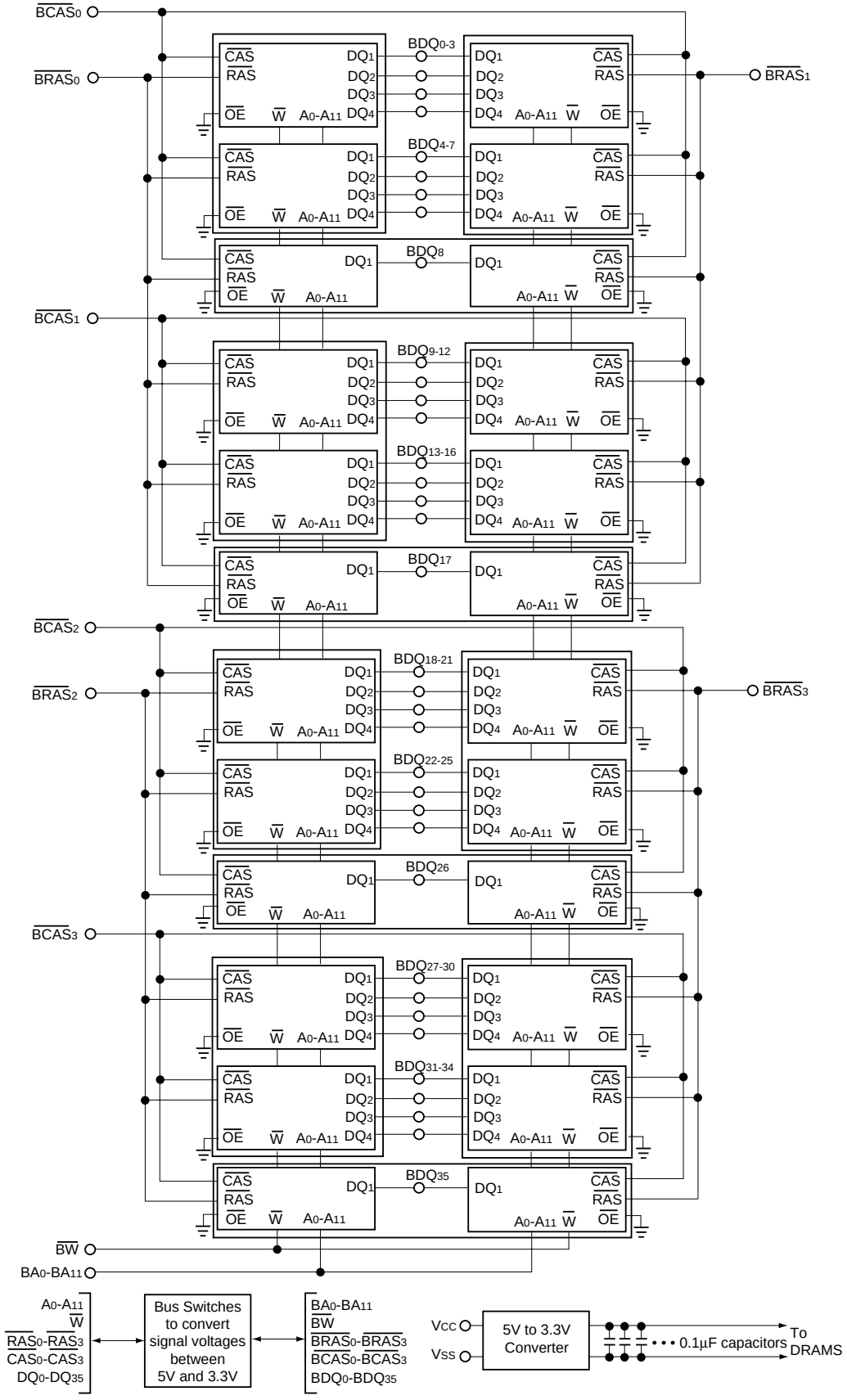
Pin Symbol	Pin Function
A_0-A_{11}	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$-$\overline{RAS}_3$	Row Address Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_5	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

For 32M x 36 Bits and 60ns:
PD_1= NC
PD_2= V_{SS}
PD_3= NC
PD_4= NC
PD_5= NC

* Pin Connection Changing Available

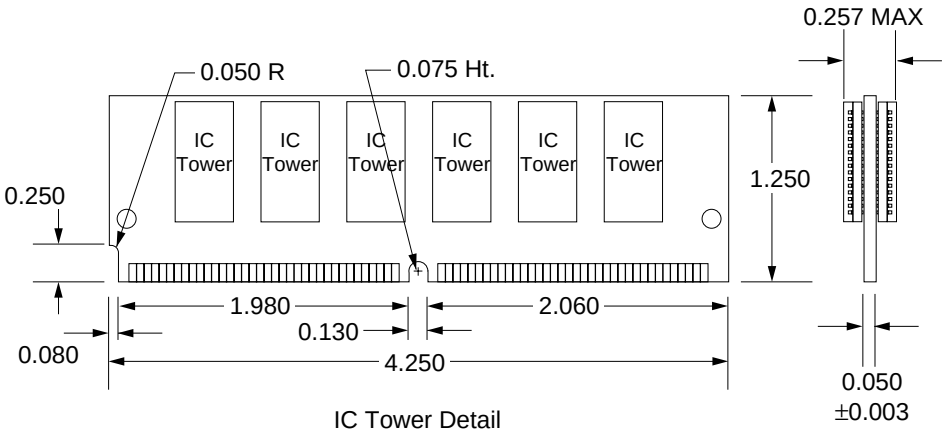
FUNCTIONAL BLOCK DIAGRAM



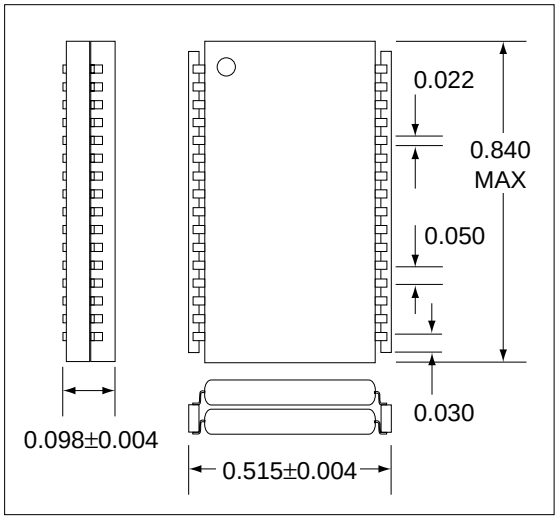
NOTE: DQ2-DQ4 of the parity DRAMs are not connected. Boxed pairs of DRAMs are stacked into an IC Tower.

PACKAGE DIMENSIONS

Units: Inches



IC Tower Detail
(Patent Number 5,514,907)



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TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED