8M X 72 Bits (64MB) DDR SDRAM 184-Pin Unbuffered DIMM ECC (PC1600/PC2100)

FEATURES

- PC1600/PC2100 Compliant
  (PC266A 133MHz—7.5ns@CL=2)
  (PC266B 133MHz—7.5ns@CL=2.5)
  (PC200 100MHz—10ns@CL=2)
- 184-Pin DIMM form factor
- Auto and self refresh capability
  (4096 cycles/64ms refresh)
- SSTL_2 compatible inputs and outputs
- +2.5V ± 0.2V V_{DD} and V_{DDQ}
- DDR architecture: Two data accesses per clock cycle, differential clock inputs (CK0 and /CK0), and bi-directional data strobe (DQS)
- Four internal banks for concurrent operation
- Auto Precharge option for each burst access
- Burst lengths: 2, 4, 8
- All inputs are sampled at the positive going edge of the system clock; data referenced to both edges of DQS
- Serial Presence Detect with EEPROM
- ECC

GENERAL DESCRIPTION

The SiliconTech SL72C8D8M4M-A###W is a 8M x 72 bits Double Data Rate (DDR) Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

This module consists of nine CMOS 2M x 8 bits x 4 banks DDR SDRAMs in 66-pin 400-mil TSOP-II packages. The DDR SDRAMs are mounted on a 184-pin glass epoxy substrate.

A serial EEPROM using the two pin IIC protocol is also mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.22µF are also mounted. Damping resistors are added to the DQ, DM, and DQS signals.

The module has gold edge connections and is intended for mounting into 184-pin DIMM edge connector sockets keyed for 2.5V V_{DD} and V_{DDQ}.

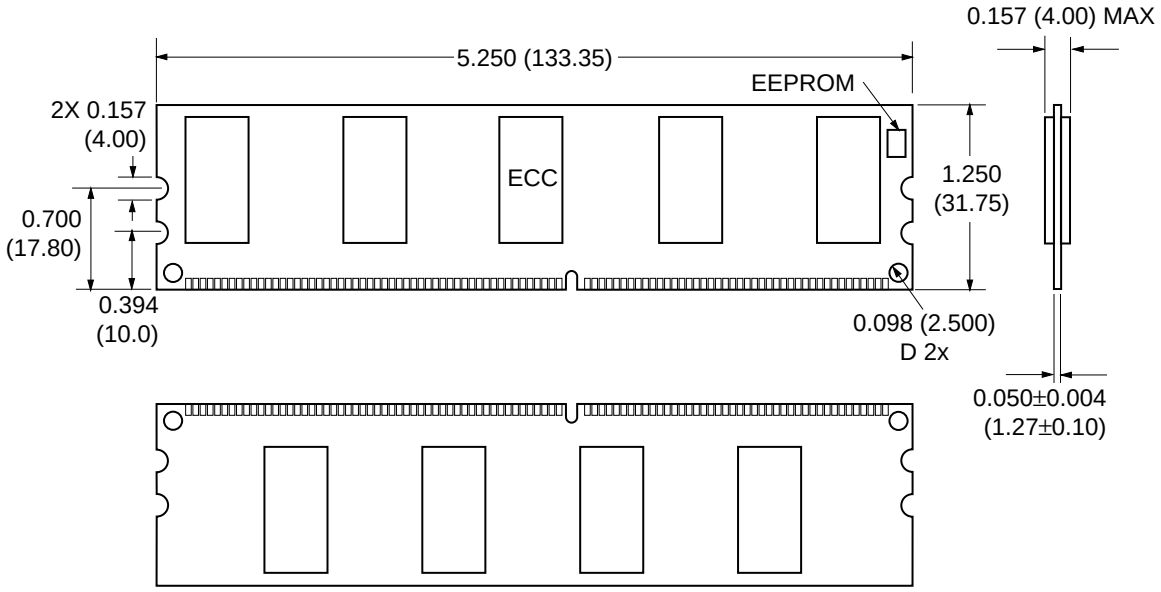
The module is available in three component options: PC266A, PC266B, and PC200. The module is PC1600 or PC2100 compliant.

ORDERING INFORMATION

Part Number	CL	MHz	Bandwidth
SL72C8D8M4M-A75DW	2	133	2.1 GB/s
SL72C8D8M4M-A75EW	2.5	133	2.1 GB/s
SL72C8D8M4M-A10DW	2	100	1.6 GB/s

PACKAGE DIMENSIONS

Units are in inches (millimeters). Tolerances are ±0.005 (±0.15) unless otherwise specified.



* "Preliminary" indicates that this product is in design. Parameters may change.

TBD

PIN CONFIGURATION (*=Not Used; /=Active Low)

Pinout

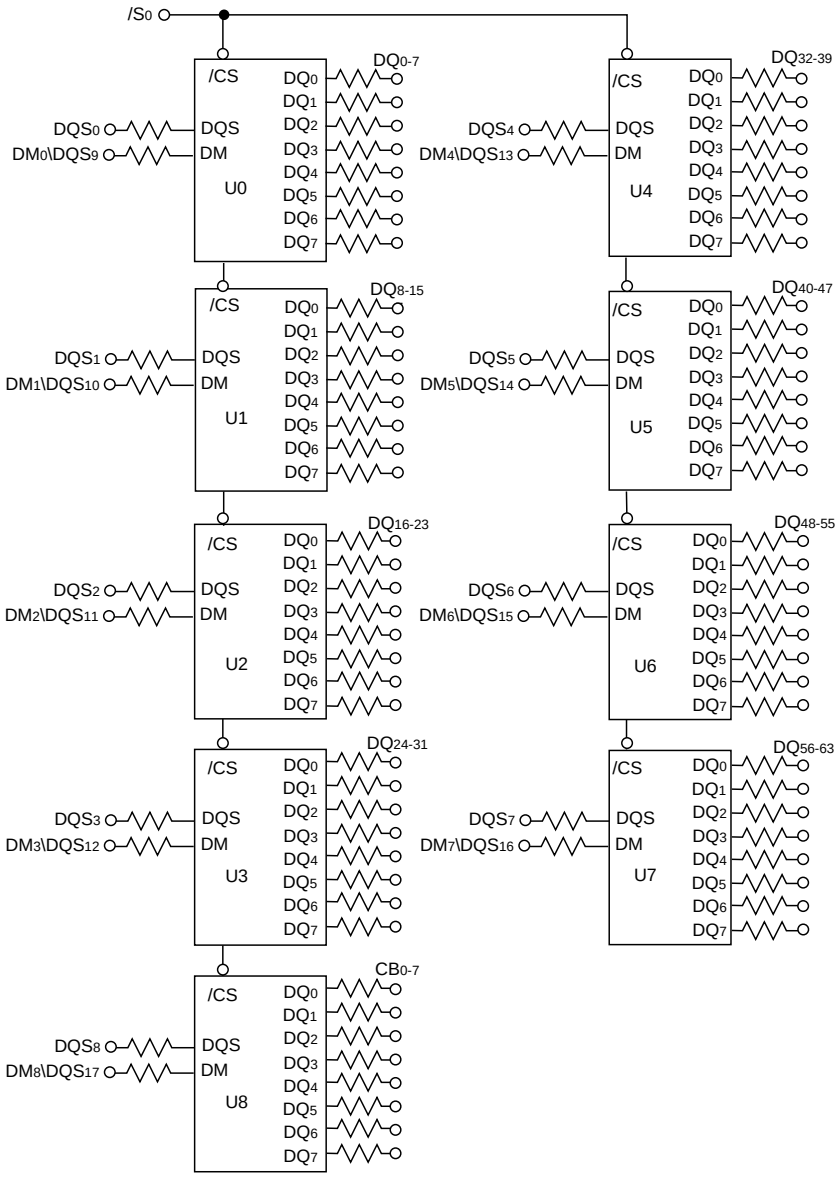
Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	93	V_{SS}	32	A_5	124	V_{SS}	62	V_{DDQ}	154	/RAS
2	DQ_0	94	DQ_4	33	DQ_{24}	125	A_6	63	/WE	155	DQ_{45}
3	V_{SS}	95	DQ_5	34	V_{SS}	126	DQ_{28}	64	DQ_{41}	156	V_{DDQ}
4	DQ_1	96	V_{DDQ}	35	DQ_{25}	127	DQ_{29}	65	/CAS	157	$/S_0$
5	DQS_0	97	DM_0\DQS_9	36	DQS_3	128	V_{DDQ}	66	V_{SS}	158	$/S_1$*
6	DQ_2	98	DQ_6	37	A_4	129	DM_3\DQS_{12}	67	DQS_5	159	DM_5\DQS_{14}
7	V_{DD}	99	DQ_7	38	V_{DD}	130	A_3	68	DQ_{42}	160	V_{SS}
8	DQ_3	100	V_{SS}	39	DQ_{26}	131	DQ_{30}	69	DQ_{43}	161	DQ_{46}
9	NC	101	NC	40	DQ_{27}	132	V_{SS}	70	V_{DD}	162	DQ_{47}
10	/RESET*	102	NC	41	A_2	133	DQ_{31}	71	$/S_2$*	163	$/S_3$*
11	V_{SS}	103	A_{13}*	42	V_{SS}	134	CB_4	72	DQ_{48}	164	V_{DDQ}
12	DQ_8	104	V_{DDQ}	43	A_1	135	CB_5	73	DQ_{49}	165	DQ_{52}
13	DQ_9	105	DQ_{12}	44	CB_0	136	V_{DDQ}	74	V_{SS}	166	DQS_3
14	DQS_1	106	DQ_{13}	45	CB_1	137	CK_0	75	CK_2	167	FETEN*
15	V_{DDQ}	107	DM_1\DQS_{10}	46	V_{DD}	138	$/CK_0$	76	$/CK_2$	168	V_{DD}
16	CK_1	108	V_{DD}	47	DQS_8	139	V_{SS}	77	V_{DDQ}	169	DM_6\DQS_{15}
17	$/CK_1$	109	DQ_{14}	48	A_0	140	DM_8\DQS_{17}	78	DQS_6	170	DQ_{54}
18	V_{SS}	110	DQ_{15}	49	CB_2	141	A_{10}	79	DQ_{50}	171	DQ_{55}
19	DQ_{10}	111	CKE_1*	50	V_{SS}	142	CB_6	80	DQ_{51}	172	V_{DDQ}
20	DQ_{11}	112	V_{DDQ}	51	CB_3	143	V_{DDQ}	81	V_{SS}	173	NC
21	CKE_0	113	BA_2*	52	BA_1	144	CB_7	82	V_{DDID}*	174	DQ60
22	V_{DDQ}	114	DQ_{20}		**Key**		**Key**	83	DQ_{56}	175	DQ_{61}
23	DQ_{16}	115	A_{12}*	53	DQ_{32}	145	V_{SS}	84	DQ_{57}	176	V_{SS}
24	DQ_{17}	116	V_{SS}	54	V_{DDQ}	146	DQ_{36}	85	V_{DD}	177	DM_7\DQS_{16}
25	DQS_2	117	DQ_{21}	55	DQ_{33}	147	DQ_{37}	86	DQS_7	178	DQ_{62}
26	V_{SS}	118	A_{11}	56	DQS_4	148	V_{DD}	87	DQ_{58}	179	DQ_{63}
27	A_9	119	DM_2\DQS_{11}	57	DQ_{34}	149	DM_4\DQS_{13}	88	DQ_{59}	180	V_{DDQ}
28	DQ_{18}	120	V_{DD}	58	V_{SS}	150	DQ_{38}	89	V_{SS}	181	SA_0
29	A_7	121	DQ_{22}	59	BA_0	151	DQ_{39}	90	NC	182	SA_1
30	V_{DDQ}	122	A_8	60	DQ_{35}	152	V_{SS}	91	SDA	183	SA_2
31	DQ_{19}	123	DQ_{23}	61	DQ_{40}	153	DQ_{44}	92	SCL	184	V_{DDSPD}

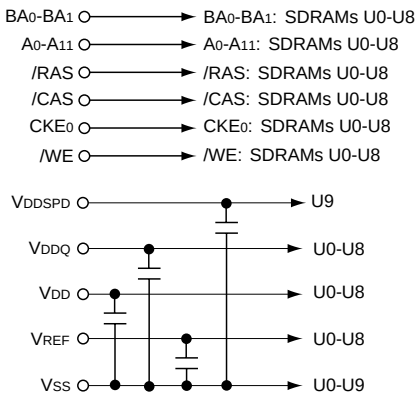
Pin Description

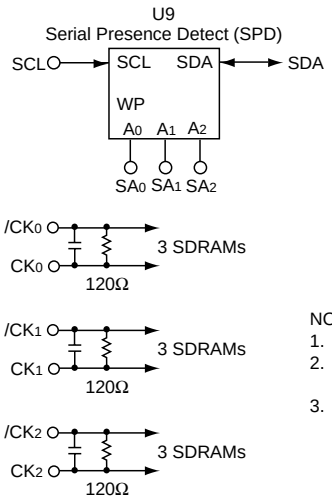
Pin Symbol	Pin Description
A_0-A_{11}, A_{12}*,A_{13}*	SDRAM address bus
BA_0-BA_1, BA_2*	SDRAM bank select
DQ_0-DQ_{63}	DIMM memory data bus
CB_0-CB_7	DIMM ECC check bits
/RAS	SDRAM row address strobe
/CAS	SDRAM column address strobe
/WE	SDRAM write strobe
$/S_0$, $/S_1$*, $/S_2$*, $/S_3$*	SDRAM chip select lines (Physical banks 0, 1, 2, and 3)
CKE_0, CKE_1*	SDRAM clock enable lines
DQS_0-DQS_8	SDRAM low data strobes
$DM_{(0-8)}$\$DQS_{(9-17)}$	SDRAM low data masks\high data strobes (x4, x8-based x72 DIMMs)
V_{DDID}*	V_{DD} Identification flag
CK_0, CK_1, CK_2	SDRAM clock (positive line of differential pair)

Pin Symbol	Pin Description
$/CK_0$, $/CK_1$, $/CK_2$	SDRAM clock (negative line of differential pair)
SCL	IIC serial bus clock for EEPROM
SDA	IIC serial bus data line for EEPROM
SA_0-SA_2	IIC slave address select for EEPROM
V_{DD}	SDRAM positive power supply
V_{DDQ}	SDRAM I/O driver positive power supply
V_{REF}	SDRAM I/O reference supply
V_{SS}	Power supply return (ground)
V_{DDSPD}	Serial EEPROM positive power supply (2.5 volts)
NC	Spare pins (no connect)
/RESET*	Reset pin (forces register inputs low)
FETEN*	FET enable line

FUNCTIONAL BLOCK DIAGRAM







NOTES:
1. DQ wiring may changed within a byte.
2. DQ, DQS, DM, CKE, /S relationships must be maintained as shown.
3. DQ, DQS, and DM resistors are 22Ω.

SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: IIC; Current sink capability of SDA driver ≤ 3mA; Maximum clock frequency: 100 KHz

Byte #	Function Described	Function Supported			Hex Value		
		PC266A	PC266B	PC200	PC266A	PC266B	PC200
0	# of bytes written into serial memory at module manufacturer	128 bytes			80h		
1	Total # of bytes of SPD memory device	256Bytes (2K-bit)			08h		
2	Fundamental memory type	DDR SDRAM			07h		
3	# of row addresses on this assembly	12			0Ch		
4	# of column addresses on this assembly	9			09h		
5	# of physical banks on this assembly	1 bank			01h		
6	Data width of this assembly	72 bits			48h		
7	…Data width of this assembly (continued)	—			00h		
8	Voltage interface level of this assembly	SSTL 2.5V			04h		
9	SDRAM cycle time at CL=2.5 (t_{CYC})	7ns	7.5ns	8ns	70h	75h	80h
10	SDRAM access time from clock at CL=2.5 (t_{AC})	0.75ns	0.75ns	0.8ns	75h	75h	80h
11	DIMM configuration type	ECC			02h		
12	Refresh rate/type	15.625µs, Self -refresh			80h		
13	SDRAM width	8 bits			08h		
14	Error Checking SDRAM data width	8 bits			08h		
15	Min. CLK delay for back-to-back rand. col. addr.	t_{CCD}=1 CLK			01h		
16	SDRAM device attributes: burst lengths supported	2,4,8			0Eh		
17	SDRAM device attributes: # of banks on SDRAM device	4 banks			04h		
18	SDRAM device attributes: CAS latency	CAS latency = 2.0, 2.5			0Ch		
19	SDRAM device attributes: CS latency	CS latency = 0			01h		
20	SDRAM device attributes: Write latency	Write Latency = 1			02h		
21	SDRAM module attributes	Differential clock			20h		
22	SDRAM device attributes: general	V_{DD}±0.2V			00h		
23	Minimum clock cycle time at CL=2 (t_{CYC})	7.5ns	8ns	10ns	75h	80h	10h
24	Max. data access time form clock at CL=2 (t_{AC})	0.75ns	0.75ns	0.8ns	75h	75h	80h
25	Minimum clock cycle time at CL=1.5 (t_{CYC})	N/A			00h		
26	Max. data access time from clock at CL=1.5 (t_{AC})	N/A			00h		
27	Minimum row precharge time (t_{RP})	20.0ns			50h		
28	Minimum row active to row active delay (t_{RRD})	15.0ns			3Ch		
29	Minumum RAS to CAS (t_{RCD})	20.0ns			50h		
30	Minumum RAS pulse width (t_{RAS})	45ns	45ns	50ns	2Dh	2Dh	32h
31	Module bank density	64MB			10h		
32	Min. command and address signal setup time (t_{AS})	1.1ns	1.1ns	1.2ns	E0h	E0h	C0h
33	Min. command and address signal hold time (t_{AH})	1.1ns	1.1ns	1.2ns	E0h	E0h	C0h
34	Min. data/data mask signal input setup time (t_{DS})	0.5ns	0.5ns	0.6ns	50h	50h	60h
35	Min. data/data mask signal input hold time (t_{DH})	0.5ns	0.5ns	0.6ns	50h	50h	60h

continued on the next page

Byte #	Function Described	Function Supported			Hex Value		
		PC266A	PC266B	PC200	PC266A	PC266B	PC200
36-61	Superset information (may be used in future)	no superset			00h		
62	SPD revision	JEDEC 1			00h		
63	Checksum for bytes 0-62	JEDEC calculation			xxh		
64	Manufacturer's JEDEC ID code per JEP-106E	Continuation code			7Fh		
65	Man. JEDEC ID code (continued)	SiliconTech's ID			A8h		
66-71					00h		
72	Manufacturing location	SiliconTech USA			01h		
73-90	Manufacturer's part number				xxh		
91	Revision code of PCB	Eng(00),RevA(01),RevB(02)			01h		
92					00h		
93	Manufacturing date	Year (BCD)			yy		
94		Calender Week (BCD)			ww		
95	Assembly serial number	Tester number			ss		
96		Serial number (bits 7-0)			ss		
97		Serial number (bits 15-8)			ss		
98		Serial number (bits 23-16)			ss		
99	Manufacture's specific data	S			53h		
100		i			69h		
101		l			6Ch		
102		i			69h		
103		c			63h		
104		o			6Fh		
105		n			6Eh		
106		T			54h		
107		e			65h		
108		c			63h		
109		h			68h		
110-127	Reserved	Undefined			00h		
128-255	Open for Customer Use	Undefined			FFh		