4M X 32 Bits DRAM 72-Pin SO-DIMM EDO Memory Module

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- Extended Data Out (EDO) Mode operation called hyper page mode
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5.0V ± 10% power supply
- 2048 cycles/32ms refresh
- JEDEC standard pinout
- Gold edge connectors

GENERAL DESCRIPTION

The SiliconTech SL32D4B4M2E-A60 is a 4M x 32 bits Dynamic RAM (DRAM) Small Outline Dual Inline Memory Module (SO-DIMM) . This module consists of eight CMOS 4M x 4 bits DRAMs in 24-pin TSOP packages mounted on a 72-pin glass epoxy substrate. Eight 0.1µF decoupling capacitors are mounted for the DRAMs.

The module has gold edge connectors intended for mounting into 72-pin SO-DIMM edge connector sockets. The module is keyed for 5V Power Supply.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{12}	49	DQ_{18}
2	DQ_0	26	DQ_{13}	50	DQ_{19}
3	DQ_1	27	DQ_{14}	51	DQ_{20}
4	DQ_2	28	A_7	52	DQ_{21}
5	DQ_3	29	NC	53	DQ_{22}
6	DQ_4	30	V_{CC}	54	DQ_{23}
7	DQ_5	31	A_8	55	NC
8	DQ_6	32	A_9	56	DQ_{24}
9	DQ_7	33	NC	57	DQ_{25}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{26}
11	PD_1	35	DQ_{15}	59	DQ_{28}
12	A_0	36	NC	60	DQ_{27}
13	A_1	37	DQ_{16}	61	V_{CC}
14	A_2	38	DQ_{17}	62	DQ_{29}
15	A_3	39	V_{SS}	63	DQ_{30}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{31}
17	A_5	41	$\overline{CAS}_2$	65	NC
18	A_6	42	$\overline{CAS}_3$	66	PD_2
19	A_{10}	43	$\overline{CAS}_1$	67	PD_3
20	NC	44	$\overline{RAS}_0$	68	PD_4
21	DQ_8	45	NC	69	PD_5
22	DQ_9	46	NC	70	PD_6
23	DQ_{10}	47	$\overline{W}$	71	PD_7
24	DQ_{11}	48	NC	72	V_{SS}

Pin Names

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_7	Presence Detect
V_{CC}	Power (+5.0V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins

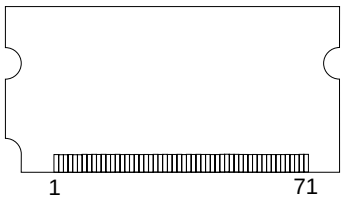
For 4Mx32 Configuration with 4Mx4, 2K DRAM Components:
PD_1=NC, PD_2=NC, PD_3=V_{SS}, PD_4=NC

Speed 60ns:
PD_5=NC, PD_6=NC

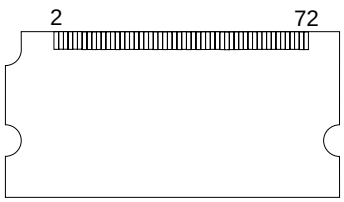
Normal Refresh:
PD_7=NC

Pin Locations

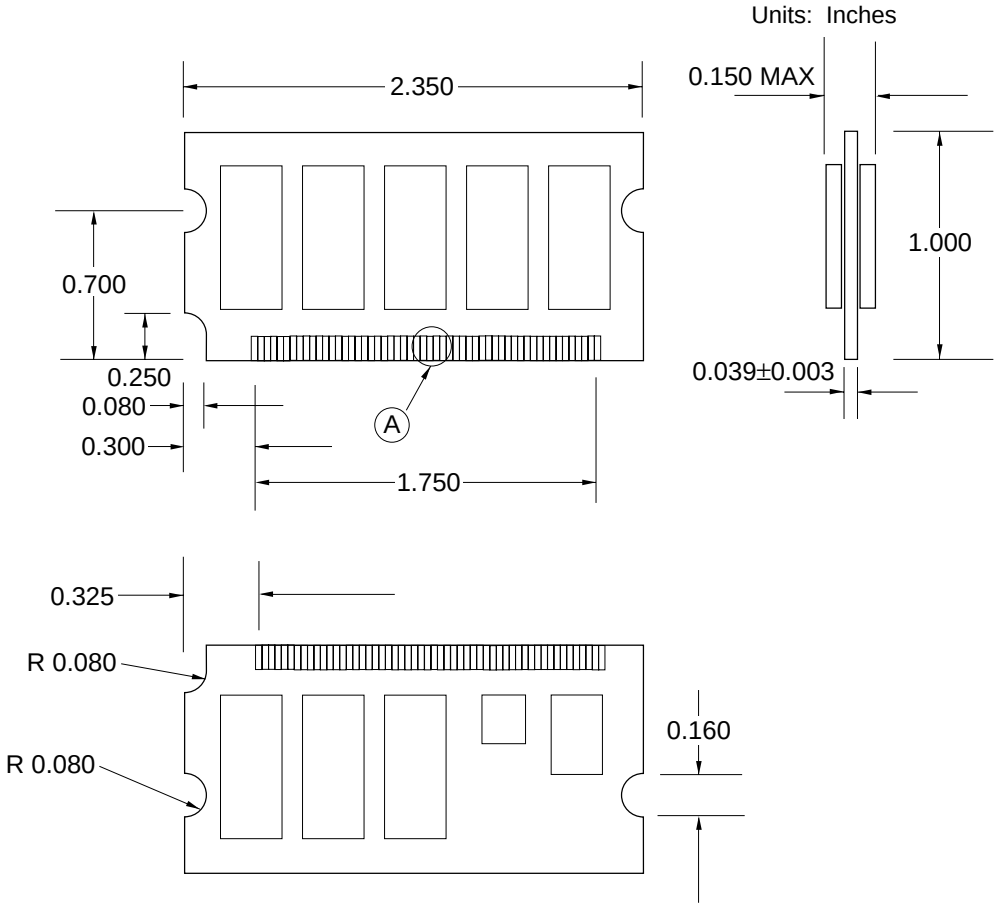
Odd numbered pins from pin 1 to pin 71 on front

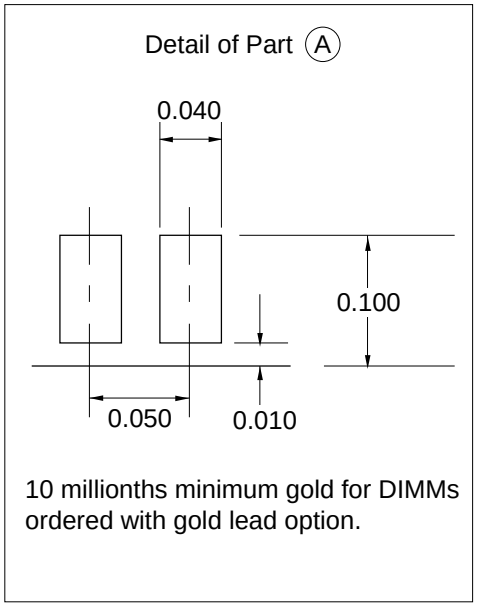


Even numbered pins from pin 2 to pin 72 on back



PACKAGE DIMENSIONS





TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

FUNCTIONAL BLOCK DIAGRAM