

## 64M X 64 Bits (512MB) SDRAM 168-Pin Unbuffered DIMM (PC100)

### FEATURES

- PC100/Intel compliant (see *Ordering Information*)
- Burst Mode Operation
- Auto and self refresh capability (4096 cycles/64ms refresh)
- LVTTTL compatible inputs and outputs
- +3.3V  $\pm$  0.3V power supply
- MRS cycle with address key programs
  - CAS Latency (CL=2 and 3)
  - Burst Length (1, 2, 4, 8, and full page)
  - Burst Type (sequential and interleave)
- All inputs are sampled at the positive going edge of the system clock
- Serial Presence Detect with EEPROM

### GENERAL DESCRIPTION

The SiliconTech SL64U4J64M4G-A10xV is a 64M x 64 bits Synchronous Dynamic RAM (SDRAM) Dual In-line Memory Module (DIMM).

This module consists of sixteen 16M x 4 bits x 4 banks IC Towers mounted on on a 168-pin glass epoxy substrate. Each IC Tower consists of two CMOS 8M x 4 bits x 4 banks SDRAMs in 54-pin 400-mil TSOP-II packages. The IC Tower stacking technology is patented by SiliconTech under patent number 5,514,907.

A serial EEPROM using the two pin I<sup>2</sup>C protocol is mounted to provide for the Serial Presence Detects (SPD). Decoupling capacitors of 0.1 $\mu$ F and 0.33 $\mu$ F are also mounted. Damping resistors are added to all the data lines. PLL circuits supply clocks to the SDRAMs.

The module has gold edge connections and is intended for mounting into 168-pin DIMM edge connector sockets keyed for unbuffered signals and 3.3V power supply.

### PIN CONFIGURATION

#### Pin Symbols

| Pin | Symbol | Pin | Symbol            | Pin | Symbol | Pin | Symbol | Pin | Symbol            | Pin | Symbol            | Pin | Symbol |
|-----|--------|-----|-------------------|-----|--------|-----|--------|-----|-------------------|-----|-------------------|-----|--------|
| 1   | VSS    | 25  | NC                | 49  | VDD    | 73  | VDD    | 97  | DQ41              | 121 | A9                | 145 | NC     |
| 2   | DQ0    | 26  | VDD               | 50  | NC     | 74  | DQ28   | 98  | DQ42              | 122 | BA0               | 146 | VREF*  |
| 3   | DQ1    | 27  | $\overline{WE}$   | 51  | NC     | 75  | DQ29   | 99  | DQ43              | 123 | A11               | 147 | NC     |
| 4   | DQ2    | 28  | DQM0              | 52  | CB2*   | 76  | DQ30   | 100 | DQ44              | 124 | VDD               | 148 | VSS    |
| 5   | DQ3    | 29  | DQM1              | 53  | CB3*   | 77  | DQ31   | 101 | DQ45              | 125 | CLK1              | 149 | DQ53   |
| 6   | VDD    | 30  | $\overline{CS}_0$ | 54  | VSS    | 78  | VSS    | 102 | VDD               | 126 | A12*              | 150 | DQ54   |
| 7   | DQ4    | 31  | DU                | 55  | DQ16   | 79  | CLK2   | 103 | DQ46              | 127 | VSS               | 151 | DQ55   |
| 8   | DQ5    | 32  | VSS               | 56  | DQ17   | 80  | NC     | 104 | DQ47              | 128 | CKE0              | 152 | VSS    |
| 9   | DQ6    | 33  | A0                | 57  | DQ18   | 81  | WP     | 105 | CB4*              | 129 | $\overline{CS}_3$ | 153 | DQ56   |
| 10  | DQ7    | 34  | A2                | 58  | DQ19   | 82  | SDA    | 106 | CB5*              | 130 | DQM6              | 154 | DQ57   |
| 11  | DQ8    | 35  | A4                | 59  | VDD    | 83  | SCL    | 107 | VSS               | 131 | DQM7              | 155 | DQ58   |
| 12  | VSS    | 36  | A6                | 60  | DQ20   | 84  | VDD    | 108 | NC                | 132 | A13*              | 156 | DQ59   |
| 13  | DQ9    | 37  | A8                | 61  | NC     | 85  | VSS    | 109 | NC                | 133 | VDD               | 157 | VDD    |
| 14  | DQ10   | 38  | A10/AP            | 62  | VREF*  | 86  | DQ32   | 110 | VDD               | 134 | NC                | 158 | DQ60   |
| 15  | DQ11   | 39  | BA1               | 63  | CKE1   | 87  | DQ33   | 111 | $\overline{CAS}$  | 135 | NC                | 159 | DQ61   |
| 16  | DQ12   | 40  | VDD               | 64  | VSS    | 88  | DQ34   | 112 | DQM4              | 136 | CB6*              | 160 | DQ62   |
| 17  | DQ13   | 41  | VDD               | 65  | DQ21   | 89  | DQ35   | 113 | DQM5              | 137 | CB7*              | 161 | DQ63   |
| 18  | VDD    | 42  | CLK0              | 66  | DQ22   | 90  | VDD    | 114 | $\overline{CS}_1$ | 138 | VSS               | 162 | VSS    |
| 19  | DQ14   | 43  | VSS               | 67  | DQ23   | 91  | DQ36   | 115 | $\overline{RAS}$  | 139 | DQ48              | 163 | CLK3   |
| 20  | DQ15   | 44  | DU                | 68  | VSS    | 92  | DQ37   | 116 | VSS               | 140 | DQ49              | 164 | NC     |
| 21  | CB0*   | 45  | $\overline{CS}_2$ | 69  | DQ24   | 93  | DQ38   | 117 | A1                | 141 | DQ50              | 165 | SA0    |
| 22  | CB1*   | 46  | DQM2              | 70  | DQ25   | 94  | DQ39   | 118 | A3                | 142 | DQ51              | 166 | SA1    |
| 23  | VSS    | 47  | DQM3              | 71  | DQ26   | 95  | DQ40   | 119 | A5                | 143 | VDD               | 167 | SA2    |
| 24  | NC     | 48  | DU                | 72  | DQ27   | 96  | VSS    | 120 | A7                | 144 | DQ52              | 168 | VDD    |

\*These pins are not used in this module.

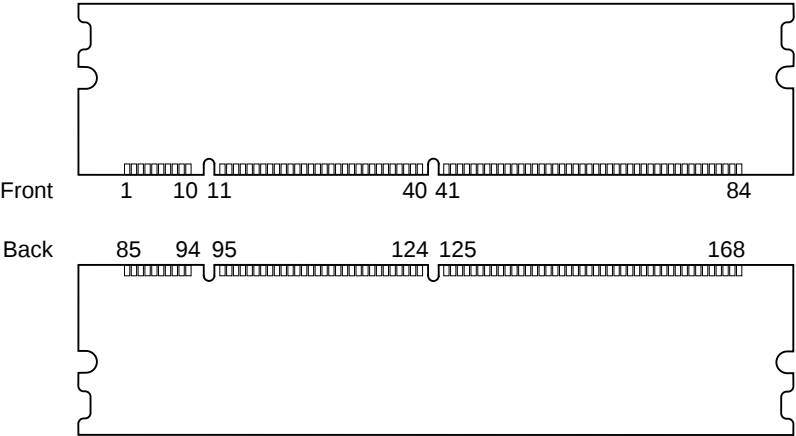
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PIN CONFIGURATION *(continued)*

Pin Functions

| Pin Symbol                                             | Pin Function           |
|--------------------------------------------------------|------------------------|
| A0-A10/AP, A11                                         | Address Inputs         |
| BA0, BA1                                               | Select Bank            |
| DQ0-DQ63                                               | Data In/Out            |
| $\overline{\text{WE}}$                                 | Write Enable           |
| CLK0-CLK3                                              | Clock Input            |
| CKE0, CKE1                                             | Clock Enable Input     |
| $\overline{\text{RAS}}$                                | Row Address Strobe     |
| $\overline{\text{CAS}}$                                | Column Address Strobe  |
| DQM0-DQM7                                              | Data Input/Output Mask |
| $\overline{\text{CS}}_0\text{-}\overline{\text{CS}}_3$ | Chip Select Input      |
| SDA                                                    | Serial Data I/O        |
| SCL                                                    | Serial Clock           |
| SA0-SA2                                                | Address in EEPROM      |
| WP                                                     | EEPROM Write Protect   |
| VDD                                                    | Power (+3.3V)          |
| VSS                                                    | Ground                 |
| NC                                                     | No Connection          |
| DU                                                     | Don't Use              |

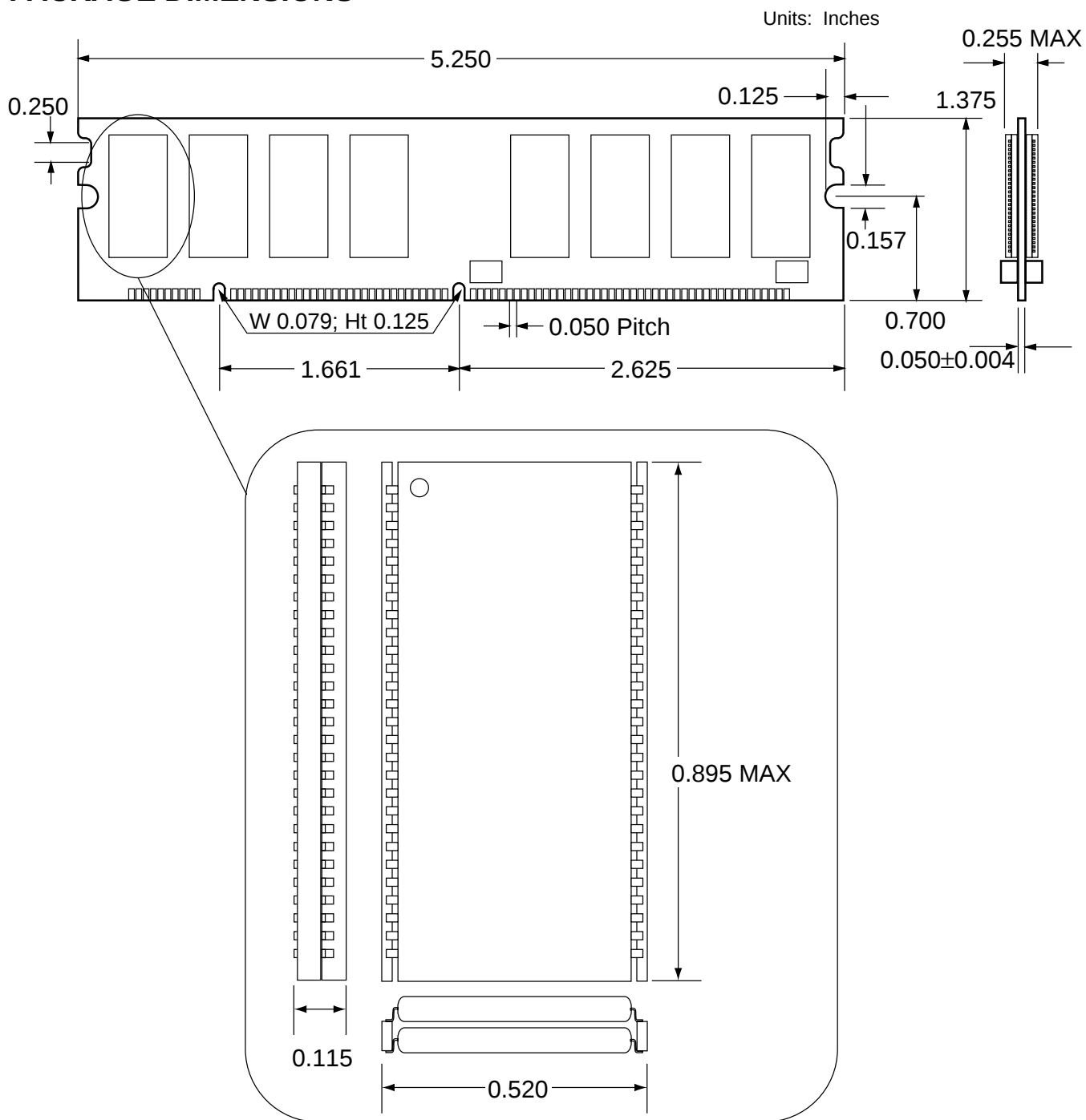
Pin Arrangement



ORDERING INFORMATION

| Part Number        | PC100 100MHz Parameters |      |     |     |       |                                |
|--------------------|-------------------------|------|-----|-----|-------|--------------------------------|
|                    | CL                      | tRCD | tRP | tRC | Units | Comment                        |
| SL64U4J64M4G-A10AV | 3                       | 3    | 3   | 8   | clks  | slowest supported (option "A") |
| SL64U4J64M4G-A10DV | 2                       | 2    | 2   | 7   | clks  | goal (option "D")              |

## PACKAGE DIMENSIONS



640A

TOLERANCES:  $\pm 0.005$  UNLESS OTHERWISE SPECIFIED

## SERIAL PRESENCE DETECT INFORMATION

Serial PD Interface Protocol: I<sup>2</sup>C; Current sink capability of SDA driver ≤ 3mA; Maximum clock frequency: 100 KHz

| Byte # | Function Described                                           | Function Supported               |      | Hex Value |     |
|--------|--------------------------------------------------------------|----------------------------------|------|-----------|-----|
|        |                                                              | A                                | D    | A         | D   |
| 0      | # of bytes written into serial memory at module manufacturer | 128 bytes                        |      | 80h       |     |
| 1      | Total # of bytes of SPD memory device                        | 256Bytes (2K-bit)                |      | 08h       |     |
| 2      | Fundamental memory type                                      | SDRAM                            |      | 04h       |     |
| 3      | # of row addresses on this assembly                          | 12                               |      | 0Ch       |     |
| 4      | # of column addresses on this assembly                       | 11                               |      | 0Bh       |     |
| 5      | # of module banks on this assembly                           | 2 banks                          |      | 02h       |     |
| 6      | Data width of this assembly                                  | 64 bits                          |      | 40h       |     |
| 7      | ...Data width of this assembly (continued)                   | —                                |      | 00h       |     |
| 8      | Voltage interface standard of this assembly                  | LVTTL                            |      | 01h       |     |
| 9      | SDRAM cycle time at CL=3 (tCYC)                              | 10ns                             | 10ns | A0h       | A0h |
| 10     | SDRAM access time from clock at CL=3 (tAC)                   | 6ns                              | 6ns  | 60h       | 60h |
| 11     | DIMM configuration type                                      | None                             |      | 00h       |     |
| 12     | Refresh rate/type                                            | 15.625μs, Self-refresh           |      | 80h       |     |
| 13     | SDRAM width                                                  | 4 bits                           |      | 04h       |     |
| 14     | Error Checking DRAM data width                               | None                             |      | 00h       |     |
| 15     | Min. CLK delay for back-to-back rand. col. addr.             | tCCD=1 CLK                       |      | 01h       |     |
| 16     | SDRAM device attributes: burst lengths supported             | 1,2,4,8, and full page           |      | 8Fh       |     |
| 17     | SDRAM device attributes: # of banks on SDRAM device          | 4 banks                          |      | 04h       |     |
| 18     | SDRAM device attributes: CAS latency                         | CAS latency = 2,3                |      | 06h       |     |
| 19     | SDRAM device attributes: CS latency                          | CS latency = 0                   |      | 01h       |     |
| 20     | SDRAM device attributes: Write latency                       | Write Latency = 0                |      | 01h       |     |
| 21     | SDRAM module attributes                                      | on-card PLL, non-buff., non-reg. |      | 04h       |     |
| 22     | SDRAM device attributes: general                             | VCC10%, B/R, S/W, P/A, A/P       |      | 0Eh       |     |
| 23     | Minimum clock cycle time at CL=2 (tCYC)                      | 12ns                             | 10ns | C0h       | A0h |
| 24     | Max. data access time form clock at CL=2 (tAC)               | 8ns                              | 6ns  | 80h       | 60h |
| 25     | Minimum clock cycle time at CL=1 (tCYC)                      | —                                | —    | 00h       | 00h |
| 26     | Max. data access time from clock at CL=1 (tAC)               | —                                | —    | 00h       | 00h |
| 27     | Minimum row precharge time (tRP)                             | 30ns                             | 20ns | 1Eh       | 14h |
| 28     | Minimum row active to row active delay (tRRD)                | 20ns                             | 20ns | 14h       | 14h |
| 29     | Minumum RAS to CAS (tRCD)                                    | 30ns                             | 20ns | 1Eh       | 14h |
| 30     | Minumum RAS pulse width (tRAS)                               | 50ns                             | 50ns | 32h       | 32h |
| 31     | Module bank density                                          | 256MB                            |      | 40h       |     |
| 32     | Min. command and address signal setup time (tAS)             | 2ns                              |      | 20h       |     |
| 33     | Min. command and address signal hold time (tAH)              | 1ns                              |      | 10h       |     |
| 34     | Min. data signal input setup time (tDS)                      | 2ns                              |      | 20h       |     |

continued on the next page

| Byte #  | Function Described                                  | Function Supported         |     | Hex Value |     |
|---------|-----------------------------------------------------|----------------------------|-----|-----------|-----|
|         |                                                     | A                          | D   | A         | D   |
| 35      | Min. data signal input hold time (t <sub>DH</sub> ) | 1ns                        |     | 10h       |     |
| 36-61   | Superset information (may be used in future)        | —                          |     | 00h       |     |
| 62      | SPD revision                                        | 1.2                        | 1.2 | 12h       | 12h |
| 63      | Checksum for bytes 0-62                             | JEDEC calculation          |     | xxh       |     |
| 64      | Manufacturer's JEDEC ID code per JEP-106E           | Continuation code          |     | 7Fh       |     |
| 65      | Man. JEDEC ID code (continued)                      | SiliconTech's ID           |     | A8h       |     |
| 66-71   |                                                     |                            |     | FFh       |     |
| 72      | Manufacturing location                              | SiliconTech USA            |     | 01h       |     |
| 73-90   | Manufacturer's part number                          |                            |     | xxh       |     |
| 91      | Revision code of PCB                                | Eng(00),RevA(01),RevB(02)  |     | 01h       |     |
| 92      |                                                     |                            |     | FFh       |     |
| 93      | Manufacturing date                                  | Year (BCD)                 |     | yy        |     |
| 94      |                                                     | Calender Week (BCD)        |     | ww        |     |
| 95      | Assembly serial number                              | Tester number              |     | ss        |     |
| 96      |                                                     | Serial number (bits 7-0)   |     | ss        |     |
| 97      |                                                     | Serial number (bits 15-8)  |     | ss        |     |
| 98      |                                                     | Serial number (bits 23-16) |     | ss        |     |
| 99      | Manufacture's specific data                         | S                          |     | 53h       |     |
| 100     |                                                     | i                          |     | 69h       |     |
| 101     |                                                     | l                          |     | 6Ch       |     |
| 102     |                                                     | i                          |     | 69h       |     |
| 103     |                                                     | c                          |     | 63h       |     |
| 104     |                                                     | o                          |     | 6Fh       |     |
| 105     |                                                     | n                          |     | 6Eh       |     |
| 106     |                                                     | T                          |     | 54h       |     |
| 107     |                                                     | e                          |     | 65h       |     |
| 108     |                                                     | c                          |     | 63h       |     |
| 109     |                                                     | h                          |     | 68h       |     |
| 110     |                                                     |                            |     | FFh       |     |
| 111     |                                                     |                            |     | FFh       |     |
| 112     |                                                     |                            |     | FFh       |     |
| 113     |                                                     |                            |     | FFh       |     |
| 114     |                                                     |                            |     | FFh       |     |
| 115     |                                                     |                            |     | FFh       |     |
| 115-125 |                                                     |                            |     | FFh       |     |
| 126     | Intel specification frequency                       | 100MHz                     |     | 64h       |     |
| 127     | Intel specification details                         | Detailed 100MHz Info       |     | FFh       | FFh |

## FUNCTIONAL BLOCK DIAGRAM

