8M X 32 Bits (32MB) Simultaneous Operation Flash 80-Pin SIMM (3.3V Only)

FEATURES

- Max. access time of 90ns; $\overline{CE}$ access time of 90ns; $\overline{OE}$ access time of 40ns
- TTL compatible inputs and outputs
- 3.3V only power supply
- JEDEC standard
- Tin (option “T”) or gold (option “G”) edge connectors
- Three power on reset options
  - No power on reset: $\overline{RST}$ tied to V_{CC} (Option “V”)
  - Power on reset: $\overline{RST}$ tied to power supervisor circuit (Option “R”)
  - System control of power on reset: $\overline{RST}$ tied to pin 7 (Option “S”; this option is not JEDEC standard)
- AMD Part Number Am29DL323CB-90EI Simultaneous Operation Flash Memory components
- Industrial Temperature Range: -40°C to +85°C
- Minimum 1,000,000 write guarantee per sector

GENERAL DESCRIPTION

The SiliconTech SL29321A-90(T/G)9(V/R/S) is a 8M x 32 bits flash 80-pin Single In-line Memory Module (SIMM). This module consists of eight 4M x 8 bits/2M x 16 bits CMOS flash memory (configured as 4M x 8 bits) in 48-pin TSOP packages mounted on an 80-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are also mounted.

Option “T” provides tin edge connectors and option “G” provides gold edge connectors. Option “R” provides power on reset through a power supervisor circuit; option “S” provides system control of power on reset by connecting the reset signals to Pin 7; and, option “V” provides no power on reset.

The module is intended for mounting into 80-pin edge connector sockets. The module uses the standard programming algorithms for AMD Am29DL323CB-90EI Bottom Boot Block Simultaneous Operation Flash Memory components.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	28	DQ_{31}	55	DQ_{15}
2	V_{CC}	29	$\overline{WE}_2$	56	DQ_{14}
3	NC	30	NC	57	DQ_{13}
4	$\overline{OE}$	31	NC	58	DQ_{12}
5	$\overline{WE}_0$	32	A_{20}	59	DQ_{11}
6	$\overline{WE}_1$	33	A_{19}	60	DQ_{10}
7	NC/$\overline{RST}$	34	A_{18}	61	DQ_9
8	DQ_{16}	35	A_{17}	62	DQ_8
9	DQ_{17}	36	A_{16}	63	DQ_7
10	DQ_{18}	37	A_{15}	64	DQ_6
11	DQ_{19}	38	A_{14}	65	DQ_5
12	DQ_{20}	39	A_{13}	66	DQ_4
13	DQ_{21}	40	A_{12}	67	DQ_3
14	DQ_{22}	41	A_{11}	68	DQ_2
15	DQ_{23}	42	A_{10}	69	DQ_1
16	DQ_{24}	43	A_9	70	DQ_0
17	DQ_{25}	44	A_8	71	NC
18	DQ_{26}	45	A_7	72	V_{CC}
19	DQ_{27}	46	A_6	73	PD_1
20	DQ_{28}	47	A_5	74	PD_2
21	NC	48	A_4	75	PD_3
22	NC	49	A_3	76	PD_4
23	$\overline{CE}_1$	50	A_2	77	PD_5
24	$\overline{CE}_0$	51	A_1	78	PD_6
25	V_{SS}	52	A_0	79	PD_7
26	DQ_{29}	53	$\overline{WE}_3$	80	V_{SS}
27	DQ_{30}	54	V_{SS}		

Pin Functions

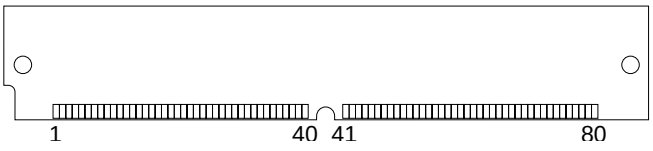
Pin Symbol	Pin Function
A_0-A_{20}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{CE}_0$, $\overline{CE}_1$	Chip Enable
$\overline{WE}_0$-$\overline{WE}_3$	Write Enable
$\overline{OE}$	Output Enable
PD_1-PD_7	Presence Detect
$\overline{RST}$	Reset
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

Pin Name	Signal
PD_1	NC
PD_2	V_{SS}
PD_3	NC
PD_4	NC
PD_5	NC
PD_6	NC
PD_7	V_{SS}

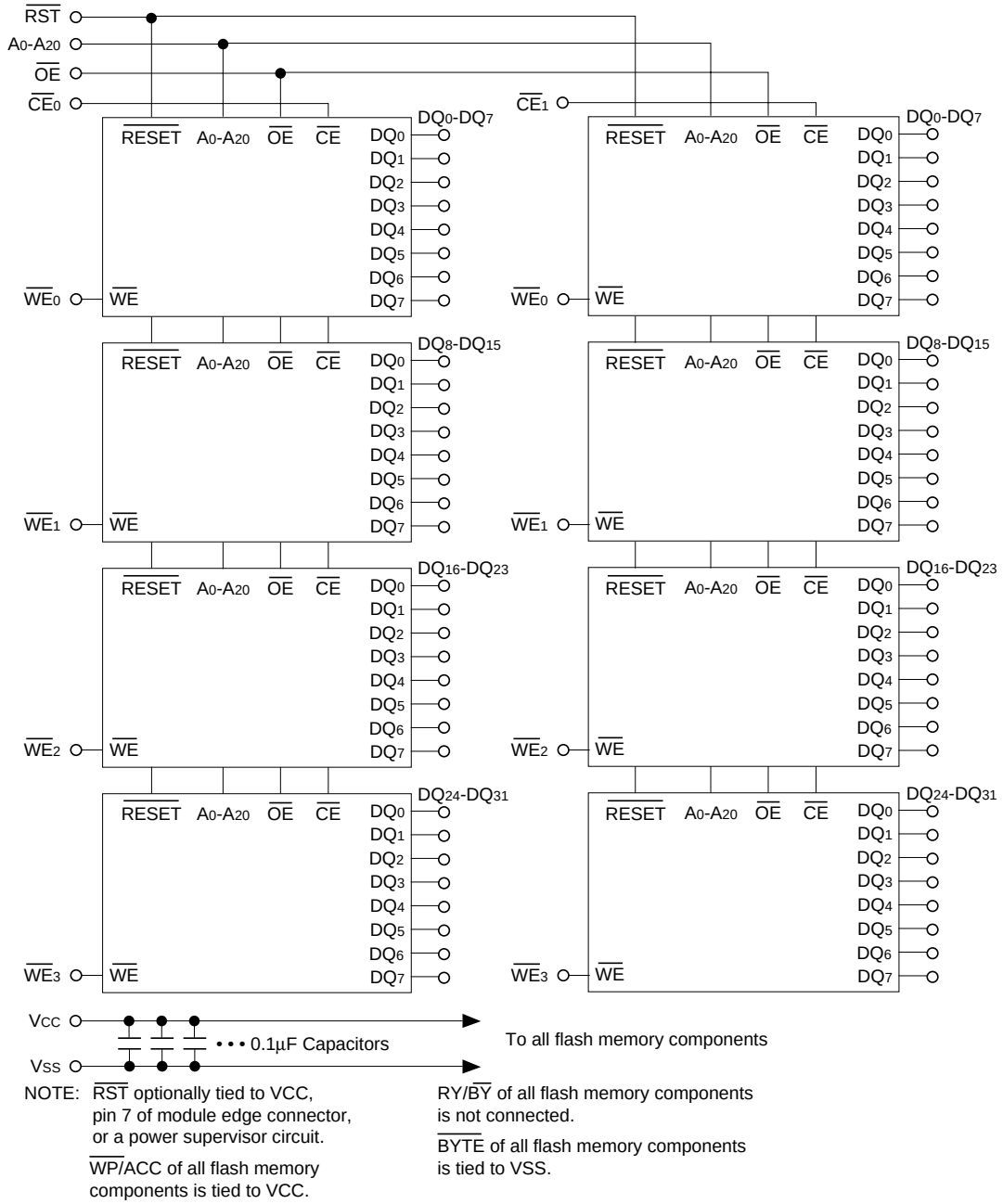
* Pin Connection Changing Available; The Presence Detects are based on the sequence of existing Presence Detects in JEDEC Standard No. 21-C page 4.4.7-3.

Pin Locations

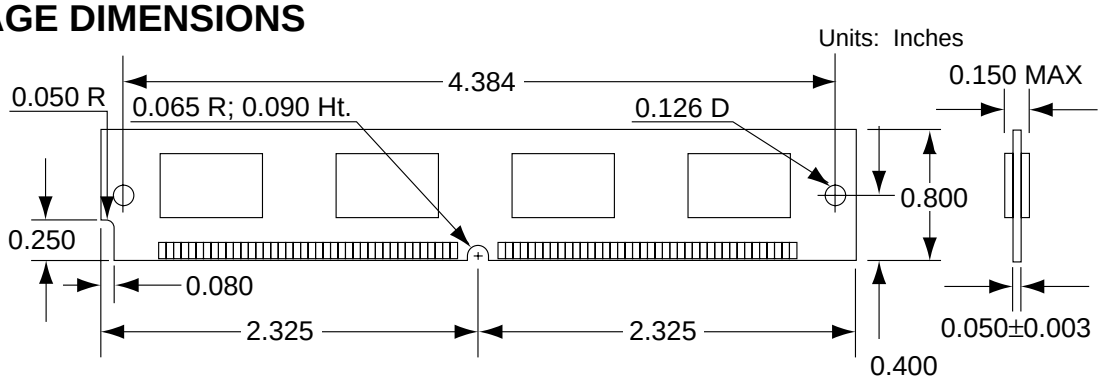


† “Advanced” indicates that this product is in consideration for development and that the product may or may not be further developed for production. All parameters may change without further notice.

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



TBD

TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED