512K X 36 Bits (2MB) Flow-Through Synchronous SRAM 144-Pin SO-DIMM

FEATURES

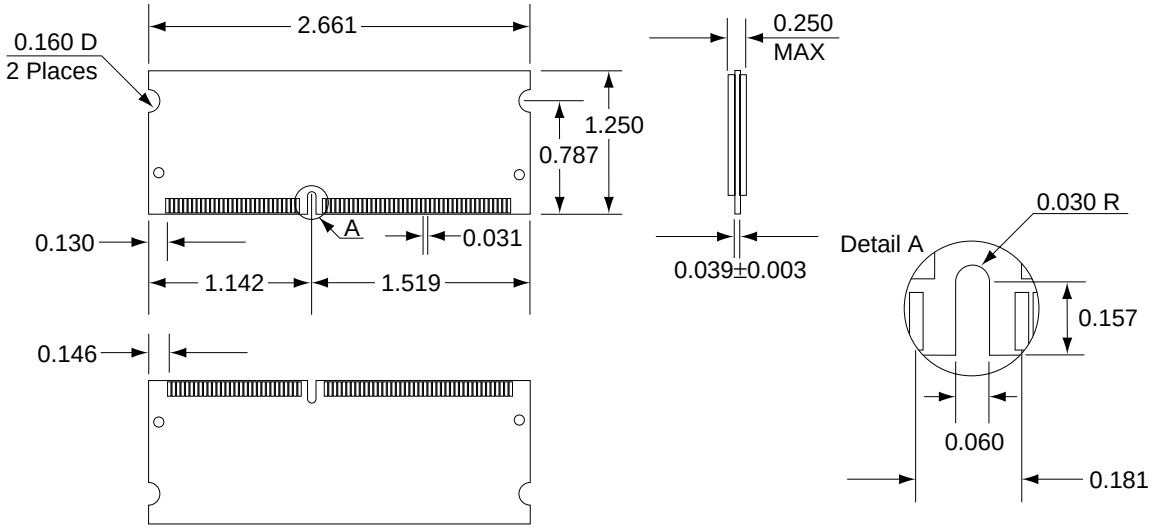
- Performance range:
  8.5ns up to 87MHz clock frequency
- +3.3V ± 0.3V power supply
- Byte write capability
- LVTLL compatible inputs and outputs
- 144-Pin SO-DIMM gold edge connectors

GENERAL DESCRIPTION

The SiliconTech SL936512K2M-09DFVG is a 512K x 36 bits synchronous Static RAM (SRAM) 144-Pin Small Outline Dual In-line Memory Module (SO-DIMM). The module consists of four 256K x 18 bits SRAM memory components in 100-pin TQFP packages mounted on a 144-pin glass epoxy substrate. Decoupling capacitors of are also mounted. The module is intended for mounting into 144-pin SO-DIMM sockets keyed for 3.3V power supply.

PACKAGE DIMENSIONS

Units: Inches



TBD

TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

* "Advanced" indicates that this product is in consideration for development and that the product may or may not be further developed for production. All parameters may change without further notice.

PIN CONFIGURATION

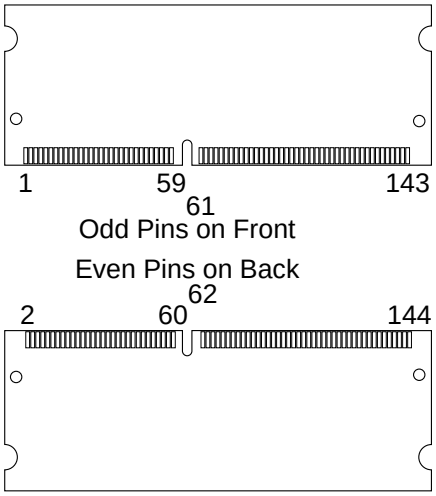
Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	21	A_{10}	41	$\overline{CS}_0$	61	V_{CC}	81	$\overline{WE}$	101	V_{SS}	121	CLK_3	141	DP_2
2	V_{SS}	22	A_{11}	42	$\overline{OE}_0$	62	V_{CC}	82	$\overline{ADS}$	102	V_{SS}	122	CLK_2	142	DP_3
3	A_0	23	NC	43	V_{SS}	63	DQ_8	83	NC	103	$\overline{BW}_2$	123	V_{SS}	143	V_{SS}
4	A_1	24	NC	44	V_{SS}	64	DQ_9	84	NC	104	$\overline{BW}_3$	124	V_{SS}	144	V_{SS}
5	A_2	25	V_{CC}	45	CLK_1	65	DQ_{10}	85	V_{CC}	105	$\overline{CS}_1$	125	DQ_{20}		
6	A_3	26	V_{CC}	46	CLK_0	66	DQ_{11}	86	V_{CC}	106	$\overline{OE}_1$	126	DQ_{21}		
7	A_4	27	A_{12}	47	V_{SS}	67	V_{SS}	87	NC	107	V_{CC}	127	V_{SS}		
8	A_5	28	A_{13}	48	V_{SS}	68	V_{SS}	88	NC	108	V_{CC}	128	V_{SS}		
9	V_{CC}	29	A_{14}	49	DQ_0	69	DQ_{12}	89	NC	109	DQ_{16}	129	DQ_{22}		
10	V_{CC}	30	A_{15}	50	DQ_1	70	DQ_{13}	90	NC	110	DQ_{17}	130	DQ_{23}		
11	RFU	31	A_{16}	51	V_{CC}	71	DQ_{14}	91	NC	111	DQ_{18}	131	DQ_{24}		
12	RFU	32	A_{17}	52	V_{CC}	72	DQ_{15}	92	NC	112	DQ_{19}	132	DQ_{25}		
13	RFU	33	V_{SS}	53	DQ_2	73	DP_0	93	V_{CC}	113	NC	133	DQ_{26}		
14	RFU	34	V_{SS}	54	DQ_3	74	DP_1	94	V_{CC}	114	NC	134	DQ_{27}		
15	V_{SS}	35	PD_1	55	DQ_4	75	RFU	95	NC	115	NC	135	DQ_{28}		
16	V_{SS}	36	PD_2	56	DQ_5	76	RFU	96	NC	116	NC	136	DQ_{29}		
17	A_6	37	V_{SS}	57	DQ_6	77	RFU	97	NC	117	NC	137	V_{CC}		
18	A_7	38	V_{SS}	58	DQ_7	78	RFU	98	NC	118	NC	138	V_{CC}		
19	A_8	39	$\overline{BW}_0$	59	V_{SS}	79	V_{SS}	99	NC	119	V_{SS}	139	DQ_{30}		
20	A_9	40	$\overline{BW}_1$	60	V_{SS}	80	V_{SS}	100	NC	120	V_{SS}	140	DQ_{31}		

Pin Functions

Pin Name	Pin Function
A_0-A_{17}	Address Inputs
DQ_0-DQ_{31}	Data Inputs/Outputs
DP_0-DP_3	Data Parity I/O
$\overline{CS}_0$, $\overline{CS}_1$	Chip Select Inputs
$\overline{OE}_0$, $\overline{OE}_1$	Output Enable Inputs
$\overline{BW}_0$-$\overline{BW}_3$	Write Enable Inputs
CLK_0-CLK_3	Clock Inputs
$\overline{ADS}$	Address Status Inputs
$\overline{WE}$	Global Write Inputs
PD_1, PD_2	Presence Detect Outputs
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection
RFU	Reserved for Future Use

Pin Locations



Presence Detect Pins

PD_1=NC, PD_2=NC

FUNCTIONAL BLOCK DIAGRAM