4M X 36 Bits DRAM 72-Pin SIMM with Extended Data Out (EDO) and ECC

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- EDO Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V ± 10% power supply
- 2048 cycles/32ms refresh
- Four $\overline{CAS}$ ECC pinout
- Gold or Tin edge connections

GENERAL DESCRIPTION

The SiliconTech SL36(S/T)4B4M2F-A60 is a 4M x 36 bits Dynamic RAM (DRAM) Single In-line Memory Module (SIMM). The module consists of nine CMOS 4M x 4 bits DRAMs in 24-pin 300-mil SOJ packages mounted on a 72-pin glass epoxy substrate. Decoupling capacitors of 0.1μF are also mounted.

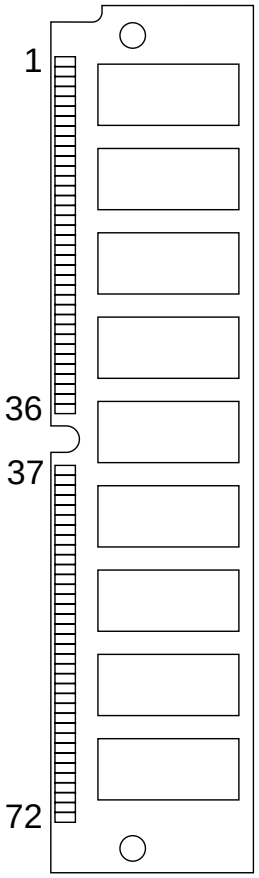
The SL36T4B4M2F-A60 has tin edge connectors and the SL36S4B4M2F-A60 has gold edge connectors. The module is intended for mounting into 72-pin SIMM edge connector sockets with the same lead, i.e. tin or gold. The module is for use in computers using ECC without single-byte accesses.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	NC	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	A_9	56	DQ_{30}
9	DQ_{21}	33	NC	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{31}
11	NC	35	PQ_{26}	59	V_{CC}
12	A_0	36	PQ_8	60	DQ_{32}
13	A_1	37	PQ_{17}	61	DQ_{14}
14	A_2	38	PQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{34}
17	A_5	41	$\overline{CAS}_2$	65	DQ_{16}
18	A_6	42	$\overline{CAS}_3$	66	NC
19	A_{10}	43	$\overline{CAS}_1$	67	PD_1
20	DQ_4	44	$\overline{RAS}_0$	68	PD_2
21	DQ_{22}	45	NC	69	PD_3
22	DQ_5	46	NC	70	PD_4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}

Pin Locations



Pin Functions

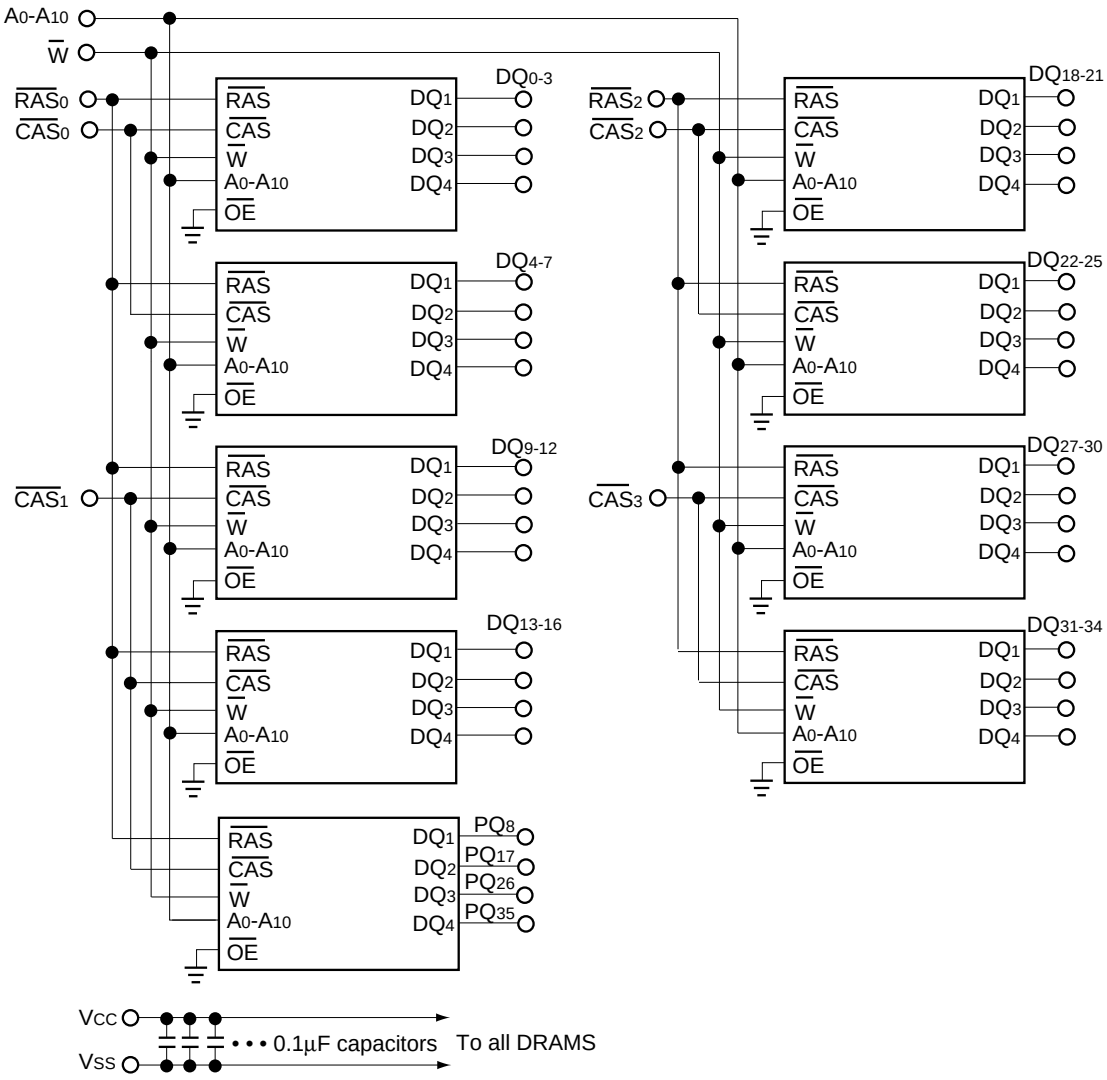
Pin Symbol	Pin Function
A_0-A_{10}	Address Inputs
DQ_x	Data In/Out
$PQ_{8,17,26,35}$	ECC In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$,$\overline{RAS}_2$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

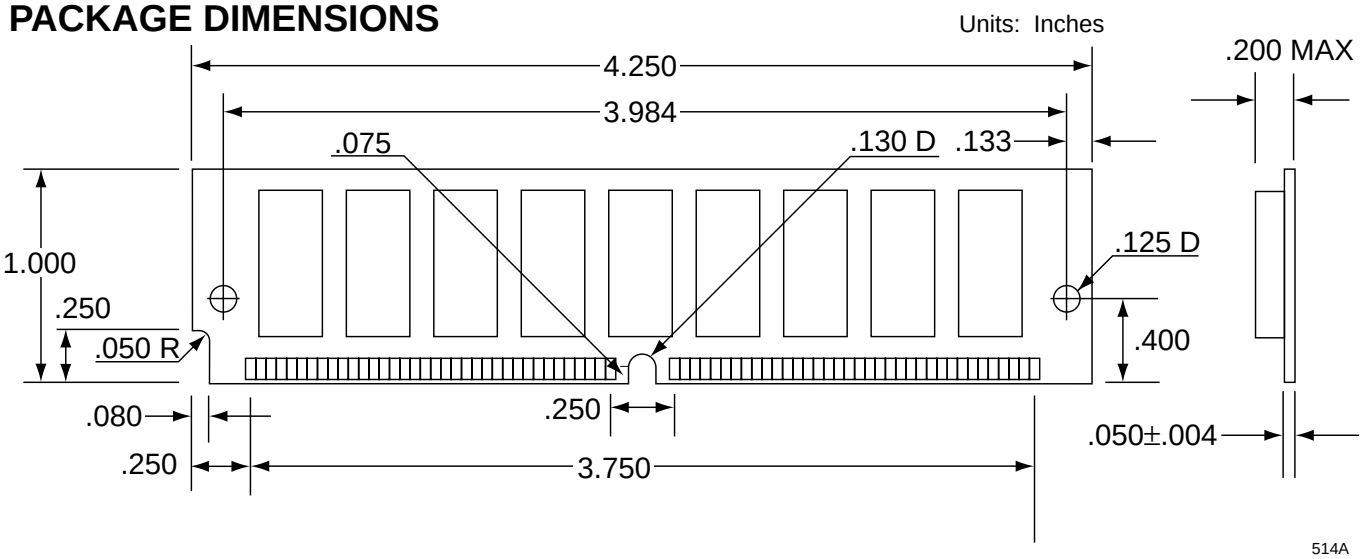
For 4Mx36 Bits Parity:
PD_1=V_{SS}
PD_2=NC
PD_3=NC
PD_4=NC

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED