1M X 32 Bits (4MB) Flash Memory Module (5V Supply; 12V Program)

FEATURES

- Access Time of 90ns
- TTL compatible inputs and outputs
- 5V V_{CC} and 12V V_{PP}
- JEDEC standard—except for no x8 operations; x16 only
- Tin (option “T”) or gold (option “G”) edge connectors
- Three power on reset options
  - No power on reset: $\overline{RST}$ tied to V_{CC} (Option “V”)
  - Power on reset: $\overline{RST}$ tied to power supervisor circuit (Option “R”)
  - System control of power on reset: $\overline{RST}$ tied to pin 7 (Option “S”; this option is not JEDEC standard)
- Intel Part Number E28F016SA-070 flash memory components

GENERAL DESCRIPTION

The SiliconTech SL29041-90(T/G)A1(R/S/V)I is a 1M x 32 bits flash memory module. The SL29041-90(T/G)A1(R/S/V)I consists of two 1M x 16 bits CMOS flash memory in 56-pin TSOP-I packages mounted on an 80-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are mounted for the flash memory.

The SL29041-90(T/G)A1(R/S/V)I is a 80-pin flash memory module with a maximum access time of 90ns and 5V power supply/12V programming. Option “T” provides tin edge connectors and option “G” provides gold edge connectors. Option “R” provides power on reset through a power supervisor circuit; option “S” provides system control of power on reset by tieing the reset signals to Pin 7; and, option “V” provides no power on reset.

The SL29041-90(T/G)A1(R/S/V)I is intended for mounting into 80-pin edge connector sockets. The SL29041-90(T/G)A1(R/S/V)I uses the standard programming algorithms for Intel E28F016SA flash memory component and is backward compatible to the 28F008SA flash memory component.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	28	DQ_{31}	55	DQ_{15}
2	V_{CC}	29	$\overline{WE}_2$	56	DQ_{14}
3	V_{PP}	30	NC	57	DQ_{13}
4	$\overline{OE}$	31	NC	58	DQ_{12}
5	$\overline{WE}_0$	32	NC	59	DQ_{11}
6	NC	33	A_{19}	60	DQ_{10}
7	NC/$\overline{RST}$	34	A_{18}	61	DQ_9
8	DQ_{16}	35	A_{17}	62	DQ_8
9	DQ_{17}	36	A_{16}	63	DQ_7
10	DQ_{18}	37	A_{15}	64	DQ_6
11	DQ_{19}	38	A_{14}	65	DQ_5
12	DQ_{20}	39	A_{13}	66	DQ_4
13	DQ_{21}	40	A_{12}	67	DQ_3
14	DQ_{22}	41	A_{11}	68	DQ_2
15	DQ_{23}	42	A_{10}	69	DQ_1
16	DQ_{24}	43	A_9	70	DQ_0
17	DQ_{25}	44	A_8	71	V_{PP}
18	DQ_{26}	45	A_7	72	V_{CC}
19	DQ_{27}	46	A_6	73	PD_1
20	DQ_{28}	47	A_5	74	PD_2
21	NC	48	A_4	75	PD_3
22	NC	49	A_3	76	PD_4
23	NC	50	A_2	77	PD_5
24	$\overline{CE}_0$	51	A_1	78	PD_6
25	V_{SS}	52	A_0	79	PD_7
26	DQ_{29}	53	NC	80	V_{SS}
27	DQ_{30}	54	V_{SS}		

Pin Functions

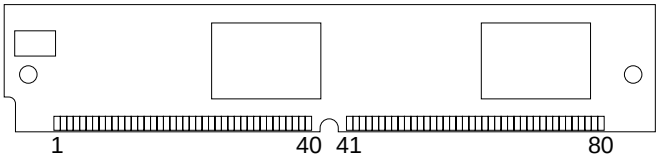
Pin Symbol	Pin Function
A_0-A_{19}	Address Inputs
DQ_0-DQ_{31}	Data In/Out
$\overline{CE}_0$	Chip Enable
$\overline{WE}_0$, $\overline{WE}_2$	Write Enable
$\overline{OE}$	Output Enable
PD_1-PD_7	Presence Detect
$\overline{RST}$	Reset
V_{CC}	Power (+5V)
V_{PP}	Programming Voltage (+12V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

(Optional)

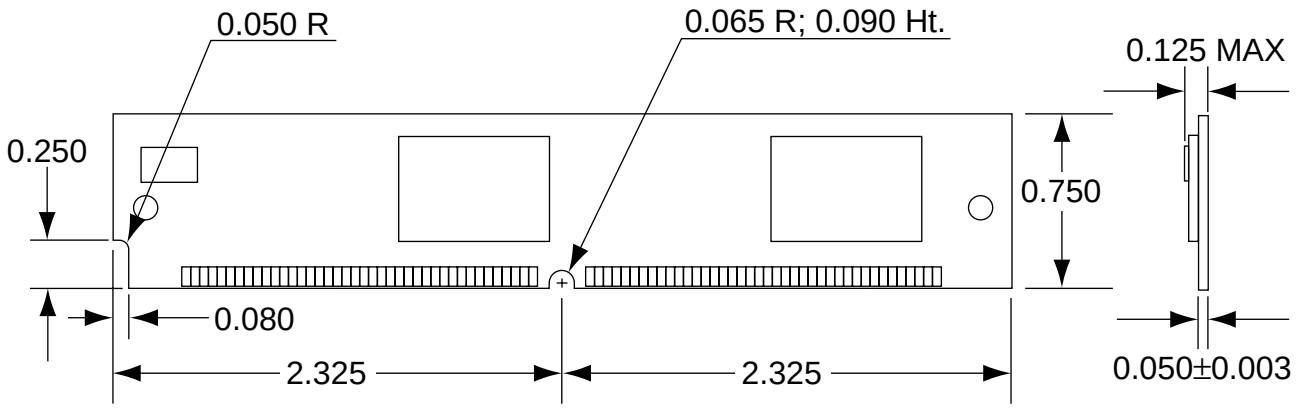
Pin Name	Signal
PD_1	NC
PD_2	V_{SS}
PD_3	NC
PD_4	V_{SS}
PD_5	NC
PD_6	NC
PD_7	V_{SS}

* Pin Connection Changing Available



PACKAGE DIMENSIONS

Units: Inches



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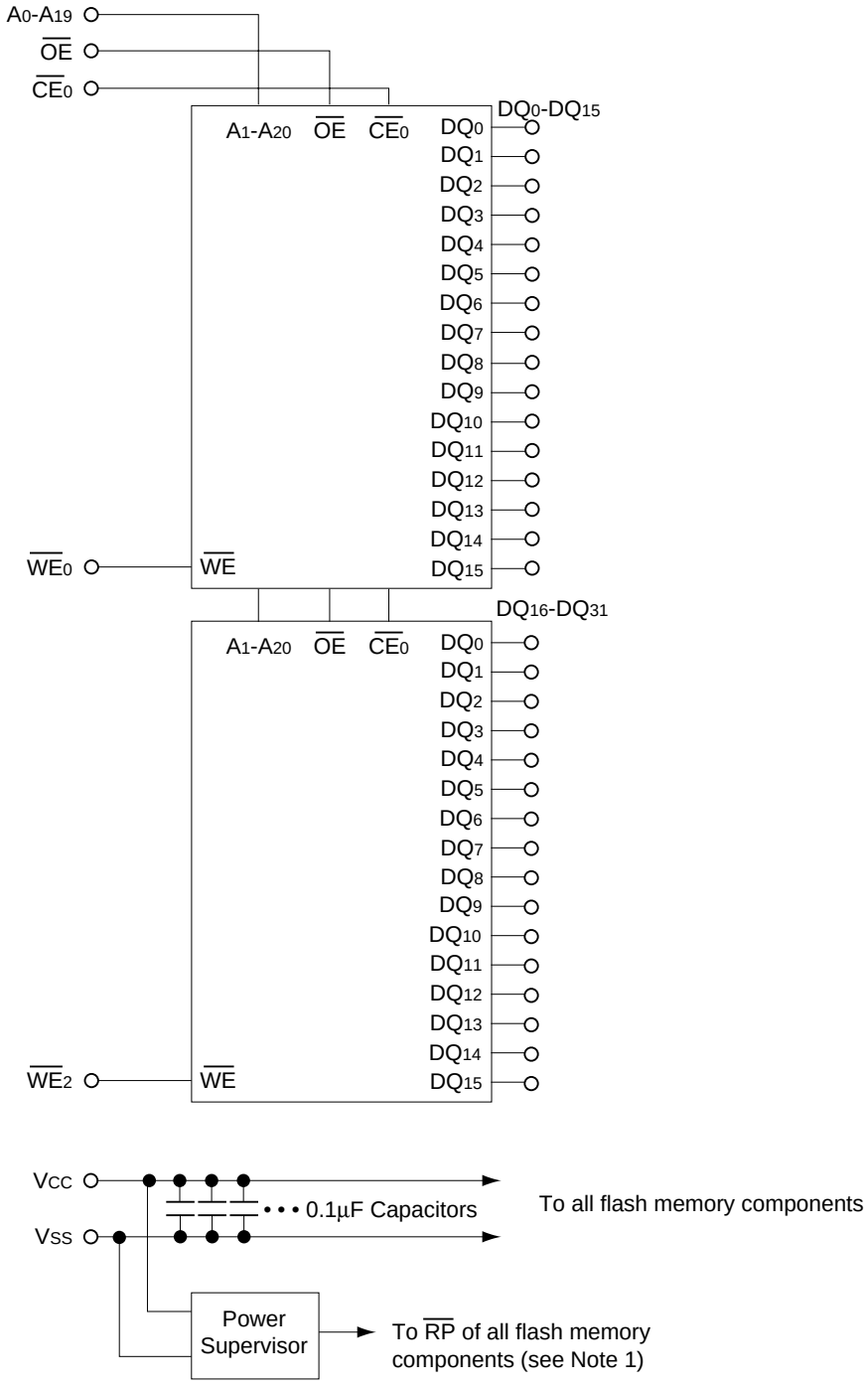
TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

FUNCTIONAL BLOCK DIAGRAM



Notes:

1. RP of all flash memory components is optionally tied to V_{CC}, tied to RST (Pin 7 of PCB), or connected to power supervisor circuit.
2. A_0 and RD/BY of all flash memory components are not connected.
3. BYTE and WP of all flash memory components is tied to V_{CC}.
4. V_{PP} of all flash memory components is connected to V_{PP} of system.
5. CE1 and 3/5 of all flash memory components is tied to V_{SS}.