

1M X 32 Bits DRAM 72-Pin SIMM with Extended Data Out (EDO)

FEATURES

- Performance range:

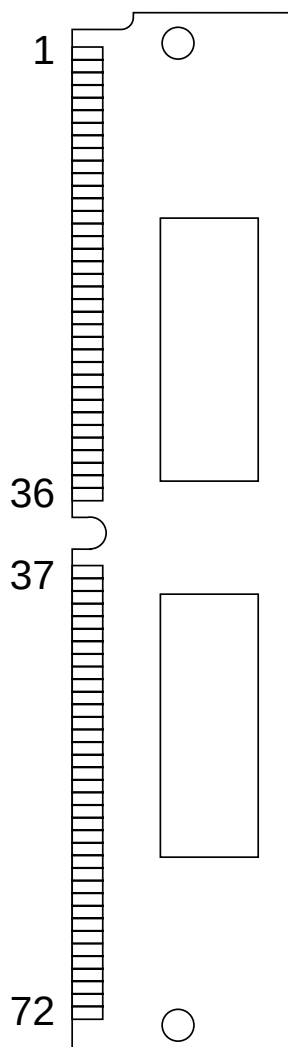
	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
SL...-A60	60ns	17ns	104ns	25ns
SL...-A70	70ns	20ns	124ns	30ns

- Extended Data Out (EDO) Mode operation called hyper page mode
- $\overline{\text{CAS}}$ -before-RAS refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V $\pm$ 10% power supply
- 1024 cycles/16ms refresh
- JEDEC standard pinout
- Gold or Tin edge connectors

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	25	DQ ₂₂	49	DQ ₈
2	DQ ₀	26	DQ ₇	50	DQ ₂₄
3	DQ ₁₆	27	DQ ₂₃	51	DQ ₉
4	DQ ₁	28	A ₇	52	DQ ₂₅
5	DQ ₁₇	29	NC	53	DQ ₁₀
6	DQ ₂	30	V _{CC}	54	DQ ₂₆
7	DQ ₁₈	31	A ₈	55	DQ ₁₁
8	DQ ₃	32	A ₉	56	DQ ₂₇
9	DQ ₁₉	33	NC	57	DQ ₁₂
10	V _{CC}	34	$\overline{\text{RAS}}_2$	58	DQ ₂₈
11	NC	35	NC	59	V _{CC}
12	A ₀	36	NC	60	DQ ₂₉
13	A ₁	37	NC	61	DQ ₁₃
14	A ₂	38	NC	62	DQ ₃₀
15	A ₃	39	V _{SS}	63	DQ ₁₄
16	A ₄	40	$\overline{\text{CAS}}_0$	64	DQ ₃₁
17	A ₅	41	$\overline{\text{CAS}}_2$	65	DQ ₁₅
18	A ₆	42	$\overline{\text{CAS}}_3$	66	NC
19	NC	43	$\overline{\text{CAS}}_1$	67	PD ₁
20	DQ ₄	44	$\overline{\text{RAS}}_0$	68	PD ₂
21	DQ ₂₀	45	NC	69	PD ₃
22	DQ ₅	46	NC	70	PD ₄
23	DQ ₂₁	47	$\overline{\text{W}}$	71	NC
24	DQ ₆	48	NC	72	V _{SS}



GENERAL DESCRIPTION

The SiliconTech SL32x6A1M1E-Axx is a 1M x 32 bits Dynamic RAM (DRAM) Single In-line Memory Module (SIMM). This module consists of two CMOS 1M x 16 bits DRAMs in 42-pin 400-mil SOJ packages mounted on a 72-pin glass epoxy substrate. Decoupling capacitors of 0.1 μ F are mounted for the DRAMs.

The SL32S6A1M1E-Axx has gold edge connectors and the SL32T6A1M1E-Axx has tin edge connectors. The module is intended for mounting into 72-pin SIMM edge connector sockets with the same lead, i.e. gold or tin.

Pin Functions

Pin Symbol	Pin Function
A ₀ -A ₉	Address Inputs
DQ ₀ -DQ ₃₁	Data In/Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}_0, \overline{\text{RAS}}_2$	Row Address Strobe
$\overline{\text{CAS}}_0, \overline{\text{CAS}}_3$	Column Address Strobe
PD ₁ -PD ₄	Presence Detect
V _{CC}	Power (+5V)
V _{SS}	Ground
NC	No Connection

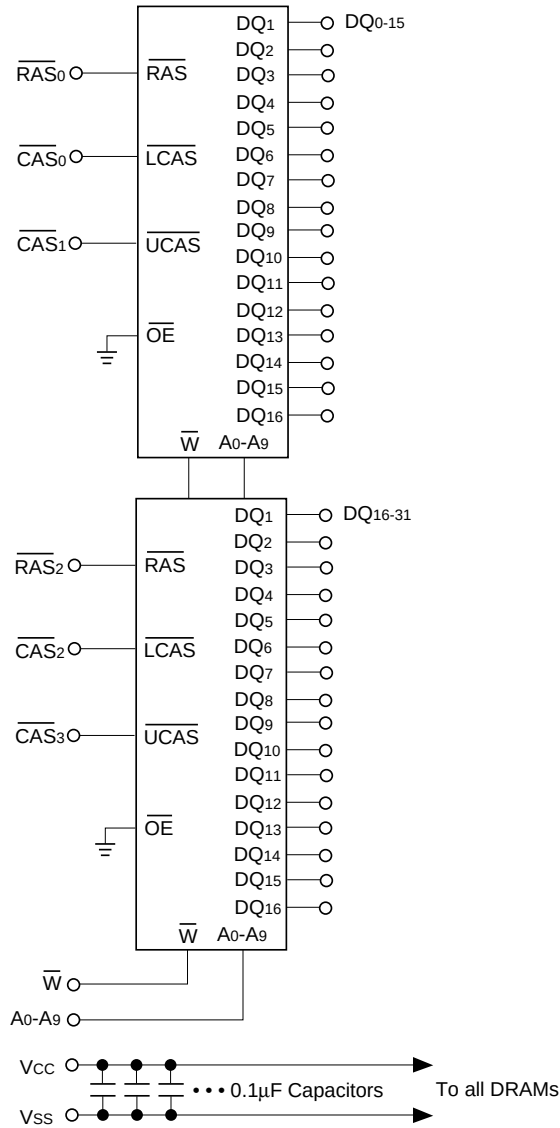
Presence Detect Pins*

(Optional)

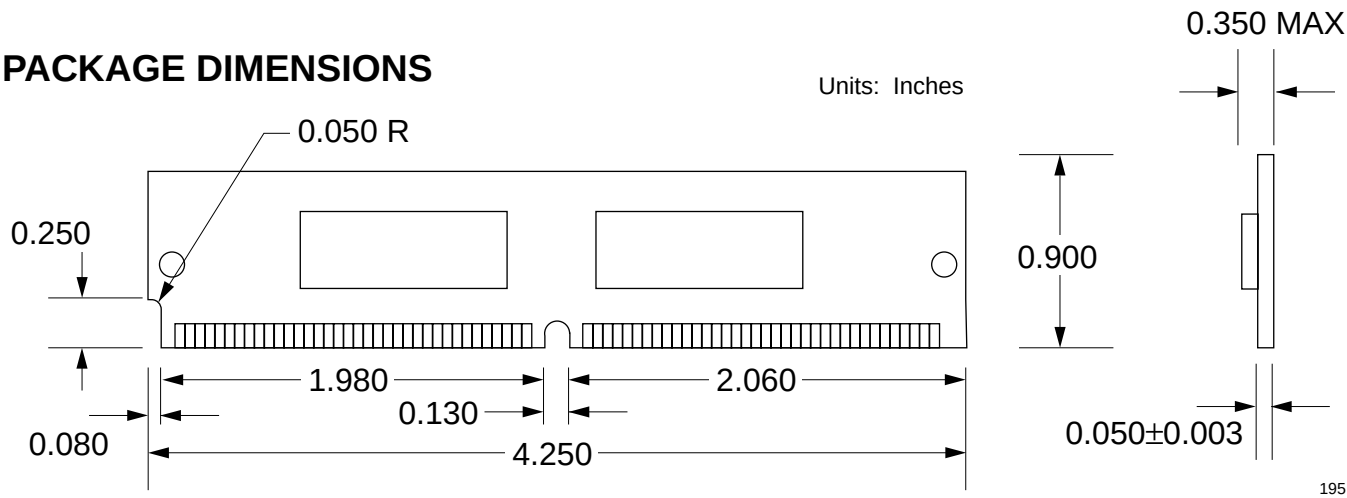
Pin Symbol	SL...-A60 (t _{RAC} =60ns)	SL...-A70 (t _{RAC} =70ns)
PD ₁	V _{SS}	V _{SS}
PD ₂	V _{SS}	V _{SS}
PD ₃	NC	V _{SS}
PD ₄	NC	NC

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

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