32M X 36 BITS DRAM SIMM with EDO and Optimized for ECC

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
SL36..-A60C	60ns	15ns	104ns	25ns
SL36..-A70C	70ns	20ns	124ns	30ns

- EDO operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V $\pm$ 10% power supply
- 4096 cycles/64ms refresh
- Four $\overline{CAS}$ ECC optimized pinout
- Tin or gold edge-connections

GENERAL DESCRIPTION

The SiliconTech SL36(S/T)4C32M4F-AxxC is a 32MB x 36 bits Dynamic RAM memory module. The module consists of eighteen CMOS 16M x 4 bits DRAMs in 32-pin 400-mil TSOP-II packages mounted on a 72-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are mounted for the DRAMs.

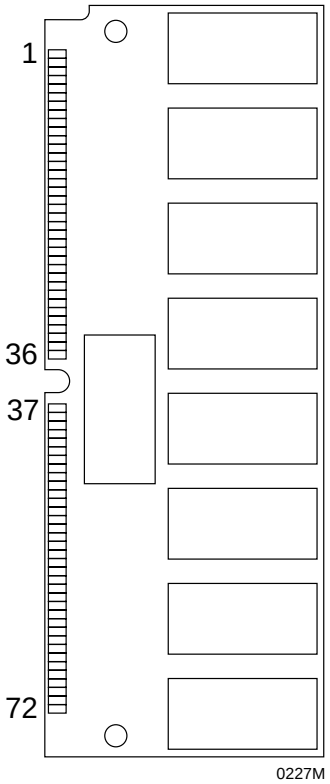
A voltage convertor steps down the 5.0V power supply from the computer to the 3.3V power supply for the DRAMs. Bus switches translate the signals between 5.0V on the computer and 3.3V on the DRAMs.

The module is a Single In-line Memory Module (SIMM) with tin edge connectors (SL36T4C32M4F-AxxC) intended for mounting into 72-pin SIMM tin edge connector sockets, or with gold edge connectors (SL36S4C32M4F-AxxC) intended for mounting into 72-pin SIMM gold edge connector sockets.

The SL36(S/T)4C32M4F-A60C has a t_{RAC} of 60ns, and the SL36(S/T)4C32M4F-A70C has a t_{RAC} of 70ns.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	A_{11}	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	A_9	56	DQ_{30}
9	DQ_{21}	33	$\overline{RAS}_1$	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS}_0$	58	DQ_{31}
11	NC	35	PQ_{26}	59	V_{CC}
12	A_0	36	PQ_8	60	DQ_{32}
13	A_1	37	PQ_{17}	61	DQ_{14}
14	A_2	38	PQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{34}
17	A_5	41	$\overline{CAS}_2$	65	DQ_{16}
18	A_6	42	$\overline{CAS}_3$	66	NC
19	A_{10}	43	$\overline{CAS}_1$	67	PD_1
20	DQ_4	44	$\overline{RAS}_0$	68	PD_2
21	DQ_{22}	45	$\overline{RAS}_1$	69	PD_3
22	DQ_5	46	NC	70	PD_4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}



Pin Names

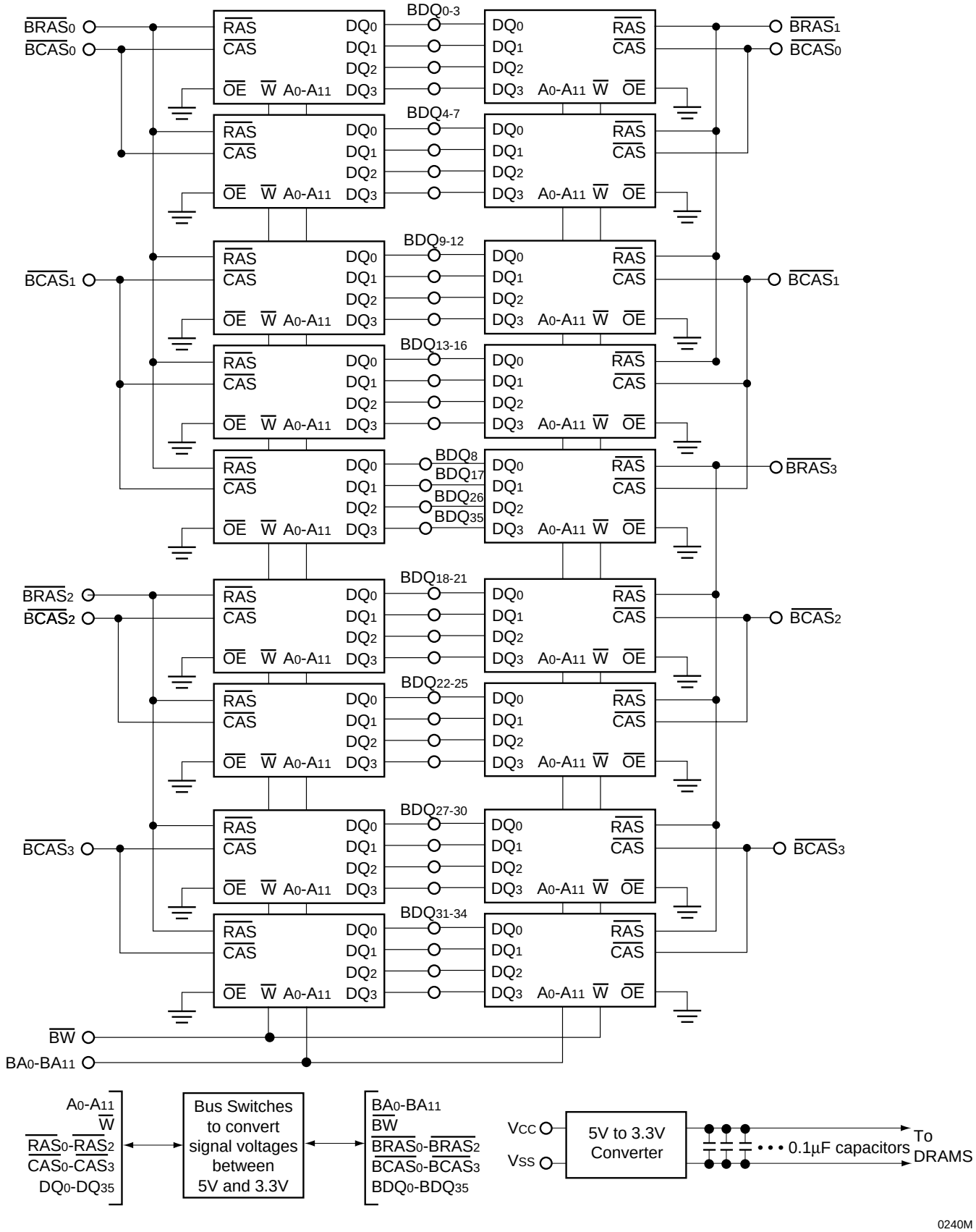
Pin Name	Pin Function
A_0-A_{11}	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_1$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*
(Optional)

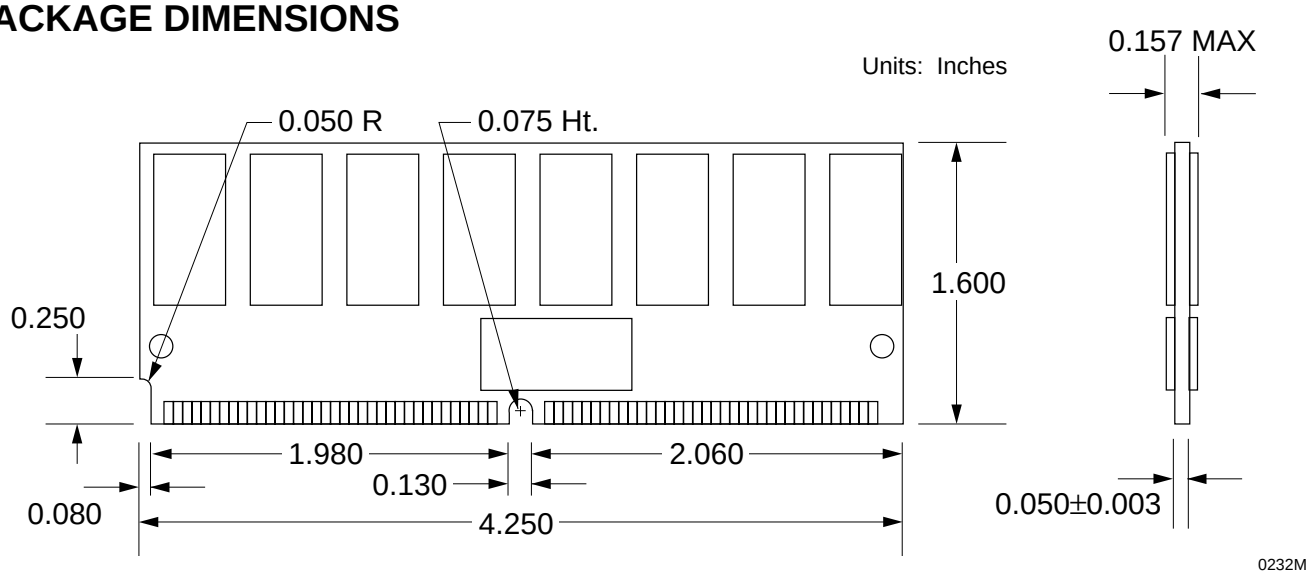
Pin	60ns	70ns
PD_1	NC	NC
PD_2	NC	NC
PD_3	NC	V_{SS}
PD_4	NC	NC

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED