

4M X 32 Bits DRAM 72-Pin SIMM with Extended Data Out (EDO)

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- Extended Data Out (EDO) operation
- $\overline{CAS}$ -before- $\overline{RAS}$ refresh capability
- $\overline{RAS}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V $\pm$ 10% power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Gold or Tin edge connectors

GENERAL DESCRIPTION

The SiliconTech SL32(S/T)6C4M4E-A60C is a 4M x 32 bit Dynamic RAM (DRAM) Single In-line Memory Module (SIMM). This module consists of two CMOS 4M x 16 bit 3.3V DRAM components in 50-pin 400-mil TSOP-II packages. Decoupling capacitors of 0.1 μ F are also mounted.

A 5.0V to 3.3V convertor supplies power to the 3.3V components, and bus switches convert the signals of the 3.3V components between 5.0V and 3.3V.

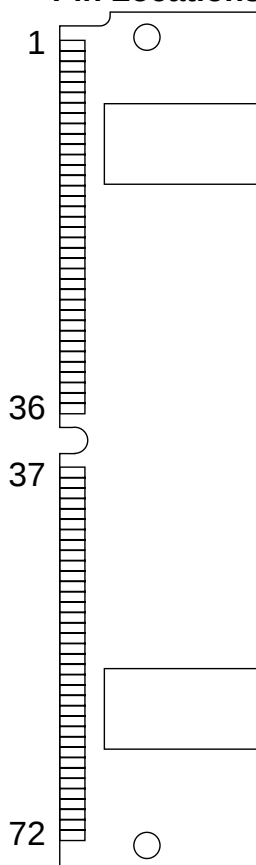
The SL32S6C4M4E-A60C has gold edge connectors and the SL32T6C4M4E-A60C has tin edge connectors. Both are intended for mounting in 72-pin Single In-line Memory Module (SIMM) sockets with the same lead.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ ₂₂	49	DQ ₈
2	DQ ₀	26	DQ ₇	50	DQ ₂₄
3	DQ ₁₆	27	DQ ₂₃	51	DQ ₉
4	DQ ₁	28	A ₇	52	DQ ₂₅
5	DQ ₁₇	29	A ₁₁	53	DQ ₁₀
6	DQ ₂	30	V_{CC}	54	DQ ₂₆
7	DQ ₁₈	31	A ₈	55	DQ ₁₁
8	DQ ₃	32	A ₉	56	DQ ₂₇
9	DQ ₁₉	33	NC	57	DQ ₁₂
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ ₂₈
11	NC	35	NC	59	V_{CC}
12	A ₀	36	NC	60	DQ ₂₉
13	A ₁	37	NC	61	DQ ₁₃
14	A ₂	38	NC	62	DQ ₃₀
15	A ₃	39	V_{SS}	63	DQ ₁₄
16	A ₄	40	$\overline{CAS}_0$	64	DQ ₃₁
17	A ₅	41	$\overline{CAS}_2$	65	DQ ₁₅
18	A ₆	42	$\overline{CAS}_3$	66	NC
19	A ₁₀	43	$\overline{CAS}_1$	67	PD ₁
20	DQ ₄	44	$\overline{RAS}_0$	68	PD ₂
21	DQ ₂₀	45	NC	69	PD ₃
22	DQ ₅	46	NC	70	PD ₄
23	DQ ₂₁	47	$\overline{W}$	71	NC
24	DQ ₆	48	NC	72	V_{SS}

Pin Locations



Pin Functions

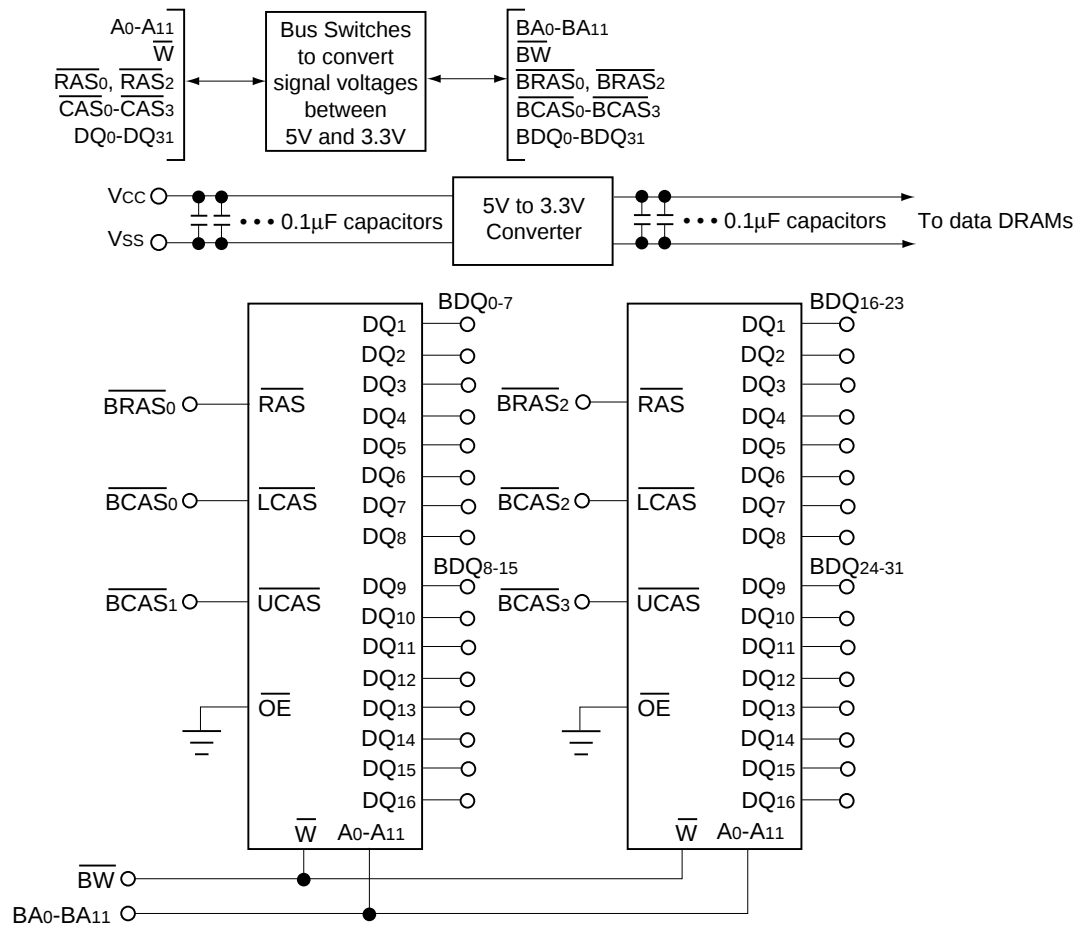
Pin Symbol	Pin Function
A ₀ -A ₁₁	Address Inputs
DQ ₀ -DQ ₃₅	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0, \overline{RAS}_2$	Row Address Strobe
$\overline{CAS}_0, \overline{CAS}_3$	Column Address Strobe
PD ₁ -PD ₄	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

Presence Detect Pins*

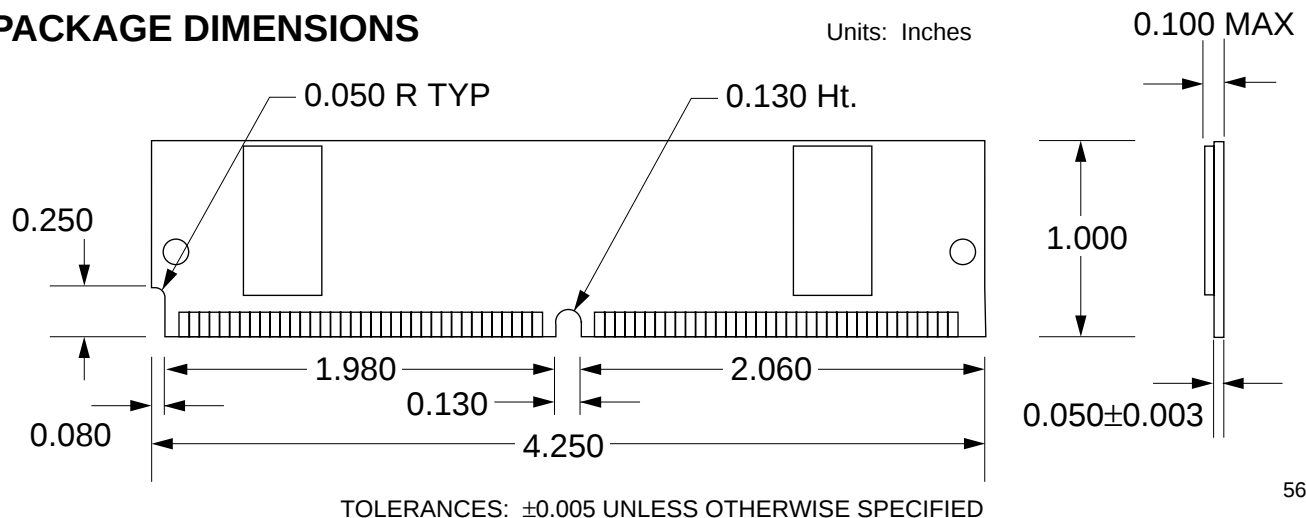
For $t_{RAC}=60ns$:
 PD₁= V_{SS}
 PD₂=NC
 PD₃=NC
 PD₄=NC

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



565A