32M X 72 Bit DRAM DIMM with EDO and ECC Optimized

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
50ns	18ns	90ns	25ns

- Extended Data Out (EDO) Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only refresh capability
- LVTTL compatible inputs and outputs
- +3.3V $\pm$ 0.3V power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- ECC Optimized
- Gold edge connectors
- NEC μPD4265405G5-A50 DRAM components

GENERAL DESCRIPTION

The SiliconTech SL72B4C32M4F-B50VI is an 32M x 72 bit Dynamic RAM (DRAM) Dual In-line Memory Module (DIMM). The module consists of thirty-six 16M x 4 bit DRAMs in 400-mil 34-pin TSOP II packages. The DRAMs are mounted on a 168-pin glass epoxy substrate. Decoupling capacitors of 0.1μF are mounted for the DRAMs. Selected inputs and outputs are buffered for improved performance and easier memory subsystem design.

The module is intended for mounting into 168-pin edge connector sockets keyed for 3.3V power supply and buffered signals.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	NC	49	V_{CC}	73	V_{CC}	97	DQ_{45}	121	A_9	145	NC
2	DQ_0	26	V_{CC}	50	NC	74	DQ_{32}	98	DQ_{46}	122	A_{11}	146	NC
3	DQ_1	27	$\overline{WE}_0$	51	NC	75	DQ_{33}	99	DQ_{47}	123	NC	147	NC
4	DQ_2	28	$\overline{CAS}_0$	52	DQ_{18}	76	DQ_{34}	100	DQ_{48}	124	V_{CC}	148	NC
5	DQ_3	29	NC	53	DQ_{19}	77	PQ_{35}	101	DQ_{49}	125	NC	149	DQ_{61}
6	V_{CC}	30	$\overline{RAS}_0$	54	V_{SS}	78	V_{SS}	102	V_{CC}	126	B_0	150	DQ_{62}
7	DQ_4	31	$\overline{OE}_0$	55	DQ_{20}	79	PD_1	103	DQ_{50}	127	V_{SS}	151	DQ_{63}
8	DQ_5	32	V_{SS}	56	DQ_{21}	80	PD_3	104	DQ_{51}	128	NC	152	V_{SS}
9	DQ_6	33	A_0	57	DQ_{22}	81	PD_5	105	DQ_{52}	129	$\overline{RAS}_3$	153	DQ_{64}
10	DQ_7	34	A_2	58	DQ_{23}	82	PD_7	106	DQ_{53}	130	$\overline{CAS}_5$	154	DQ_{65}
11	DQ_8	35	A_4	59	V_{CC}	83	ID_0	107	V_{SS}	131	NC	155	DQ_{66}
12	V_{SS}	36	A_6	60	DQ_{24}	84	V_{CC}	108	NC	132	$\overline{PDE}$	156	DQ_{67}
13	DQ_9	37	A_8	61	NC	85	V_{SS}	109	NC	133	V_{CC}	157	V_{CC}
14	DQ_{10}	38	A_{10}	62	NC	86	DQ_{36}	110	V_{CC}	134	NC	158	DQ_{68}
15	DQ_{11}	39	NC	63	NC	87	DQ_{37}	111	NC	135	NC	159	DQ_{69}
16	DQ_{12}	40	V_{CC}	64	NC	88	DQ_{38}	112	$\overline{CAS}_1$	136	DQ_{54}	160	DQ_{70}
17	DQ_{13}	41	NC	65	DQ_{25}	89	DQ_{39}	113	NC	137	DQ_{55}	161	DQ_{71}
18	V_{CC}	42	NC	66	DQ_{26}	90	V_{CC}	114	$\overline{RAS}_1$	138	V_{SS}	162	V_{SS}
19	DQ_{14}	43	V_{SS}	67	DQ_{27}	91	DQ_{40}	115	NC	139	DQ_{56}	163	PD_2
20	DQ_{15}	44	$\overline{OE}_2$	68	V_{SS}	92	DQ_{41}	116	V_{SS}	140	DQ_{57}	164	PD_4
21	DQ_{16}	45	$\overline{RAS}_2$	69	DQ_{28}	93	DQ_{42}	117	A_1	141	DQ_{58}	165	PD_6
22	DQ_{17}	46	$\overline{CAS}_4$	70	DQ_{29}	94	DQ_{43}	118	A_3	142	DQ_{59}	166	PD_8
23	V_{SS}	47	NC	71	DQ_{30}	95	DQ_{44}	119	A_5	143	V_{CC}	167	ID_1
24	NC	48	$\overline{WE}_2$	72	DQ_{31}	96	V_{SS}	120	A_7	144	DQ_{60}	168	V_{CC}

continued on the next page

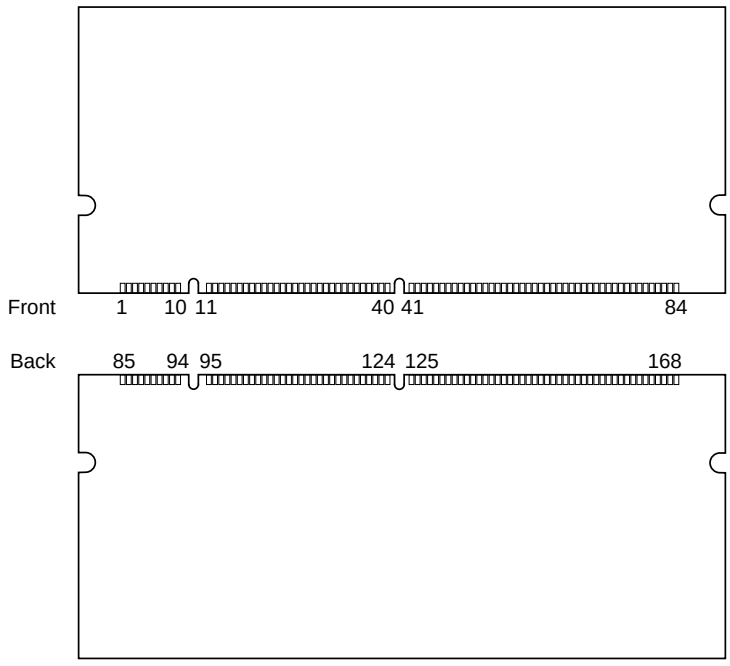
PIN CONFIGURATION (continued)

Pin Names

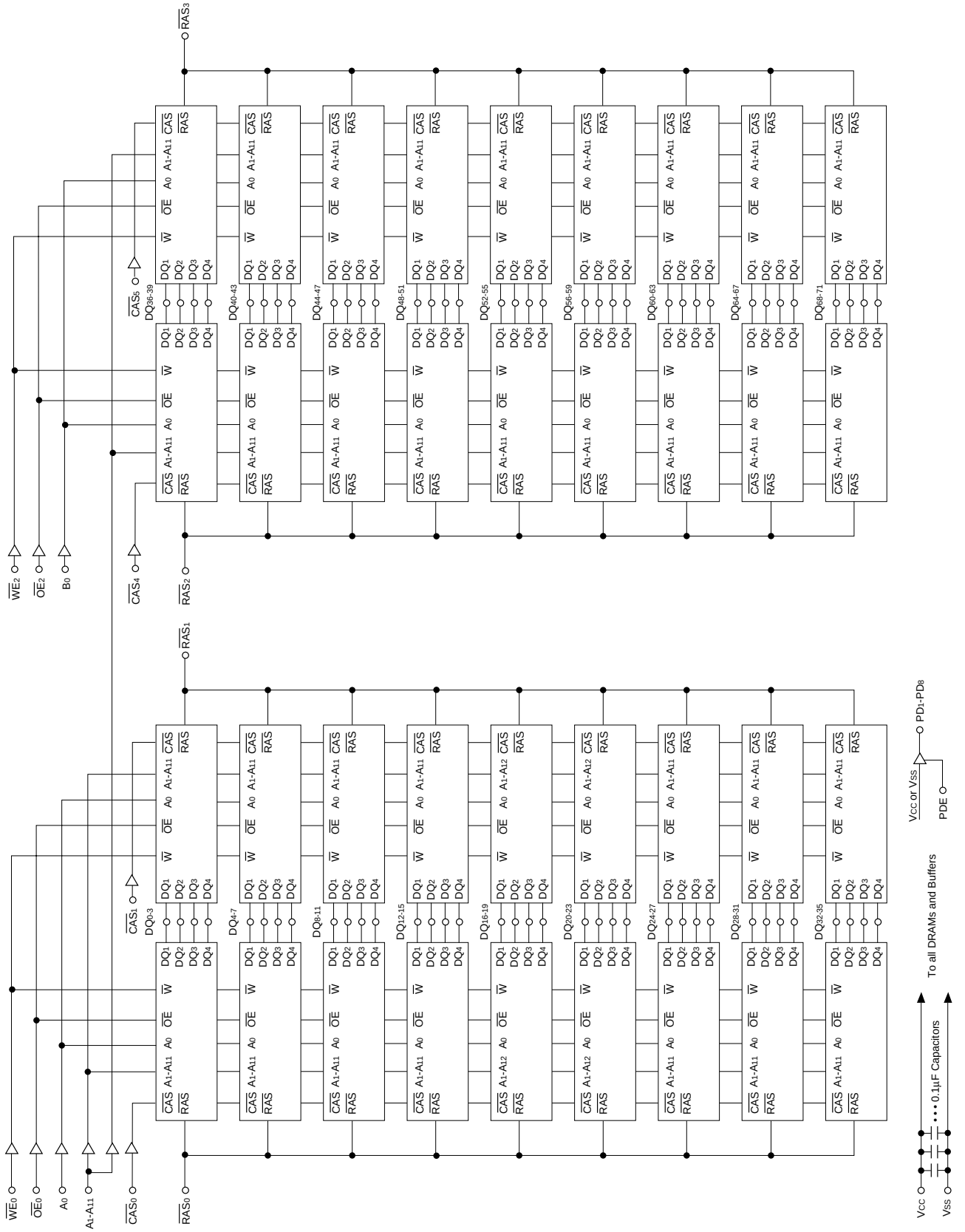
Pin Name	Pin Function
A_0, B_0, A_1-A_{11}	Address Inputs (Buffered)
DQ_0-DQ_{71}	Data In/Out
$\overline{WE}_0$, $\overline{WE}_2$	Read/Write Input (Buffered)
$\overline{OE}_0$, $\overline{OE}_2$	Output Enable (Buffered)
$\overline{RAS}_1$- $\overline{RAS}_3$	Row Adress Strobe
$\overline{CAS}_0$, $\overline{CAS}_1$, $\overline{CAS}_4$,$\overline{CAS}_5$	Column Addr. Strobe (Buffered)
PD_1-PD_8	Presence Detect (Buffered)
$\overline{PDE}$	Presence Detect Enable
ID_0-ID_1	ID Bits
V_{CC}	Power (+3.3V)
V_{SS}	Ground
NC	No Connection

Presence Detect

For 32Mx72 Configuration with 16M x 4 Bits, EDO, and 4K Refresh DRAM components:
PD_1=NC, PD_2=V_{SS}, PD_3=V_{SS}, PD_4=V_{SS}
For EDO:
PD_5=NC
For 50ns:
PD_6=V_{SS}, PD_7=V_{SS}
For ECC:
PD_8=V_{SS}
For x72 ECC:
ID_0 =V_{SS}
For Normal Refresh Mode:
ID_1=V_{SS}

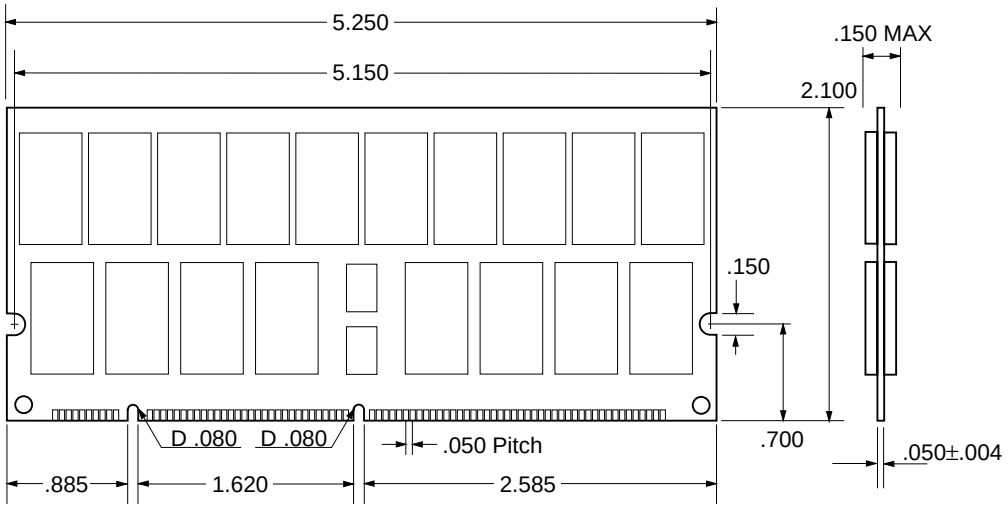


FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED