

16M X 36 Bits (64MB) DRAM 72-Pin SIMM with Extended Data Out (EDO)

FEATURES

- Performance range:

Part #	t _{RAC}	t _{CAC}	t _{RC}	t _{HPC}
SL...-A50C	50ns	13ns	84ns	20ns
SL...-A60C	60ns	15ns	104ns	25ns

- Extended Data Out (EDO) Mode operation
- $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh capability
- $\overline{\text{RAS}}$ -only and Hidden refresh capability
- TTL compatible inputs and outputs
- +5V $\pm$ 10% power supply
- 4096 cycles/64ms refresh
- JEDEC standard pinout
- Gold or Tin edge connectors

GENERAL DESCRIPTION

The SiliconTech SL36(S/T)4C16M4F-AxxC is a 16M x 36 bits Dynamic RAM (DRAM) Single In-line Memory Module (SIMM). This module consists of nine CMOS 16M x 4 bits 3.3V DRAM components in 32-pin 400-mil SOJ packages. Decoupling capacitors of 0.1 μ F are also mounted.

A 5.0V to 3.3V convertor supplies power to the 3.3V components, and bus switches convert the signals to the 3.3V components from 5.0V to 3.3V.

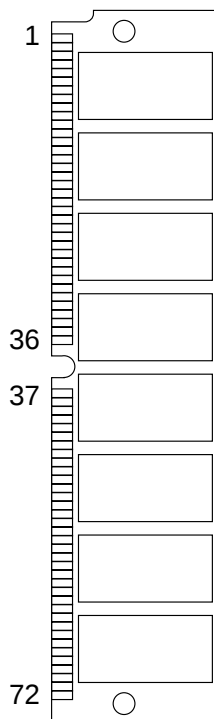
The SL36S4C16M4F-AxxC has gold edge connectors and the SL36T4C16M4F-AxxC has tin edge connectors. The SL36(S/T)4C16M4F-A50C and the SL36(S/T)4C16M4F-A60C have a t_{RAC} of 50ns and 60ns respectively.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	25	DQ ₂₂	49	DQ ₈
2	DQ ₀	26	DQ ₇	50	DQ ₂₄
3	DQ ₁₆	27	DQ ₂₃	51	DQ ₉
4	DQ ₁	28	A ₇	52	DQ ₂₅
5	DQ ₁₇	29	A ₁₁	53	DQ ₁₀
6	DQ ₂	30	V _{CC}	54	DQ ₂₆
7	DQ ₁₈	31	A ₈	55	DQ ₁₁
8	DQ ₃	32	A ₉	56	DQ ₂₇
9	DQ ₁₉	33	NC	57	DQ ₁₂
10	V _{CC}	34	$\overline{\text{RAS}}_2$	58	DQ ₂₈
11	NC	35	NC	59	V _{CC}
12	A ₀	36	NC	60	DQ ₂₉
13	A ₁	37	NC	61	DQ ₁₃
14	A ₂	38	NC	62	DQ ₃₀
15	A ₃	39	V _{SS}	63	DQ ₁₄
16	A ₄	40	$\overline{\text{CAS}}_0$	64	DQ ₃₁
17	A ₅	41	$\overline{\text{CAS}}_2$	65	DQ ₁₅
18	A ₆	42	$\overline{\text{CAS}}_3$	66	NC
19	A ₁₀	43	$\overline{\text{CAS}}_1$	67	PD ₁
20	DQ ₄	44	$\overline{\text{RAS}}_0$	68	PD ₂
21	DQ ₂₀	45	NC	69	PD ₃
22	DQ ₅	46	NC	70	PD ₄
23	DQ ₂₁	47	$\overline{\text{W}}$	71	NC
24	DQ ₆	48	NC	72	V _{SS}

Pin Locations



Pin Functions

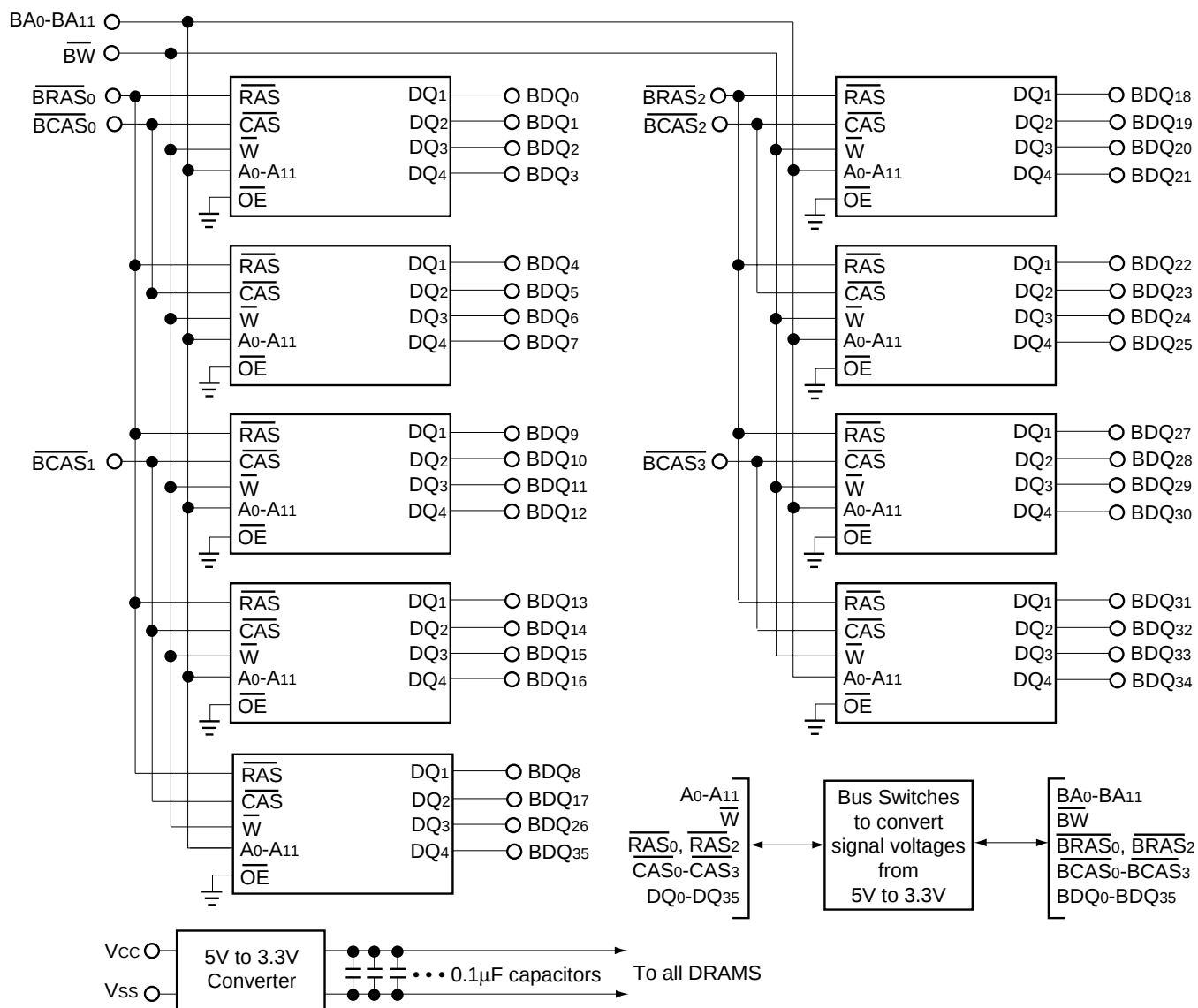
Pin Symbol	Pin Function
A ₀ -A ₁₁	Address Inputs
DQ ₀ -DQ ₃₅	Data In/Out
$\overline{\text{W}}$	Read/Write Input
$\overline{\text{RAS}}_0$, $\overline{\text{RAS}}_2$	Row Address Strobe
$\overline{\text{CAS}}_0$ - $\overline{\text{CAS}}_3$	Column Address Strobe
PD ₁ -PD ₄	Presence Detect
V _{CC}	Power (+5V)
V _{SS}	Ground
NC	No Connection

Presence Detect Pins*

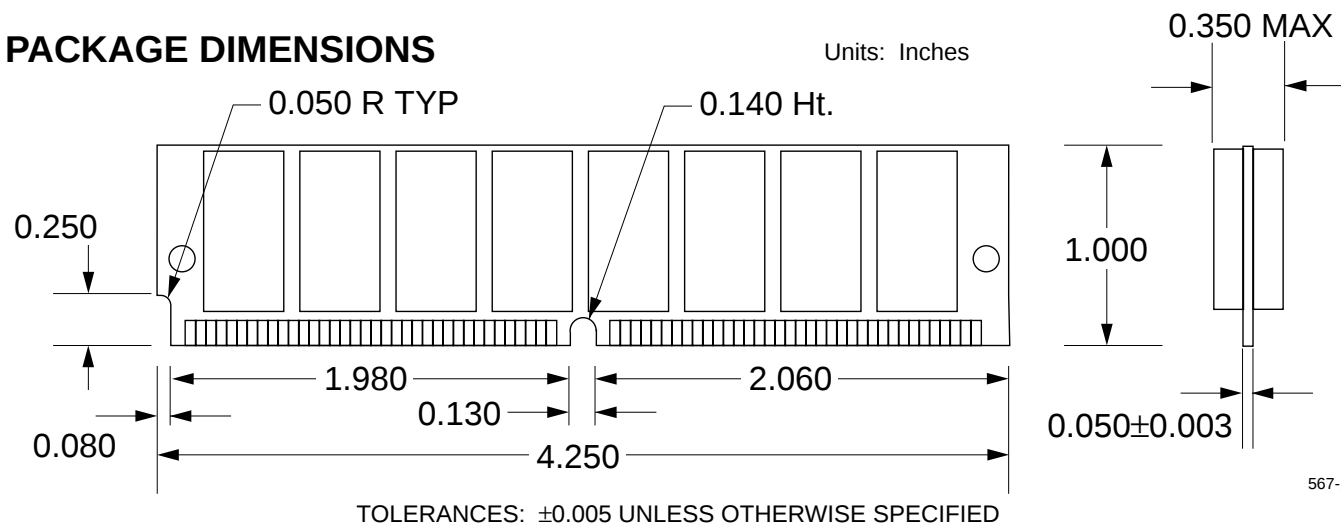
Pin Symbol	SL...-A50C (t _{RAC} =50ns)	SL...-A60C (t _{RAC} =60ns)
PD ₁	V _{SS}	V _{SS}
PD ₂	NC	NC
PD ₃	V _{SS}	NC
PD ₄	V _{SS}	NC

* Pin Connection Changing Available

FUNCTIONAL BLOCK DIAGRAM



PACKAGE DIMENSIONS



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