

4M X 32 Bits DRAM 72-Pin SO-DIMM EDO Memory Module

FEATURES

- Performance range:

t_{RAC}	t_{CAC}	t_{RC}	t_{HPC}
60ns	15ns	104ns	25ns

- Extended Data Out (EDO) Mode operation called hyper page mode
- $\overline{CAS}$ -before- $\overline{RAS}$ refresh capability
- $\overline{RAS}$ -only and Hidden refresh capability
- LVTTL compatible inputs and outputs
- +3.3V $\pm$ 0.3V power supply
- 2048 cycles/32ms refresh
- JEDEC standard pinout
- Gold edge connectors

GENERAL DESCRIPTION

The SiliconTech SL32D4B4M2E-A60V is a 4M x 32 bits Dynamic RAM (DRAM) Small Outline Dual Inline Memory Module (SO-DIMM). This module consists of eight CMOS 4M x 4 bits DRAMs in 24-pin SOJ packages mounted on a 72-pin glass epoxy substrate. Eight 0.1 μ F decoupling capacitors are mounted for the DRAMs.

The module has gold edge connectors intended for mounting into 72-pin SO-DIMM edge connector sockets. The module is keyed for 3.3V Power Supply.

PIN CONFIGURATION

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V _{SS}	25	DQ ₁₂	49	DQ ₁₈
2	DQ ₀	26	DQ ₁₃	50	DQ ₁₉
3	DQ ₁	27	DQ ₁₄	51	DQ ₂₀
4	DQ ₂	28	A ₇	52	DQ ₂₁
5	DQ ₃	29	NC	53	DQ ₂₂
6	DQ ₄	30	V _{CC}	54	DQ ₂₃
7	DQ ₅	31	A ₈	55	NC
8	DQ ₆	32	A ₉	56	DQ ₂₄
9	DQ ₇	33	NC	57	DQ ₂₅
10	V _{CC}	34	$\overline{RAS}_2$	58	DQ ₂₆
11	PD ₁	35	DQ ₁₅	59	DQ ₂₈
12	A ₀	36	NC	60	DQ ₂₇
13	A ₁	37	DQ ₁₆	61	V _{CC}
14	A ₂	38	DQ ₁₇	62	DQ ₂₉
15	A ₃	39	V _{SS}	63	DQ ₃₀
16	A ₄	40	$\overline{CAS}_0$	64	DQ ₃₁
17	A ₅	41	$\overline{CAS}_2$	65	NC
18	A ₆	42	$\overline{CAS}_3$	66	PD ₂
19	A ₁₀	43	$\overline{CAS}_1$	67	PD ₃
20	NC	44	$\overline{RAS}_0$	68	PD ₄
21	DQ ₈	45	NC	69	PD ₅
22	DQ ₉	46	NC	70	PD ₆
23	DQ ₁₀	47	$\overline{W}$	71	PD ₇
24	DQ ₁₁	48	NC	72	V _{SS}

Pin Names

Pin Name	Pin Function
A ₀ -A ₁₀	Address Inputs
DQ ₀ -DQ ₃₁	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$, $\overline{RAS}_2$	Row Address Strobe
$\overline{CAS}_0$ - $\overline{CAS}_3$	Column Address Strobe
PD ₁ -PD ₇	Presence Detect
V _{CC}	Power (+3.3V)
V _{SS}	Ground
NC	No Connection

Presence Detect Pins

For 4Mx32 Configuration with 4Mx4, 2K DRAM Components:
PD₁=NC, PD₂=NC, PD₃=V_{SS}, PD₄=NC

Speed 60ns:

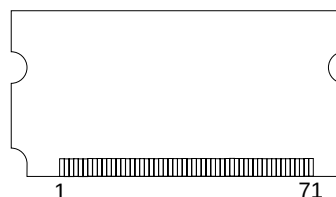
PD₅=NC, PD₆=NC

Normal Refresh:

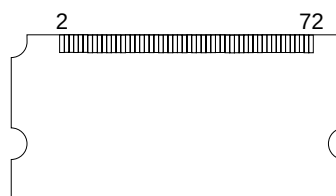
PD₇=NC

Pin Locations

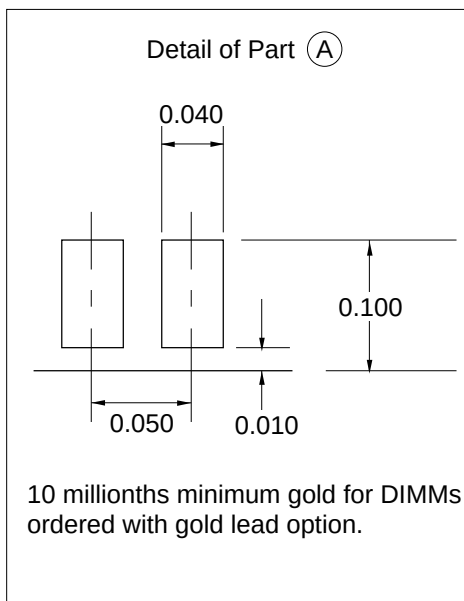
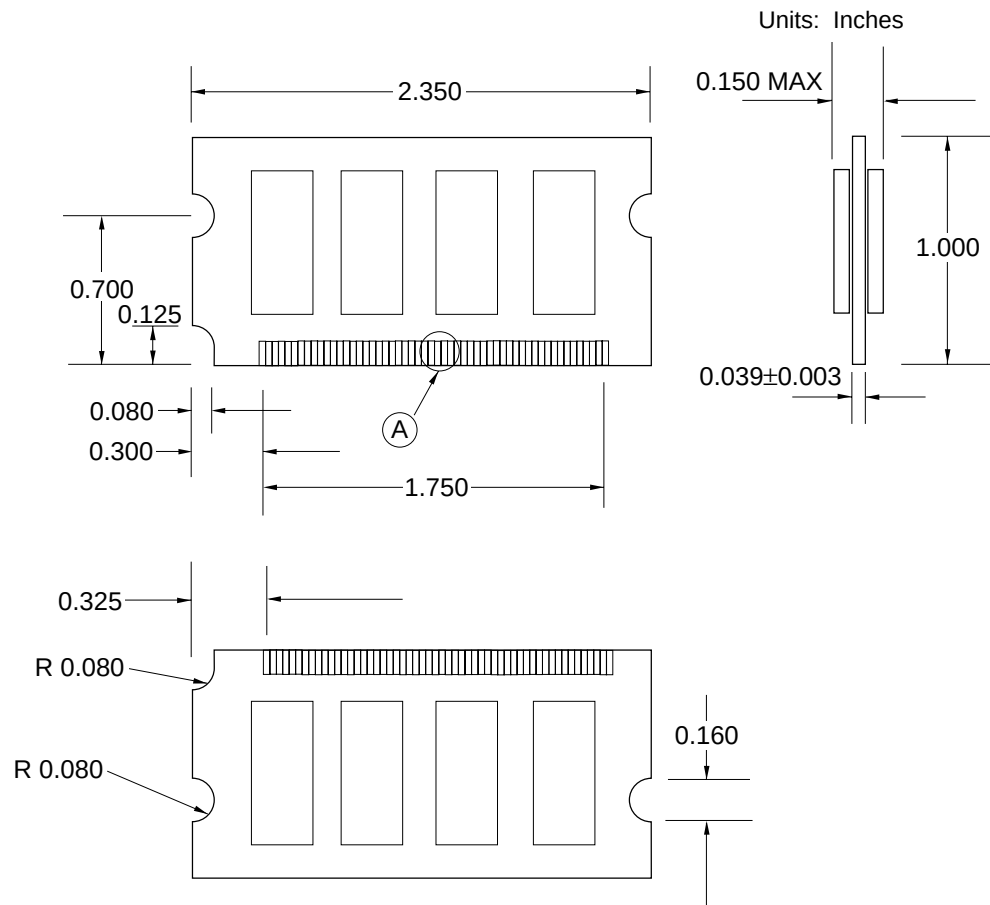
Odd numbered pins from pin 1 to pin 71 on front



Even numbered pins from pin 2 to pin 72 on back



PACKAGE DIMENSIONS

TOLERANCES: ± 0.005 UNLESS OTHERWISE SPECIFIED

FUNCTIONAL BLOCK DIAGRAM

