8M X 36 Bits DRAM SIMM with Fast Page Mode

FEATURES

- Performance range:

	t_{RAC}	t_{CAC}	t_{RC}	t_{PC}
SL…-A50	50ns	13ns	90ns	35ns
SL…-A60	60ns	15ns	110ns	40ns
SL…-A70	70ns	20ns	130ns	45ns

- Fast Page Mode operation
- $\overline{CAS}$-before-$\overline{RAS}$ refresh capability
- $\overline{RAS}$-only and Hidden refresh capability
- TTL compatible inputs and outputs
- Single +5V ± 10% power supply
- 2048 cycles/32ms refresh
- JEDEC standard pinout

GENERAL DESCRIPTION

The SiliconTech SL36(S/T)4B8M2B-Axx is a 8M x 36 bits Dynamic RAM (DRAM) memory module. This module consists of sixteen CMOS 4M x 4 bits DRAMs in 24-pin SOJ package and eight CMOS 4M x 1 bit DRAMs in a 20-pin SOJ package mounted on a 72-pin glass epoxy substrate. Decoupling capacitors of 0.1µF are mounted for the DRAMs.

The module is a Single In-line Memory Module (SIMM) with tin edge connections (SL36T4B8M2B-Axx) or gold edge connections (SL36S4B8M2B-Axx) and is intended for mounting into 72-pin SIMM edge connector sockets of like lead.

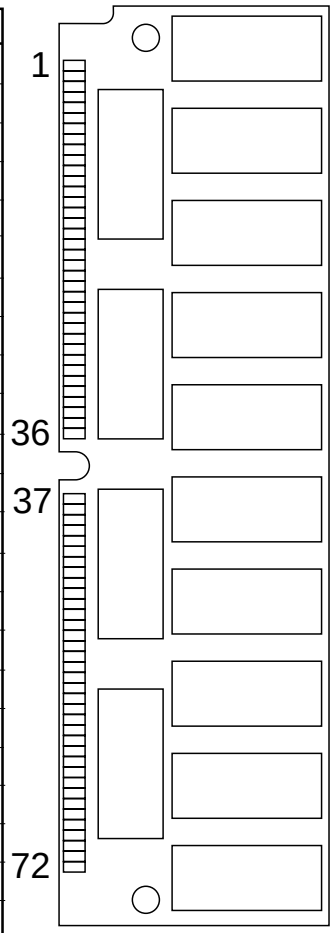
The SL36S4B8M2B-A50, SL36S4B8M2B-A60, and SL36S4B8M2B-A70 have t_{RAC} of 50ns, 60ns, and 70ns respectively.

PIN CONFIGURATION

Pin Symbols

Pin	Symbol	Pin	Symbol	Pin	Symbol
1	V_{SS}	25	DQ_{24}	49	DQ_9
2	DQ_0	26	DQ_7	50	DQ_{27}
3	DQ_{18}	27	DQ_{25}	51	DQ_{10}
4	DQ_1	28	A_7	52	DQ_{28}
5	DQ_{19}	29	NC	53	DQ_{11}
6	DQ_2	30	V_{CC}	54	DQ_{29}
7	DQ_{20}	31	A_8	55	DQ_{12}
8	DQ_3	32	A_9	56	DQ_{30}
9	DQ_{21}	33	$\overline{RAS}_3$	57	DQ_{13}
10	V_{CC}	34	$\overline{RAS}_2$	58	DQ_{31}
11	NC	35	DQ_{26}	59	V_{CC}
12	A_0	36	DQ_8	60	DQ_{32}
13	A_1	37	DQ_{17}	61	DQ_{14}
14	A_2	38	DQ_{35}	62	DQ_{33}
15	A_3	39	V_{SS}	63	DQ_{15}
16	A_4	40	$\overline{CAS}_0$	64	DQ_{34}
17	A_5	41	$\overline{CAS}_2$	65	DQ_{16}
18	A_6	42	$\overline{CAS}_3$	66	NC
19	A_{10}	43	$\overline{CAS}_1$	67	PD_1
20	DQ_4	44	$\overline{RAS}_0$	68	PD_2
21	DQ_{22}	45	$\overline{RAS}_1$	69	PD_3
22	DQ_5	46	NC	70	PD_4
23	DQ_{23}	47	$\overline{W}$	71	NC
24	DQ_6	48	NC	72	V_{SS}

Pin Locations



Pin Functions

Pin Name	Pin Function
A_0-A_{10}	Address Inputs
DQ_0-DQ_{35}	Data In/Out
$\overline{W}$	Read/Write Input
$\overline{RAS}_0$-$\overline{RAS}_3$	Row Adress Strobe
$\overline{CAS}_0$-$\overline{CAS}_3$	Column Address Strobe
PD_1-PD_4	Presence Detect
V_{CC}	Power (+5V)
V_{SS}	Ground
NC	No Connection

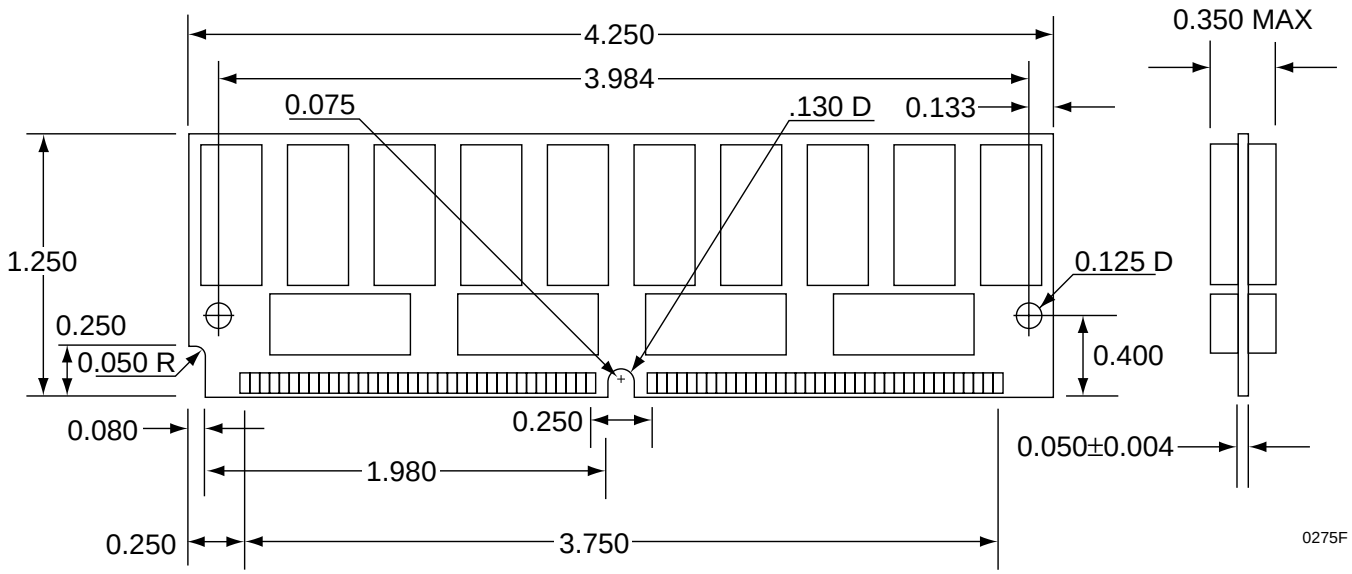
Presence Detect Pins*

Pin	50ns	60ns	70ns
PD_1	NC	NC	NC
PD_2	V_{SS}	V_{SS}	V_{SS}
PD_3	V_{SS}	NC	V_{SS}
PD_4	V_{SS}	NC	NC

* Pin Connection Changing Available

PACKAGE DIMENSIONS

Units: Inches



TOLERANCES: ±0.005 UNLESS OTHERWISE SPECIFIED

FUNCTIONAL BLOCK DIAGRAM