Precision RESET Controller with 16K I²C Memory

3 and 5 Volt Systems

FEATURES

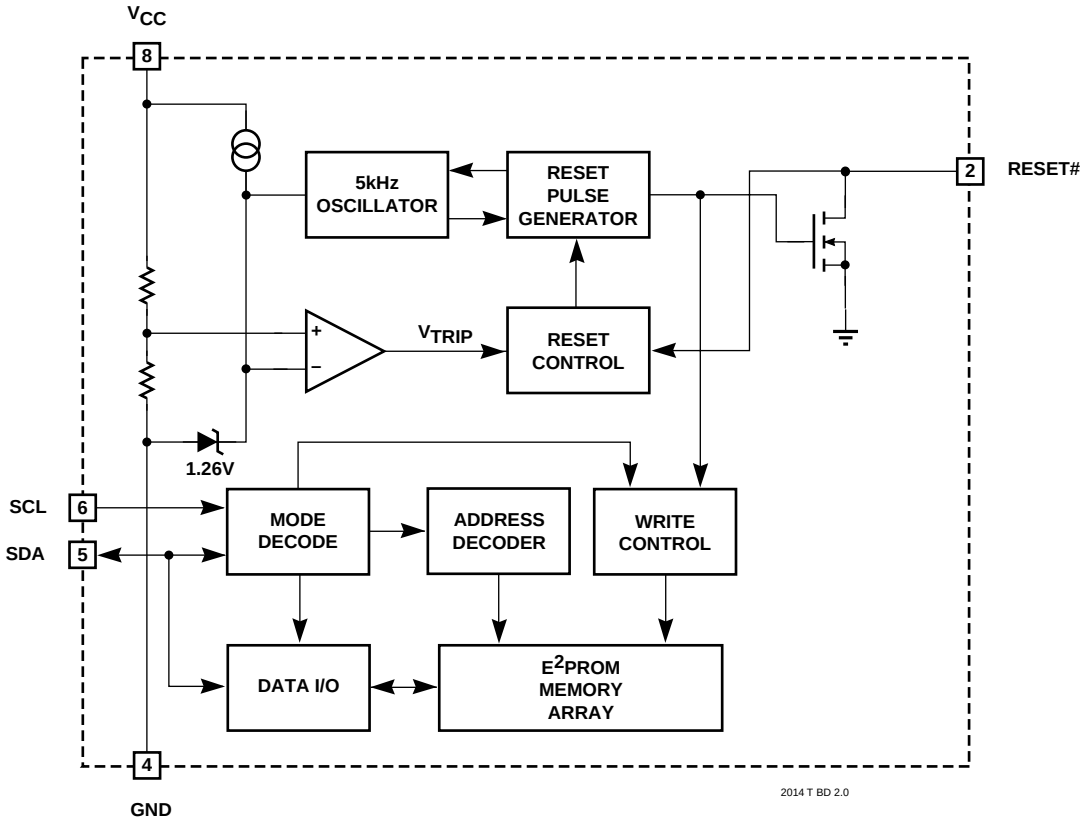
- Precision Supply Voltage Monitor
  - — Active Low
  - — Integrated memory write lockout
- Guaranteed RESET (RESET#) assertion to V_{CC} = 1V
- Power-Fail Accuracy Guaranteed
- No External Components
- 3V and 5V system versions
- Low Power CMOS
  - — Active current less than 3mA
  - — Standby current less than 25µA
- Memory Internally Organized 2k X 8
  - — Two Wire Serial Interface (I²C™)
    - – Bidirectional data transfer protocol
    - – Standard 100KHz and Fast 400KHz
- High Reliability
  - — Endurance: 100,000 erase/write cycles
  - — Data retention: 100 years
- 8-Pin PDIP or SOIC Packages

OVERVIEW

The S24163 is a power supervisory device with 16,384-bits of serial E²PROM. It is fabricated using SUMMIT's advanced CMOS E²PROM technology and is suitable for both 3 and 5 volt systems.

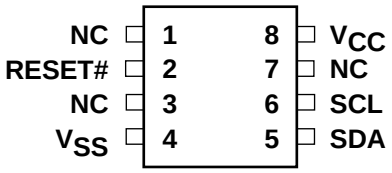
The S24163 is internally organized as 2048 x 8. It features the I²C serial interface and software protocol allowing operation on a simple two-wire bus.

BLOCK DIAGRAM



PIN CONFIGURATION

SMS24163
8-Pin PDIP
or 8-Pin SOIC



2014 T PCon 2.0

PIN DESCRIPTIONS

SCL — Serial Clock: The SCL input is used to clock data into and out of the device. In the WRITE mode data must remain stable while SCL is HIGH. In the READ mode data is clocked out on the falling edge of SCL.

SDA — Serial Data: The SDA pin is a bidirectional pin used to transfer data into and out of the device. Data may change only when SCL is LOW, except START and STOP conditions. It is an open-drain output and may be wire-ORed with any number of open-drain or open-collector outputs.

RESET# — Reset: This is an active low open drain output. It is driven low whenever V_{CC} is below V_{TRIP}. It is also an input and can be used to debounce a switch input or perform signal conditioning. The pin has an internal pull-up and should be left unconnected if the signal is not used in the system. However, an external pull-up resistor must be connected when the pin is tied to a system RESET# line.

V_{CC} — Power: V_{CC} is the voltage input, typically 2.7 to 5.5 volts.

GND — Ground: Power return.

NC — No Connect: The no connect inputs are not used. However, to ensure proper operation, they can be unconnected or tied to ground. They must not be tied to V_{CC}.

ENDURANCE AND DATA RETENTION

The S24163 is designed for applications requiring up to 100,000 erase/write cycles and unlimited read cycles. It provides 100 years of secure data retention, with or without power applied, after the execution of 100,000 erase/write cycles.

APPLICATIONS

The S24163 is ideal for applications requiring low voltage and low power consumption. This device provides microcontroller RESET control and can be manually resettable. This device also uses a cost effective, space-saving, 8-pin SOIC or PDIP plastic package. Typical applications include alarm devices, electronic locks, meters, keys, pagers and cellular phones.

RESET CONTROLLER DESCRIPTION

The device provides a precise reset output to a microcontroller and it's associated circuitry ensuring correct system operation during power-up/down conditions and brownout situations. The output is open drain, allowing control of the reset function by multiple devices.

During power-up the reset output remains in a fixed active state until V_{CC} passes through the reset threshold and remains above the threshold for 200ms. The reset output is valid whenever $V_{CC} \geq 1V$. If V_{CC} falls below the threshold for more than t_{GLITCH} the device will immediately generate a reset and drive the output.

The reset pin is an I/O; therefore, forcing the pin to the active state can also manually reset the device. Because the I/O needs to be an open drain, the internal timer can only be triggered by the leading edge of the input. The resulting reset output will either be t_{PURST}, or the externally applied reset signal, whichever is longer. This can provide an affective debounce or reset signal extender solution.

CHARACTERISTICS OF THE I^2C BUS

General Description

The I^2C bus was designed for two-way, two-line serial communication between different integrated circuits. The two lines are a serial data line (SDA), and a serial clock line (SCL). The SDA line must be connected to a positive supply by a pull-up resistor, located somewhere on the bus (See Figure 1). Data transfer between devices may be initiated with a START condition only when SCL and SDA are HIGH (bus is not busy).

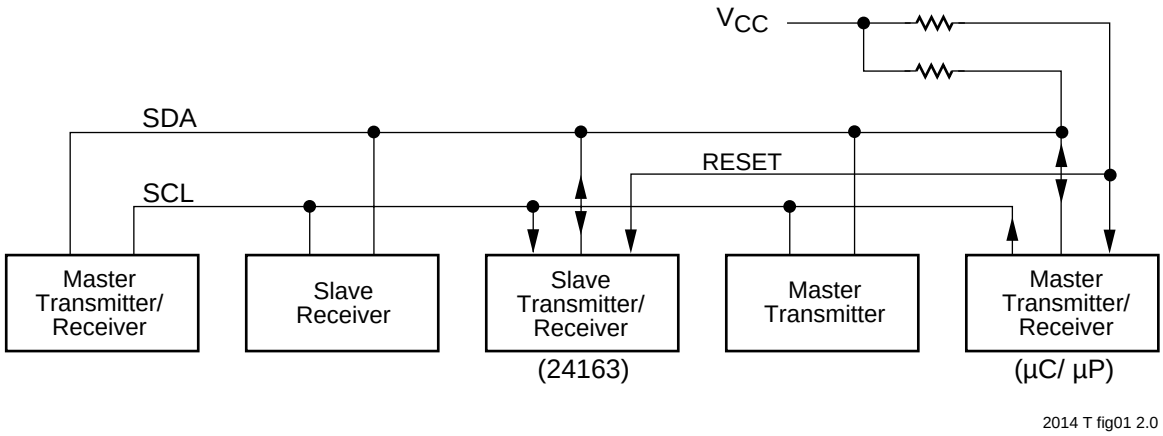


FIGURE 1. TYPICAL SYSTEM CONFIGURATION

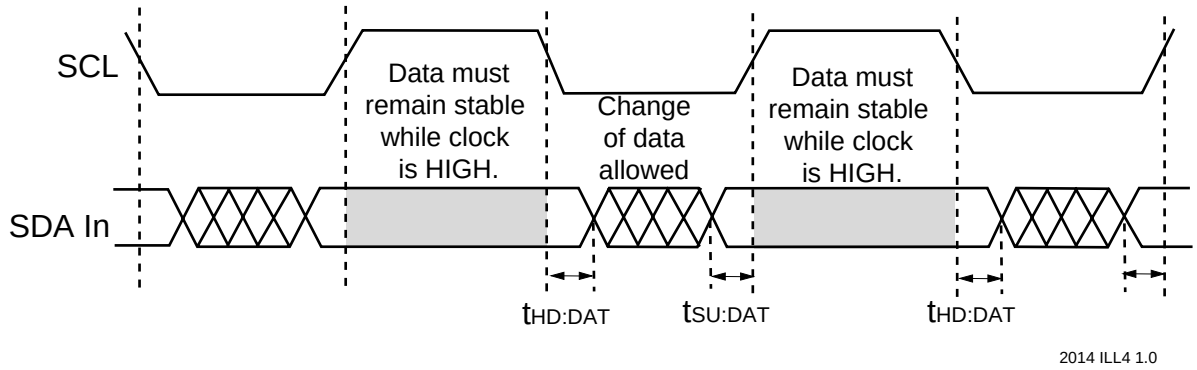


FIGURE 2. INPUT DATA PROTOCOL

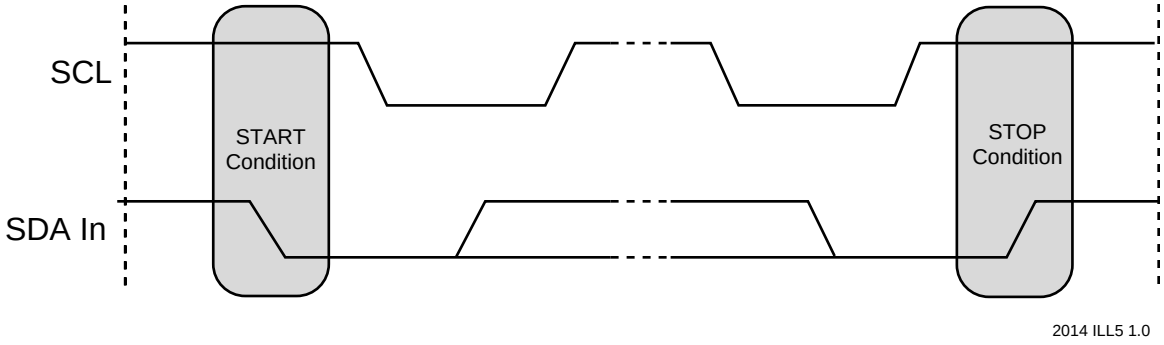


FIGURE 3. START AND STOP CONDITIONS

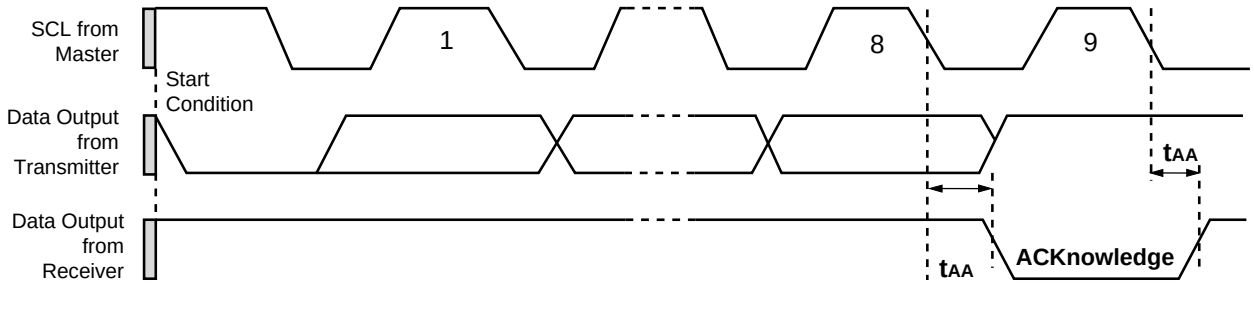


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

Input Data Protocol

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during clock HIGH time, because changes on the data line while SCL is HIGH will be interpreted as start or stop condition (See Figure 2).

START and STOP Conditions

When both the data and clock lines are HIGH, the bus is said to be not busy. A HIGH-to-LOW transition on the data line, while the clock is HIGH, is defined as the "START" condition. A LOW-to-HIGH transition on the data line, while the clock is HIGH, is defined as the "STOP" condition (See Figure 3).

DEVICE OPERATION

The S24163 is a 16,384-bit serial E^2PROM. The device supports the I^2C bidirectional data transmission protocol. The protocol defines any device that sends data onto the bus as a "transmitter" and any device which receives data as a "receiver." The device controlling data transmission is called the "master" and the controlled device is called the "slave." Since it never initiates any data transfers the S24163 is always a "slave" device.

Acknowledge (ACK)

Acknowledge is a software convention used to indicate successful data transfers. The transmitting device, either the master or the slave, will release the bus after transmitting eight bits. During the ninth clock cycle, the receiver will pull the SDA line LOW to ACKnowledge that it received the eight bits of data (See Figure 4).

The S24163 will respond with an ACKnowledge after recognition of a START condition and its slave address byte. If both the device and a write operation are selected, the S24163 will respond with an ACKnowledge after the receipt of each subsequent 8-bit word.

In the READ mode the S24163 transmits eight bits of data, then releases the SDA line, and monitors the line for an ACKnowledge signal. If an ACKnowledge is detected, and no STOP condition is generated by the master, the S24163 will continue to transmit data. If an ACKnowledge is not detected the S24163 will terminate further data transmissions and await a STOP condition before returning to the standby power mode.

Device Addressing

Following a start condition the master must output the address of the slave it is accessing. The most significant four bits of the slave address are the device type identifier (see figure 5). For the S24163 this is fixed as 1010[B_{HEX}].

Word Address

The next three bits of the slave address are an extension of the array's address and are concatenated with the eight bits of address in the word address field, providing direct access to the 2,048 X 8 array.

Read/Write Bit

The last bit of the data stream defines the operation to be performed. When set to "1" a read operation is selected; when set to "0" a write operation is selected.

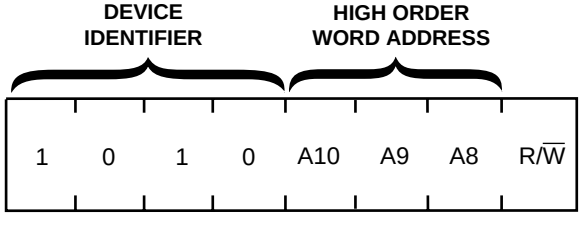


FIGURE 5. SLAVE ADDRESS BYTE

WRITE OPERATIONS

The S24163 allows two types of write operations: byte write and page write. The byte write operation writes a single byte during the nonvolatile write period (t_{WR}). The page write operation allows up to 16 bytes in the same page to be written during t_{WR}.

Byte WRITE

After the slave address is sent (to identify the slave device, specify high order word address and a read or write operation), a second byte is transmitted which contains the low 8 bit addresses of any one of the 2,048 words in the array.

Upon receipt of the word address, the S24163 responds with an ACKnowledge. After receiving the next byte of data, it again responds with an ACKnowledge. The master then terminates the transfer by generating a STOP condition, at which time the S24163 begins the internal write cycle.

While the internal write cycle is in progress, the S24163 inputs are disabled, and the device will not respond to any requests from the master. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

Page WRITE

The S24163 is capable of a 16-byte page write operation. It is initiated in the same manner as the byte-write operation, but instead of terminating the write cycle after the first data word, the master can transmit up to 15 more words of data. After the receipt of each word, the S24163 will respond with an ACKnowledge.

The S24163 automatically increments the address for subsequent data words. After the receipt of each word, the four low order address bits are internally incremented by one. The high order five bits of the address byte remain constant. Should the master transmit more than sixteen words, prior to generating the STOP condition, the address counter will "roll over," and the previously written data will be overwritten. As with the byte-write operation, all inputs are disabled during the internal write cycle. Refer to Figure 6 for the address, ACKnowledge and data transfer sequence.

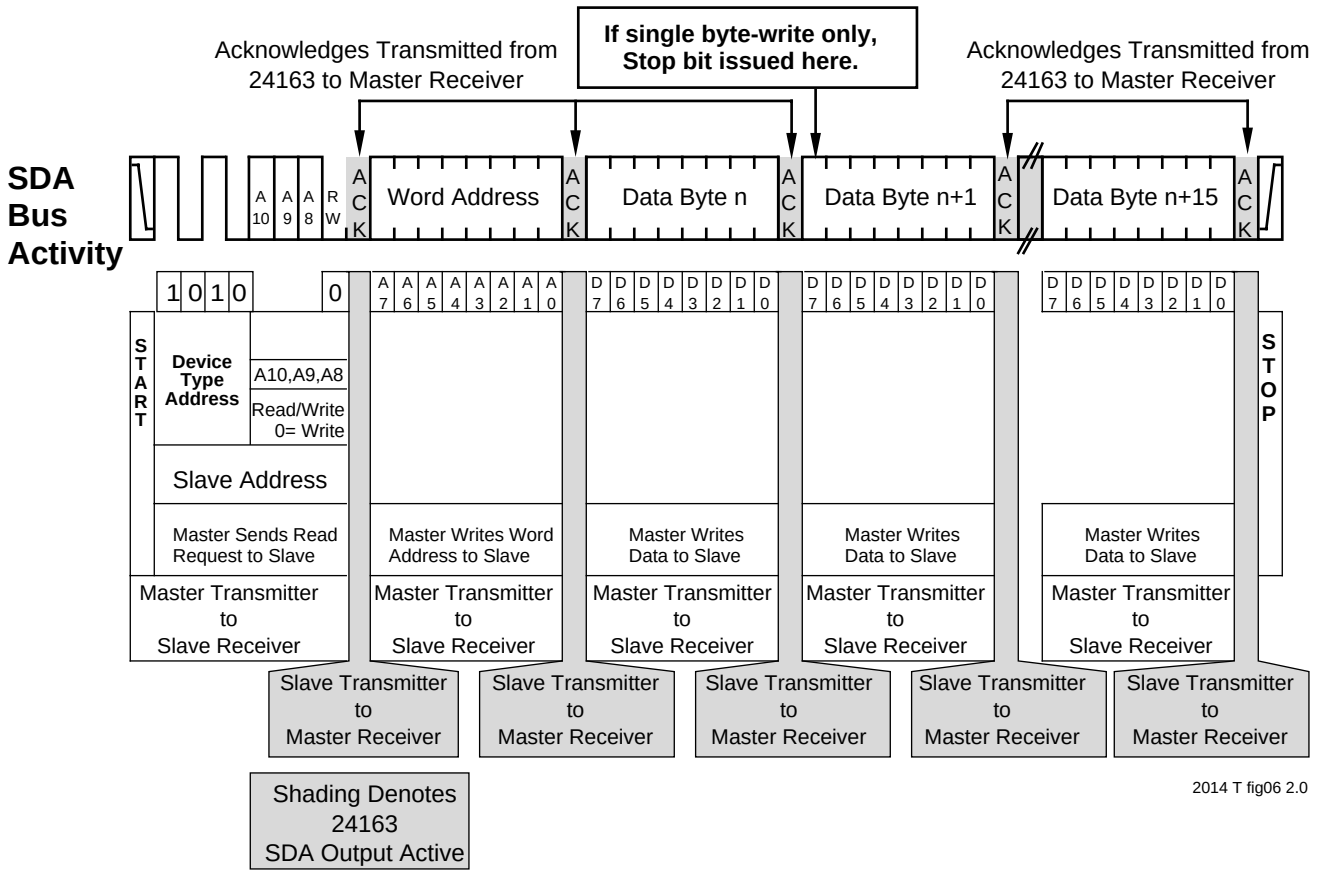


FIGURE 6. PAGE/BYTE WRITE MODE

Acknowledge Polling

When the S24163 is performing an internal WRITE operation, it will ignore any new START conditions. Since the device will only return an acknowledge after it accepts the START, the part can be continuously queried until an acknowledge is issued, indicating that the internal WRITE cycle is complete.

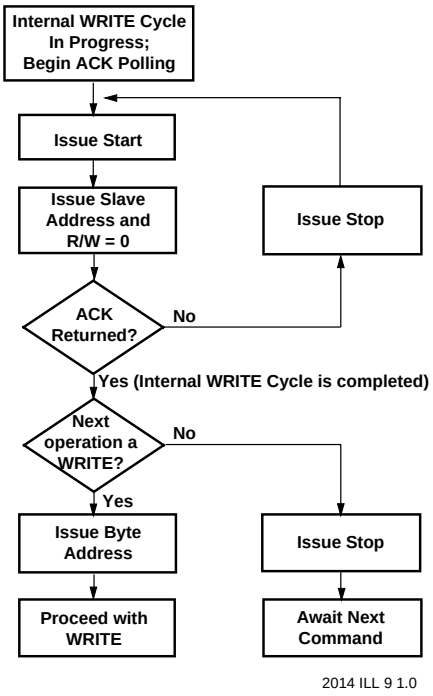


FIGURE 7. ACKNOWLEDGE POLLING

To poll the device, give it a START condition, followed by a slave address for a WRITE operation (See Figure 7).

READ OPERATIONS

Read operations are initiated with the R/W bit of the identification field set to "1." There are four different read options:

1. Current Address Byte Read
2. Random Address Byte Read
3. Current Address Sequential Read
4. Random Address Sequential Read

Current Address Byte Read

The S24163 contains an internal address counter which maintains the address of the last word accessed, incremented by one. If the last address accessed (either a read or write) was to address location n, the next read operation would access data from address location n+1 and increment the current address pointer. When the S24163 receives the slave address field with the R/W bit set to "1," it issues an acknowledge and transmits the 8-bit word stored at address location n+1.

The current address byte read operation only accesses a single byte of data. The master does not acknowledge the transfer, but does generate a stop condition. At this point, the S24163 discontinues data transmission. See Figure 8 for the address acknowledge and data transfer sequence.

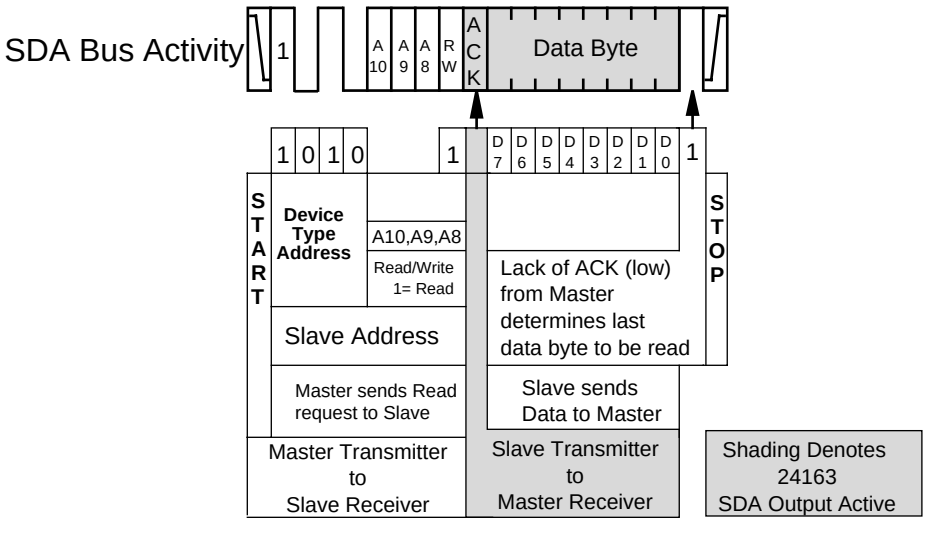


FIGURE 8. CURRENT ADDRESS BYTE READ MODE

Random Address Byte Read

Random address read operations allow the master to access any memory location in a random fashion. This operation involves a two-step process. First, the master issues a write command which includes the start condition and the slave address field (with the R/W bit set to WRITE) followed by the address of the word it is to read. This procedure sets the internal address counter of the S24163 to the desired address.

After the word address acknowledge is received by the master, the master immediately reissues a start condition followed by another slave address field with the R/W bit set to READ. The S24163 will respond with an acknowledge and then transmit the 8-data bits stored at the addressed location. At this point, the master does not acknowledge the transmission but does generate the stop condition. The S24163 discontinues data transmission and reverts to its standby power mode. See Figure 9 for the address, acknowledge and data transfer sequence.

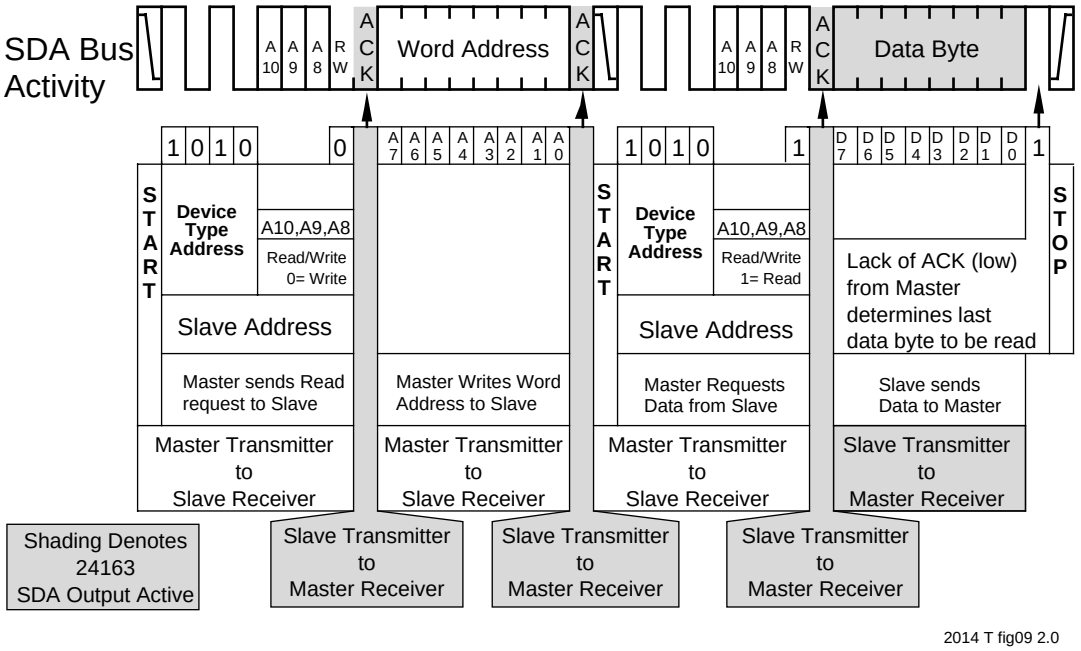


FIGURE 9. RANDOM ADDRESS BYTE READ MODE

Sequential READ

Sequential READs can be initiated as either a current address READ or random access READ. The first word is transmitted as with the other byte read modes (current address byte READ or random address byte READ); however, the master now responds with an ACKnowledge, indicating that it requires additional data from the S24163. The S24163 continues to output data for each ACKnowledge received. The master terminates the sequential READ operation by not responding with an ACKnowledge, and issues a STOP conditions.

During a sequential read operation, the internal address counter is automatically incremented with each acknowledge signal. For read operations, all address bits are incremented, allowing the entire array to be read using a single read command. After a count of the last memory address, the address counter will 'roll-over' and the memory will continue to output data. See Figure 10 for the address, acknowledge and data transfer sequence.

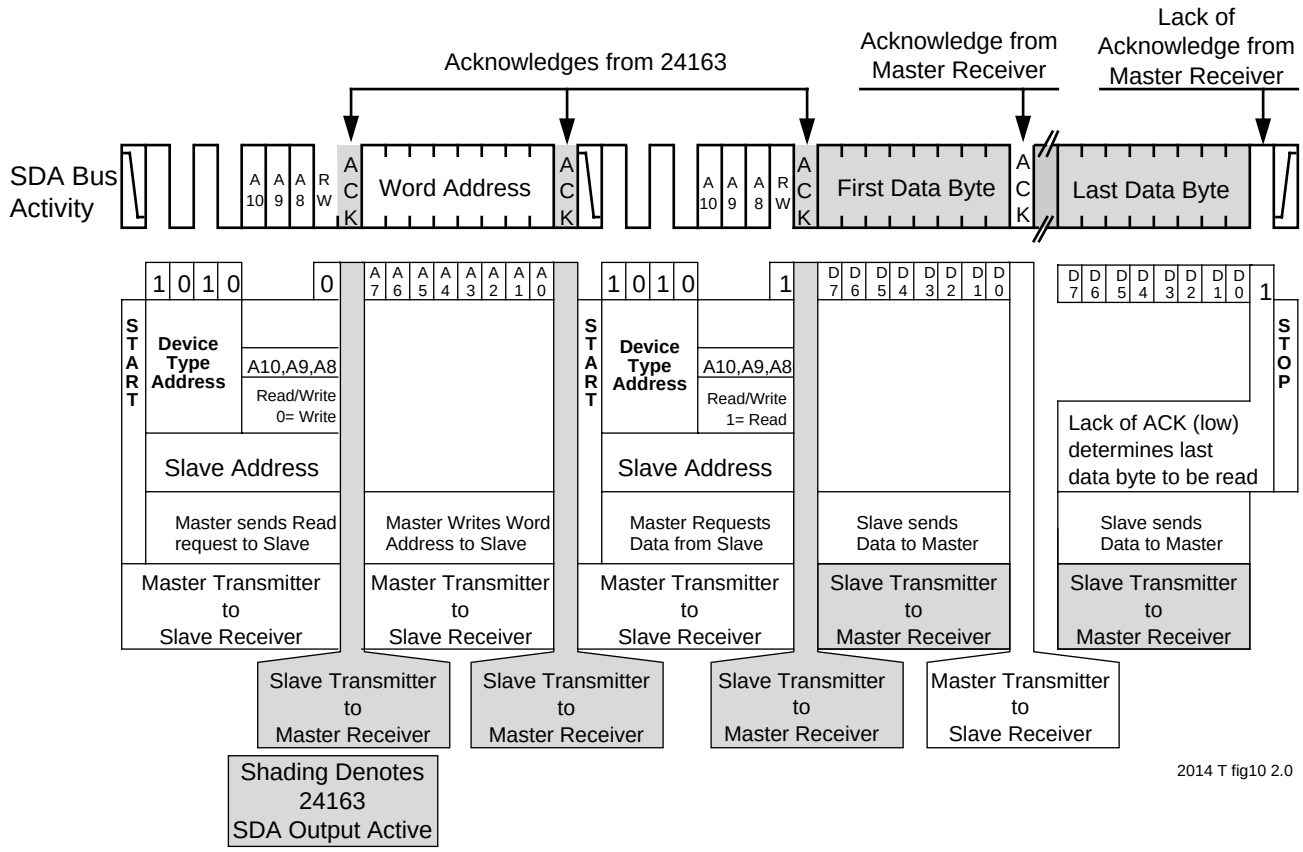


FIGURE 10. SEQUENTIAL READ OPERATION (starting with a Random Address READ)

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... -40°C to +85°C
Storage Temperature ..... -65°C to +125°C
Soldering Temperature (less than 10 seconds) ..... 300°C
Supply Voltage ..... 0 to 6.5V
Voltage on Any Pin ..... -0.3V to V_{CC}+0.3V
ESD Voltage (JEDEC method) 2,000V

NOTE: These are STRESS ratings only. Appropriate conditions for operating these devices are given elsewhere in this specification. Stresses beyond those listed here may permanently damage the part. Prolonged exposure to maximum ratings may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

S24163, T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
S24163-3, T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

Symbol	Parameter	Conditions		Min	Max	Units
I_{CC}	Supply Current (CMOS)	SCL = CMOS Levels @ 100KHz SDA = Open All other inputs = GND or V_{CC}	V_{CC} =5.5V		3	mA
			V_{CC} =3.3V		2	mA
I_{SB}	Standby Current (CMOS)	SCL = SDA = V_{CC} All other inputs = GND	V_{CC} =5.5V		50	µA
			V_{CC} =3.3V		25	µA
I_{LI}	Input Leakage	V_{IN} = 0 To V_{CC}			10	µA
I_{LO}	Output Leakage	V_{OUT} = 0 To V_{CC}			10	µA
V_{IL}	Input Low Voltage	S0, S1, S2, SCL, SDA, RESET			0.3xV_{CC}	V
V_{IH}	Input High Voltage	S0, S1, S2, SCL, SDA		0.7xV_{CC}		V
V_{OL}	Output Low Voltage	I_{OL} = 3mA			0.4	V

2014 PGM T1 1.0

AC ELECTRICAL CHARACTERISTICS

S24163, T_A = -40°C to +85°C, V_{CC} = 5V ± 10%
S24163-3, T_A = -40°C to +85°C, V_{CC} = 2.7V to 5.5V

			2.7V to 4.5V		4.5V to 5.5V		
Symbol	Parameter	Conditions	Min	Max	Min	Max	Units
f_{SCL}	SCL Clock Frequency		0	100		400	KHz
t_{LOW}	Clock Low Period		4.7		1.3		µs
t_{HIGH}	Clock High Period		4.0		0.6		µs
t_{BUF}	Bus Free Time	Before New Transmission	4.7		1.3		µs
$t_{SU:STA}$	Start Condition Setup Time		4.7		0.6		µs
$t_{HD:STA}$	Start Condition Hold Time		4.0		0.6		µs
$t_{SU:STO}$	Stop Condition Setup Time		4.7		0.6		µs
t_{AA}	Clock to Output	SCL Low to SDA Data Out Valid	0.3	3.5	0.2	0.9	µs
t_{DH}	Data Out Hold Time	SCL Low to SDA Data Out Change	0.3		0.2		µs
t_R	SCL and SDA Rise Time			1000		300	ns
t_F	SCL and SDA Fall Time			300		300	ns
$t_{SU:DAT}$	Data In Setup Time		250		100		ns
$t_{HD:DAT}$	Data In Hold Time		0		0		ns
T_I	Noise Spike Width @ SCL, SDA Inputs	Noise Suppression Time Constant		100		100	ns
t_{WR}	Write Cycle Time			10		10	ms

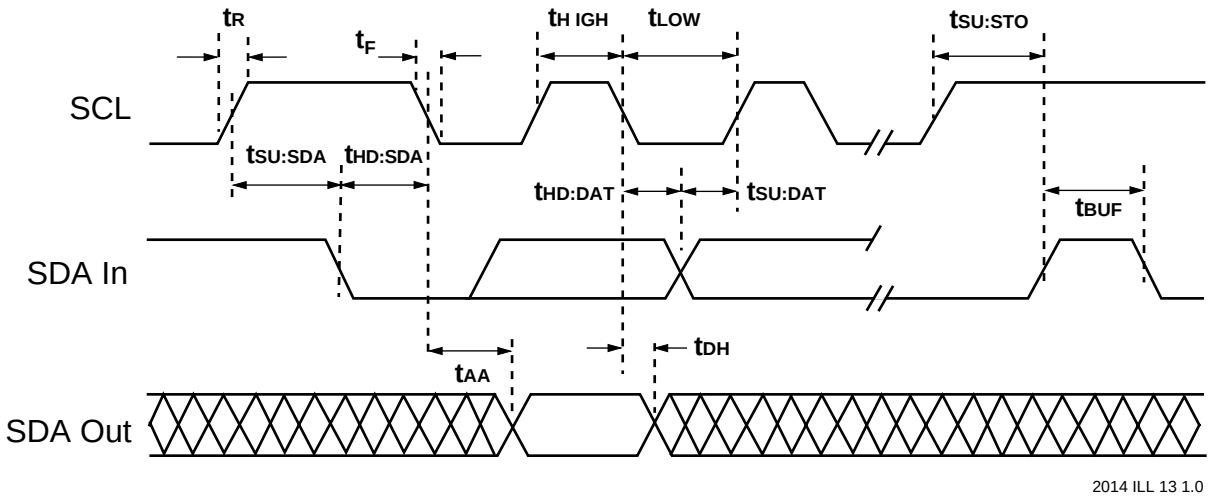
2014 PGM T2 1.0

CAPACITANCE

T_A = 25°C, f = 100KHz

Symbol	Parameter	Max	Units
C_{IN}	Input Capacitance	5	pF
C_{OUT}	Output Capacitance	8	pF

2014 PGM T3 1.0



2014 ILL 13 1.0

FIGURE 11. BUS TIMING

RESET CIRCUIT AC and DC ELECTRICAL CHARACTERISTICS

T_A = -40°C to +85°C

		S24163-2.7		S24163–A		S24163–B		
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Unit
V_{TRIP}	Reset Trip Point	2.55	2.7	4.25	4.5	4.5	4.75	V
t_{PURST}	Power-Up Reset Timeout	130	270	130	270	130	270	ms
t_{RPD}	V_{TRIP} to RESET Output Delay		5		5		5	µs
V_{RVALID}	RESET Output Valid	1		1		1		V
t_{GLITCH}	Glitch Reject Pulse Width		30		30		30	ns
V_{OLRS}	RESET Output Low Voltage I_{OL} – 1mA		0.4		0.4		0.4	V

2014 PGM T4 1.1

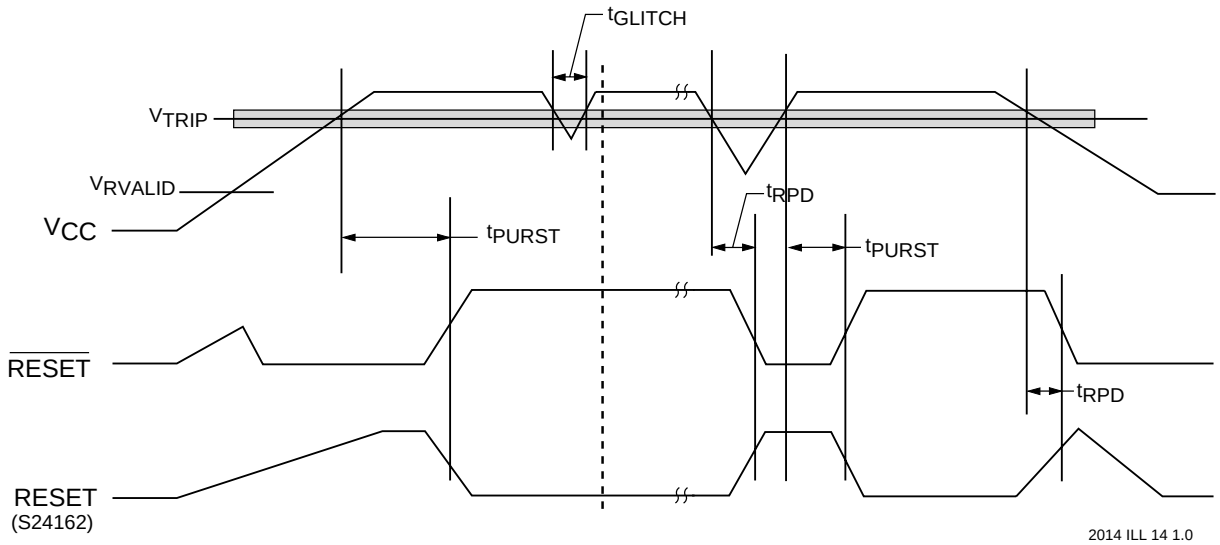
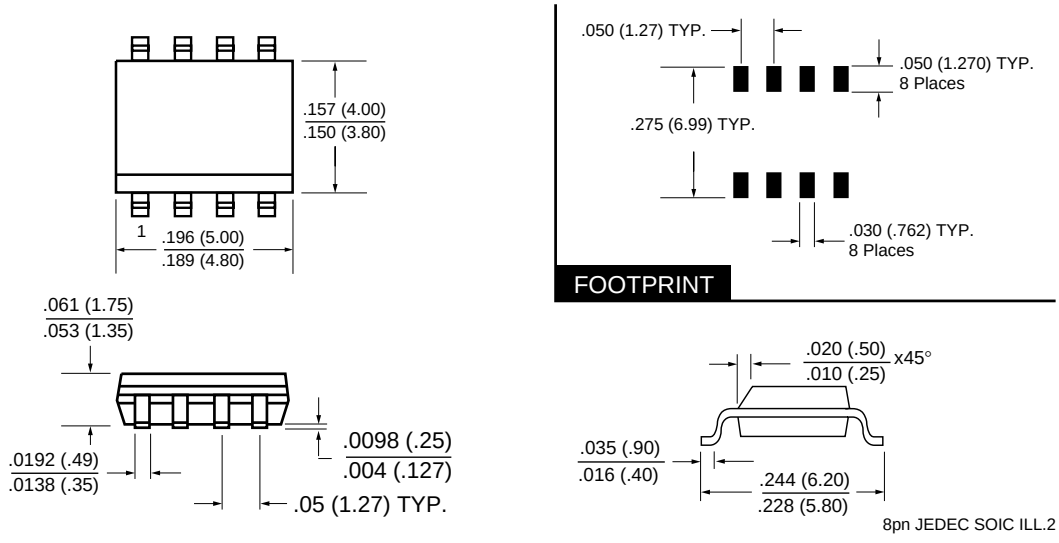
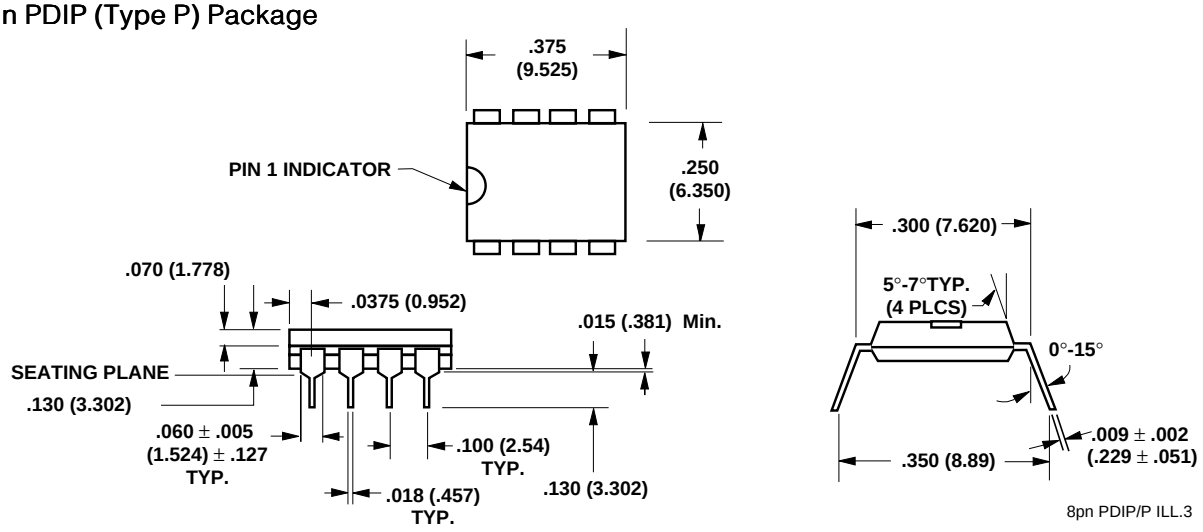


FIGURE 12. RESET OUTPUT TIMING

8 Pin SOIC (Type S) Package JEDEC (150 mil body width)



8 Pin PDIP (Type P) Package



8pn PDIP/P ILL.3

ORDERING INFORMATION

S24163 P A T

Base Part Number

Package

P = 8 Lead PDIP
S = 8 Lead 150mil SOIC

Tape & Reel Option
Blank = Tube
T = Tape & Reel

Operating Voltage Range
A = 4.5V to 5.5V V_{TRIP} min. @ 4.25V
B = 4.5V to 5.5V V_{TRIP} min. @ 4.50V
2.7 = 2.7V to 5.5V V_{TRIP} min. @ 2.55V

2014 Tree 2.0