

PRODUCT CATALOG

N-CHANNEL ENHANCEMENT MOS FET

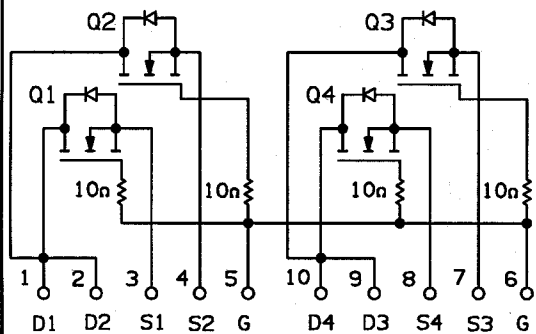
500V, 86A, 0.07 Ω

SDF85NA50 HI
SDF85NA50 JD

FEATURES

- RUGGED PACKAGE
- HI-REL CONSTRUCTION
- CERAMIC EYELETS
- LEAD BENDING OPTIONS
- COPPER CORED 52 ALLOY PINS
- LOW IR LOSSES
- LOW THERMAL RESISTANCE
- OPTIONAL MIL-STD-883 SCREENING

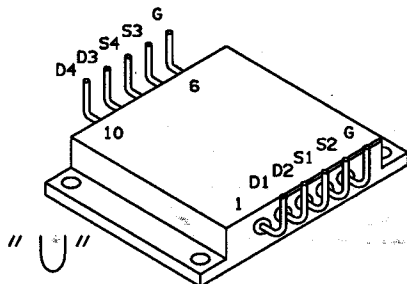
SCHEMATIC



(CUSTOM SCHEMATIC OPTIONS AVAILABLE)

STANDARD BEND CONFIGURATION

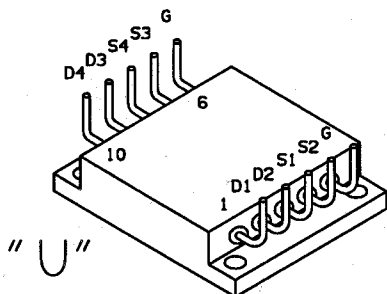
HI



(CUSTOM BEND OPTIONS AVAILABLE)

STANDARD BEND CONFIGURATION

JD



(CUSTOM BEND OPTIONS AVAILABLE)

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL		UNITS
DRAIN-SOURCE VOLTAGE	V _{DSS}	500	V _{dc}
DRAIN-GATE VOLTAGE (R _{GS} =1.0M Ω)	V _{DGR}	500	V _{dc}
GATE-SOURCE VOLTAGE CONTINUOUS	V _{GS}	± 20	V _{dc}
DRAIN CURRENT CONTINUOUS (T _c = 25°C)	I _D	85	A _{dc}
DRAIN CURRENT PULSED	I _{DM}	340	A
TOTAL POWER DISSIPATION	P _D	850	W
POWER DISSIPATION DERATING > 25°C		6.67	W/°C
OPERATING & STORAGE TEMP.	T _J /T _{sig}	-55 TO +150	°C
THERMAL RESISTANCE	R _{thJc}	0.15	°C/W
MAX. LEAD TEMPERATURE	T _L	300	°C

ELECTRICAL CHARACTERISTICS T_c = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNITS
Drain-source Breakdown Volt.	V(BR) _{DSS}	V _{GS} =0V I _D =250 μ A	500	-	-	V
Gate Threshold Voltage	V _{GS} (TH)	V _D =V _{GS} I _D =250 μ A	2.0	-	4.0	V
Gate Source Leakage	I _{GSS}	V _{GS} = ± 20 V	-	-	100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _D =MAX. RATING V _{GS} =0	-	-	250	μ A
		V _D =0.8 MAX. RATING V _{GS} =0 T _J =125°C	-	-	1000	μ A
Static Drain-Source On-State Resistance(1)	R _{DS} (ON)	V _{GS} =10 V I _D =12A	-	-	.27	Ω
Forward Trans-Conductance (2)	g _{fs}	V _D $\geq$ 50 V I _D =12A	13	-	-	S(U)
Input Capacitance	C _{ISS}	V _{GS} =0V V _D =25 V f=1.0 MHz	-	4100	-	pF
Output Capacitance	C _{OSS}		-	480	-	pF
Reverse Transfer Capacitance	C _{RSS}		-	84	-	pF
Turn-On Delay	t _d (on)	V _D =250V R _G =4.3n I _D =21A R _D =12n	-	-	35	ns
Rise Time	t _r	(MOSFET switching times are essentially independent of operating temp.)	-	-	120	ns
Turn-Off Delay	t _d (off)		-	-	130	ns
Fall Time	t _f		-	-	98	ns
Total Gate Charge (Gate-Source Plus Gate-Drain)	Q _g	V _{GS} =10V, I _D =21A	-	-	190	nC
Gate-Source Charge	Q _{gs}	V _D =0.8 MAX. RATING (Gate charge is essentially independent of the operating temperature)	-	-	27	nC
Gate-Drain ("Miller") Charge	Q _{gd}		-	-	93	nC

TOTAL MODULE RATINGS AND CHARACTERISTICS T_c = 25°C (UNLESS OTHERWISE SPECIFIED)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNITS
PIN-CASE ISOLATION	PCI	V _{CASE} -PINS ALL PINS SHORTED TO CASE	10	-	m Ω
STATIC DRAIN-SOURCE ON-STATE VOLTAGE	V _{DS} (ON)	V _{GS} $\geq$ 10V I _D = 85A	-	5.0	V
STATIC DRAIN-SOURCE ON-STATE RESISTANCE	R _{DS} (ON)	V _{GS} = 10V I _D = 42A	-	0.05	OHM
ZERO GATE VOLTAGE DRAIN CURRENT	I _{DSS}	V _{GS} = 0V V _D = 500V	-	1.0	mA

- (1) T_J = 25°C TO 150°C.
- (2) PULSE TEST: PULSE WIDTH < 300 μ S, DUTY CYCLE < 2%.
- (3) TEST ARE PERFORMED AT ELEMENT EVALUATION. TEST CONDITIONS AND LIMITS APPLY TO EACH MOSFET SEPARATELY.