OC-48 SONET/SDH/ATM 4-BIT TRANSCEIVER S3457

FEATURES

- SiGe BiCMOS Technology
- Complies with Bellcore and ITU-T specifications
- 4-bit LVDS data path at 622.08 Mbps
- On-chip high-frequency PLL for clock generation
- Supports OC-48 (2488.32 Mbps)
- Reference frequency of 155.52 MHz
- Diagnostic loopback mode
- Supports line timing
- Lock detect
- Signal detect input
- Low jitter LVDS interface
- Internal FIFO to decouple transmit clocks
- Single 3.3V supply
- Typical power 1.5 W
- Compact 128 TQFP package

APPLICATIONS

- Wavelength Division Multiplex (WDM) equipment
- SONET/SDH-based transmission systems
- SONET/SDH modules
- SONET/SDH test equipment
- ATM over SONET/SDH
- Section repeaters
- Add Drop Multiplexers (ADM)
- Broad-band cross-connects
- Fiber optic terminators
- Fiber optic test equipment

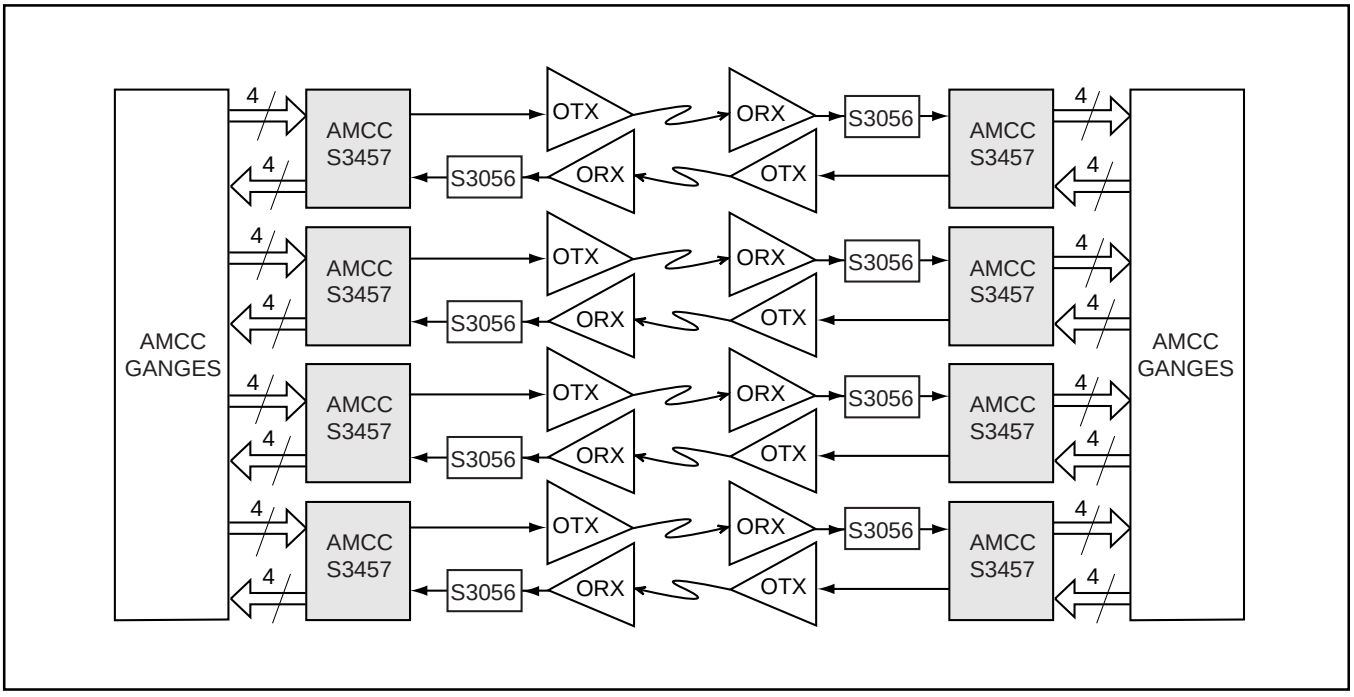
GENERAL DESCRIPTION

The S3457 SONET/SDH transceiver chip is a fully integrated serialization/deserialization SONET OC-48 (2488.32 Mbps) interface device. The S3457 receives an OC-48 scrambled NRZ signal. The chip performs all necessary serial-to-parallel and parallel-to-serial functions in conformance with SONET/SDH transmission standards. The device is suitable for SONET-based WDM applications. Figure 1 shows a typical network application.

On-chip clock synthesis is performed by the high-frequency phase-locked loop on the S3457 transceiver chip allowing the use of a slower external transmit clock reference. The chip can be used with a 155.52 MHz reference clock, in support of existing system clocking schemes.

The low jitter LVDS interface guarantees compliance with the bit-error rate requirements of the Bellcore and ITU-T standards. The S3457 is packaged in a compact 128 TQFP, offering designers a small package outline.

Figure 1. System Block Diagram



SONET OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, forms a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3457 chip supports the OC-48 rate (2.488 Gbps).

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for the STS-48 consists of 144 transport overhead bytes followed by the Synchronous Payload Envelope (SPE) bytes. This pattern of 144 overhead and 4176 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.) For more details on SONET operations, refer to the Bellcore SONET standard document.

Figure 2. SONET Structure

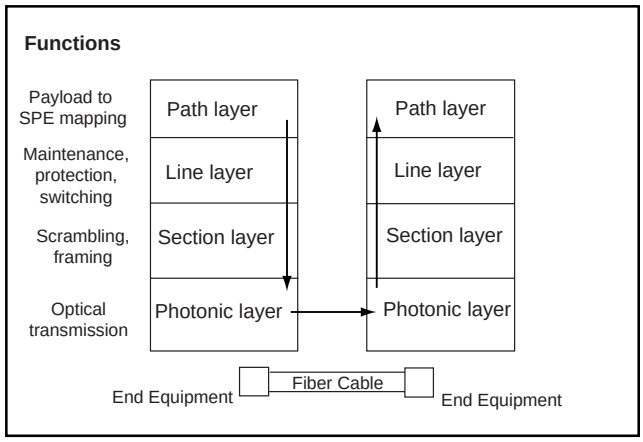
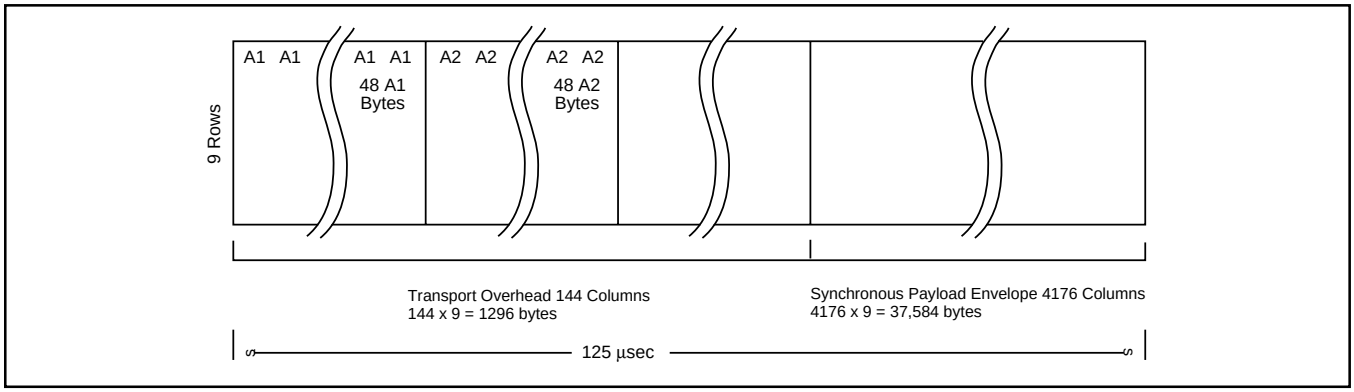


Table 1. SONET Signal Hierarchy

Elec.	CCITT	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24	STM-8	OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Figure 3. STS–48/OC–48 Frame Format



S3457 OVERVIEW

The S3457 transceiver implements SONET/SDH serialization/deserialization, and transmission functions. The block diagram in Figure 4 shows the basic operation of the chip. This chip can be used to implement the front end of SONET equipment, which consists primarily of the serial transmit interface and the serial receive interface. The chip handles all the functions of these two elements, including parallel-to-serial and serial-to-parallel conversion, clock generation, and system timing. The system timing circuitry consists of management of the data stream and clock distribution throughout the front end.

The S3457 is divided into a transmitter section and a receiver section. The sequence of operations is as follows:

Transmitter Operations:

1. 4-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver Operations:

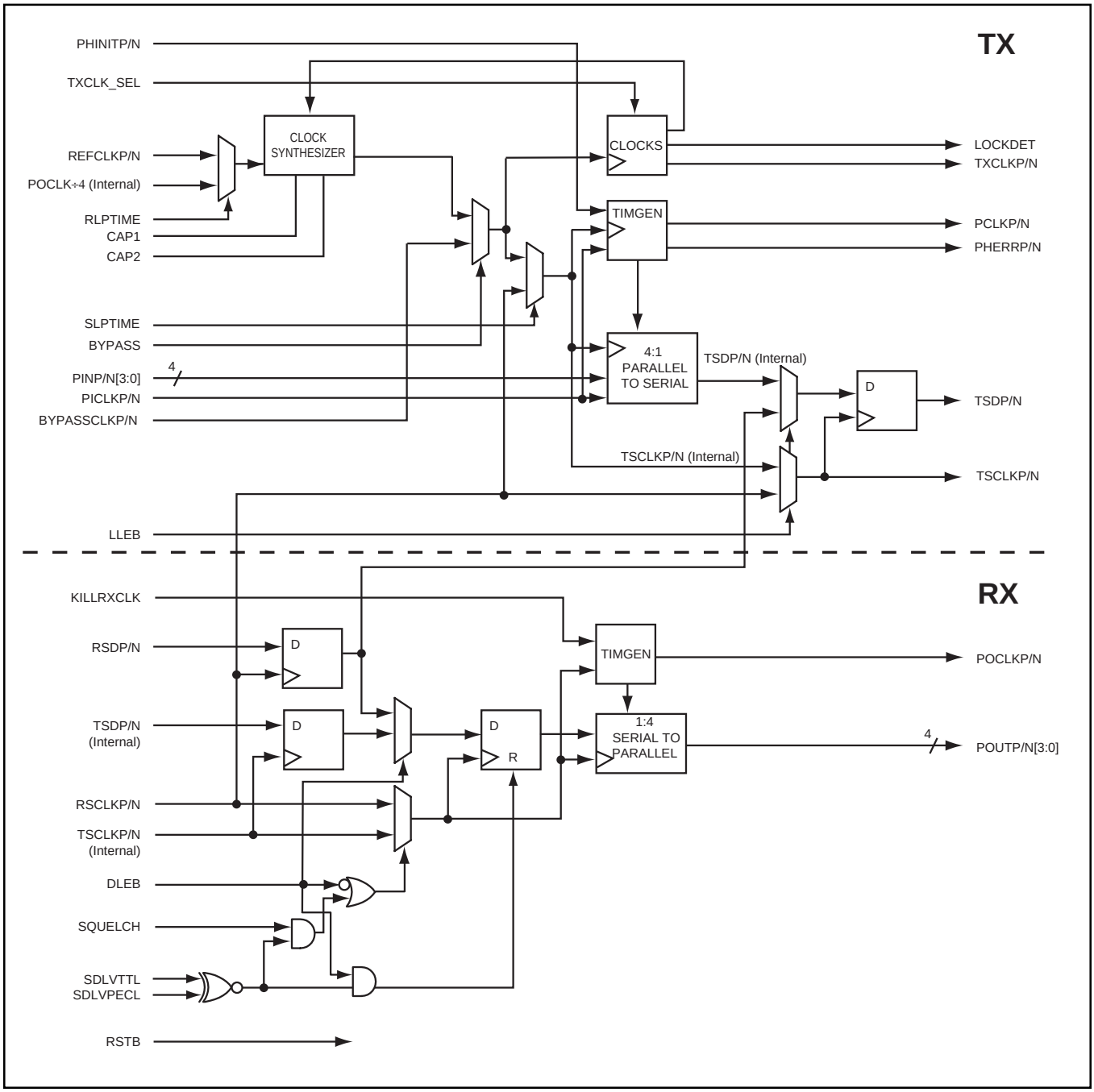
1. Serial input
2. Serial-to-parallel conversion
3. 4-bit parallel output

Internal clocking and control functions are transparent to the user.

Suggested Interface Devices

AMCC	S3056	OC-48 Clock Recovery Device
AMCC	S19202	STS-192 POS/ATM SONET/SDH Mapper

Figure 4. S3457 Transceiver Functional Block Diagram



S3457 TRANSCEIVER FUNCTIONAL DESCRIPTION

TRANSMITTER OPERATION

The S3457 transceiver chip performs the serialization stage in the processing of a transmit SONET STS-48 data stream. It converts 4-bit parallel data into bit-serial format at 2488.32 Mbps.

A high-frequency bit clock can be generated from a 155.52 MHz frequency reference by using an integral frequency synthesizer containing a Phase-Locked Loop (PLL) circuit with a divider in the loop.

Diagnostic loopback (transmitter to receiver) and line loopback (receiver to transmitter) is provided. See *Other Operating Modes*.

Clock Synthesizer

The clock synthesizer, shown in the block diagram in Figure 4, is a monolithic PLL that generates the serial output clock frequency locked to the input Reference Clock (REFCLKP/N).

The REFCLKP/N input must be generated from a crystal oscillator which has a frequency accuracy that meets the value stated in Table 7 in order for the Transmit Serial Clock (TSCLK) frequency to have the same accuracy required for operation in a SONET system. Lower accuracy crystal oscillators may be used in applications less demanding than SONET/SDH.

The on-chip PLL consists of a phase detector, which compares the phase relationship between the Voltage Controlled Oscillator (VCO) output and the REFCLKP/N input, a loop filter which converts the phase detector output into a smooth DC voltage, and a VCO, whose frequency is varied by this voltage.

The loop filter generates a VCO control voltage based on the average DC level of the phase discriminator output pulses. A single external clean-up capacitor is utilized as part of the loop filter. The loop filter's corner frequency is optimized to minimize output phase jitter.

Table 2. Reference Jitter Limits

Frequency Band	Maximum Reference Clock Jitter
12 kHz to 20 MHz	-61 dBc

Timing Generator

The timing generation function, seen in Figure 4, provides a divide by 4 version of the transmit serial clock. This circuitry also provides an internally generated load signal, which transfers the PINP/N[3:0] data from the FIFO to the serial shift register.

The Parallel Clock (PCLK) output is a 4-bit parallel rate version of the transmit serial clock (divide by 4). PCLK is intended for use as a 4-bit parallel clock for upstream multiplexing and overhead processing circuits. Using PCLK for upstream circuits will ensure a stable frequency and phase relationship between the data coming into and leaving the S3457 device.

The timing generator also produces a feedback reference clock to the clock synthesizer. A counter divides the synthesized clock down to the same frequency as the Reference Clock (REFCLK). The PLL in the clock synthesizer maintains the stability of the synthesized clock by comparing the phase of the internal clock with that of the REFCLK. The modulus of the counter is a function of the reference clock frequency and the operating frequency.

Parallel-to-Serial Converter

The parallel-to-serial converter shown in Figure 4 is comprised of a FIFO and a parallel-to-serial register. The FIFO input latches the data from the PINP/N[3:0] bus on the rising edge of Parallel Input Clock (PICLK). The parallel-to-serial register is a loadable shift register which takes its parallel input from the FIFO output.

An internally generated divide-by-4 clock, which is phase aligned to the TSCLK as described in the timing generator description, activates the parallel data transfer between registers. The serial data is shifted out of the parallel-to-serial register at the TSCLK rate.

FIFO

A FIFO is added to decouple the internal and external (PICLK) clocks. The internally generated divide-by-4 clock is used to clock out data from the FIFO. Phase Initialization (PHINITP/N) and Lock Detect (LOCKDET) are used to center or reset the FIFO. The PHINITP/N and LOCKDET signals will center the FIFO after the third PICLK pulse. This is in order to insure that PICLK is stable. This scheme allows the user to have an infinite PCLK to PICLK delay through the ASIC. Once the FIFO is centered, the PCLK to PICLK delay can have a maximum drift as specified in Table 18. See Figure 12.

FIFO Initialization

The FIFO can be initialized in one of the following three ways:

1. During power up, once the PLL has locked to the reference clock provided on the REFCLK pins, the LOCKDET will go active and initialize the FIFO.
2. When Reset (RSTB) goes active, the entire chip is reset. This causes the PLL to go out of lock and thus the LOCKDET goes inactive. When the PLL reacquires the lock, the LOCKDET goes active and initializes the FIFO. Note: PCLK is held reset when RSTB is active.
3. The user can also initialize the FIFO by raising PHINIT.

During the normal running operation, the incoming data is passed from the PICLK timing domain to the internally generated divide by 4 clock timing domain. Although the frequency of PICLK and the internally generated clock is the same, their phase relationship is arbitrary. To prevent errors caused by short setup or hold times between the two timing domains, the timing generator circuitry monitors the phase relationship between PICLK and the internally generated clock. When a potential setup or hold time violation is detected, the Phase Error (PHERR) pulses high for one PCLK period. If the condition persists, PHERR will remain high. When PHERR conditions occur, PHINIT should be activated to recenter the FIFO (at least 2 PCLK periods). This can be done by connecting PHERR to PHINIT. When realignment occurs up to 10 bytes of data will be lost. The user can also take in the PHERR signal, process it and send an output to PHINIT in such a way that idle bytes are lost during the realignment process. PHERR will go inactive when the realignment is complete.

RECEIVER OPERATION

The S3457 transceiver chip provides the first stage of the digital processing of a receive SONET STS-48 bit-serial stream. It converts the bit-serial 2.488 Gbps data stream into a 4-bit parallel data format. A loopback mode is provided for diagnostic loopback (transmitter to receiver). A line loopback (receiver to transmitter) is also provided. Both line and diagnostic loopback modes can be active at the same time.

Serial-to-Parallel Converter

The serial-to-parallel converter consists of two 4-bit registers. The first is a serial-in, parallel-out shift register, which performs serial-to-parallel conversion.

The S3457 converts the bit-serial 2.488 Gbps data stream into a 622.08 Mbps 4-bit wide parallel data format. The serial data and clock inputs are differential CML and are internally biased and terminated signals. The rising edge of the positive serial clock is synchronous with the input data transitions. Parallel output clock and data are LVDS signals at 622.08 Mbps. The falling edge of the Positive Output Clock (POCLK) is synchronous with the output parallel register which drives POUTP/N[3:0].

OTHER OPERATING MODES

Diagnostic Loopback

When the Diagnostic Loopback Enable (DLEB) input is active, a loopback from the transmitter to the receiver at the serial data rate can be set up for diagnostic purposes. The differential serial output data and clock from the transmitter are routed to the serial-to-parallel block in place of the normal Receive Serial Data (RSD) and Receive Serial Clock (RSCLK). TSD/TSCLK outputs are active. DLEB takes precedence over SDLVPECL and SDLVTTL.

Line Loopback

The line loopback circuitry selects the source of the data and clock which is output on TSD and TSCLK. When the Line Loopback Enable (LLEB) input is inactive, it selects the data and clock from the parallel to serial converter block. When LLEB is active, it forces the output data multiplexer to select the data and clock from the RSD and RSCLK inputs, and a receive-to-transmit loopback can be established at the serial data rate. Diagnostic loopback and line loopback can be active at the same time.

Loop Timing

In Serial Loop Timing (SLPTIME) mode, the clock synthesizer PLL of the S3457 is bypassed, and the timing of the entire transmitter section is controlled by the RSCLKP/N. This mode is entered by setting the SLPTIME input to an LVTTL High level.

In this mode the REFCLKP/N input is not used. It should be carefully noted that the internal PLL continues to operate in this mode, and continues as the source for the TXCLKP/N, and if this signal is being used, the REFCLKP/N input must be properly driven.

In Reference Loop Timing (RLPTIME) mode, the parallel clock from the receiver (POCLKP/N) is used as the reference clock to the transmitter. In this mode, the REFCLKP/N input is not used. The TXCLKP/N is generated from the POCLKP/N in this operating mode.

"Squelched Clock" Operation

Some integrated optical receiver/clock recovery modules force their recovered serial receive clock output to the logic zero state if the optical signal is removed or reduced below a fixed threshold. This condition is accompanied by the expected deassertion of the signal detect output.

The S3457 has been designed for operation with clock recovery devices that provide a continuous serial clock for seamless downstream clocking in the event of optical signal loss.

For operation with an optical transceiver that provides the "squelched clock" behavior as described above, the S3457 can be operated in the "squelched clock" mode by activating the SQUELCH pin.

In this condition, the receive serial clock RSCLKP/N is used for all receiver timing when the SDLVPECL/SDLVTTL inputs are in the active state. When the SDLVPECL/SDLVTTL inputs are placed in the inactive state (usually by the deassertion of LOCKDET or signal detect from the optical transceiver/clock recovery unit) the transmitter serial clock will be used to maintain timing in the receiver section. This will allow the POCLK to continue to run and the parallel outputs to flush out the last received characters and then assume the all zero state imposed at the serial data input.

It is important to note that in this mode there will be a one time shortening or lengthening of the POCLK cycle, resulting in an apparent phase shift in the POCLK at the deassertion of the SD condition. Another similar phase shift will occur when the SD condition is reasserted.

In the normal operating mode with SQUELCH inactive, there will be no phase discontinuities at the POCLK output during signal loss or reacquisition (assuming operation with continuous clocking from the CRU device such as the AMCC S3040, S3050, or S3056).

Table 3. S3457 Transmitter Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
PINP0 PINN0 PINP1 PINN1 PINP2 PINN2 PINP3 PINN3	LVDS	I	63 64 66 67 68 69 71 72	Parallel Input Data, aligned to the parallel input clock (PICLK). PINP/N[3] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit transmitted). PINP/N[0] is the least significant bit (corresponding to bit 3 of each PCM word, the last bit transmitted). PINP/N[3:0] is sampled on the rising edge of PICLK. Internally terminated.
PICLKP PICLKN	LVDS	I	61 62	Parallel Input Clock. A divide-by-4, nominally 50% duty cycle input clock, to which PINP/N[3:0] is aligned. PICLK is used to transfer the data on the PINP/N inputs into a holding register in the parallel-to-serial converter. The rising edge of PICLK samples PINP/N[3:0]. Internally terminated.
CAP1 CAP2	Analog	I	103 104	Transmitter Loop Filter Capacitor. The external loop filter capacitor and resistors are connected to these pins. See Figure 22.
PHINITP PHINITN	LVDS	I	74 73	Phase Initialization. Rising edge will realign internal timing. Internally terminated.
TXCLK_SEL	LVTTL	I	6	Transmit Clock Select. Used to select between the 155.52 MHz or 77.76 MHz clock on the TXCLKP/N output. A Low on TXCLK_SEL selects 155.52 MHz TXCLK, and a High on TXCLK_SEL selects 77.76 MHz TXCLK.
TSDP TSDN	Diff. CML	O	121 122	Transmit Serial Data. Differential CML serial data stream signals, normally connected to an optical transmitter module.
TSCLKP TSCLKN	Diff. CML	O	114 115	Transmit Serial Clock. Differential CML. Can be used to retime the TSD signal.
PCLKP PCLKN	LVDS	O	55 56	Parallel Clock. A reference clock generated by dividing the internal bit clock by 4. It is normally used to coordinate 4-bit wide transfers between upstream logic and the S3457 device.
PHERRP PHERRN	LVDS	O	57 58	Phase Error. Active High. Pulses High during each PCLK cycle for which there is a potential setup/hold timing violation between the internal byte clock and PICLK timing domains.
LOCKDET	LVTTL	O	83	Lock Detect. Goes High after the PLL has locked to the clock provided on the REFCLK pins. LOCKDET is an asynchronous output.

Table 4. S3457 Receiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RSDP RSDN	Differential CML	I	22 23	Receive Serial Data. Data stream signals normally connected to an optical receiver module. Internally biased and terminated.
RSCLKP RSCLKN	Differential CML	I	16 18	Receive Serial Clock. Used to supply a clock input for the RSDP/N inputs. Internally biased and terminated.
SDLVPECL	Single Ended LVPECL	I	12	LVPECL Signal Detect. LVPECL signal with an internal pull-down. Active High when SDLVTTL is held at a logic 0. A single-ended 10K LVPECL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVPECL is inactive, the data on the Receive Serial Data In (RSDP/N) pins will be internally forced to a constant zero. When SDLVPECL is active, data on the RSDP/N pins will be processed normally. When SDLVTTL is to be connected to the optical receiver module instead of SDLVPECL, then SDLVPECL should be tied High to implement an active Low signal detect, or left unconnected to implement an active High signal detect.
SDLVTTL	LVTTL	I	11	LVTTL Signal Detect. Active High when SDLVPECL is unconnected (logic 0). Active Low when SDLVPECL is tied high. A single-ended LVTTL input to be driven by the external optical receiver module to indicate a loss of received optical power. When SDLVTTL is inactive, the data on the RSDP/N pins will be internally forced to a constant zero. When SDLVTTL is active, data on the RSDP/N pins will be processed normally.
POUTP0 POUTN0 POUTP1 POUTN1 POUTP2 POUTN2 POUTP3 POUTN3	LVDS	O	30 31 35 36 39 40 41 42	Parallel Output data bus, aligned to the Parallel Output Clock (POCLKP/N). POUTP/N[3] is the most significant bit (corresponding to bit 1 of each PCM word, the first bit received). POUTP/N[0] is the least significant bit (corresponding to bit 4 of each PCM word, the last bit received). POUTP/N[3:0] is updated on the falling edge of POCLK.
POCLKP POCLKN	LVDS	O	44 45	Parallel Output Clock. A divide-by-4, nominally 50% duty cycle, parallel output clock that is aligned to the POUTP/N[3:0] 4-bit parallel output data. POUTP/N[3:0] is updated on the falling edge of POCLK.

Table 5. S3457 Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
REFCLKP REFCLKN	Internally Biased Diff. LVPECL	I	79 78	Reference Clock input. Used as the reference for the internal bit clock frequency synthesizer. Internally biased.
DLEB	LVTTL	I	9	Diagnostic Loopback Enable. Active Low. Selects diagnostic loopback. When DLEB is inactive, the S3457 device uses the primary data (RSD) and clock (RSCLK) inputs. When active, the S3457 device uses the diagnostic loopback clock and data from the transmitter. TSD/TSCLK is active in DLEB mode.
LLEB	LVTTL	I	7	Line Loopback Enable. Active Low. Selects line loopback. When LLEB is active, the S3457 will route the data from the RSD/RSCLK inputs to the TSD/TSCLK outputs.
KILLRXCLK	LVTTL	I	13	Kill Receive Clock input. Active Low. For normal operation, KILLRXCLK is High. When this input is Low, it will force the POCLK output to a logic "0" state.
SLPTIME	LVTTL	I	92	Serial Loop Time clock select input. Active High. When active, SLPTIME enables the recovered clock from the receive section to be used in place of the synthesized transmit clock.
RLPTIME	LVTTL	I	93	Reference Loop Time clock select input. Active High. When active, RLPTIME enables POCLK from the receiver to be used as the reference clock input to the transmitter.
SQUELCH	LVTTL	I	10	RSCLK Clock Squelch. Active High. When SQUELCH is active and SD is inactive, the transmit clock will be used in place of the RSCLK.
RSTB	LVTTL	I	8	Master Reset. Active Low. Reset input for the device. During reset, all clocks are disabled. RSTB should be low for a duration of one REFCLK cycle.
TXCLKP TXCLKN	Diff. LVPECL	O	3 2	Transmit Clock. 155.52 MHz/77.76 MHz Clock output from the clock synthesizer. This output should be connected to the reference clock input of the external clock recovery function.
BYPASSCLKP BYPASSCLKN	Differential CML	I	87 86	Bypass Clock. Provides an alternative serial clock bypassing the internal VCO. Internally biased and terminated.
BYPASS	LVTTL	I	95	Bypass Clock select. Active High. Selects between BYPASSCLKP/N and the VCO clock. REFCLKP/N must be high or low in the BYPASS mode. It should not be left floating.

Table 5. S3457 Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
AGND	GND		98, 99, 101, 102, 105, 106, 107, 109	Ground (0 V)
AVCC	+3.3 V		97, 100, 108	Power Supply
REFCLK_VCC	+3.3 V		80	Power Supply
REFCLK_GND	GND		77	Ground (0 V)
TXCORE_VCC	+3.3 V		52, 90, 127	Power Supply
TXCORE_GND	GND		51, 89, 126	Ground (0 V)
LVTTL_VCC	+3.3 V		5, 91	Power Supply
LVTTL_GND	GND		14, 94, 96	Ground (0 V)
CMOS_GND	GND		82	Ground (0 V)
CMOS_VCC	+3.3 V		84	Power Supply
NC			20, 25, 32, 33, 34, 47, 50, 53, 76, 81, 111, 118, 125, 128	Not Connected
TXCLK_GND	GND		1	Ground (0 V)
TXCLK_VCC	+3.3 V		4	Power Supply
GND	GND		17, 28, 110	Ground (0 V)
RSCLK_VCC	+3.3 V		15	Power Supply
RSCLK_GND	GND		19	Ground (0 V)
RSD_VCC	+3.3 V		24	Power Supply
RSD_GND	GND		21	Ground (0 V)
RXCORE_VCC	+3.3 V		26, 48	Power Supply
RXCORE_GND	GND		27, 49	Ground (0 V)

Table 5. S3457 Common Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
POUT_VCC	+3.3 V		29, 37, 43	Power Supply
POUT_GND	GND		38, 46	Ground (0 V)
PCLK_VCC	+3.3 V		54	Power Supply
PCLK_GND	GND		59	Ground (0 V)
PIN_VCC	+3.3 V		65, 75	Power Supply
PIN_GND	GND		60, 70	Ground (0 V)
BYPCLK_VCC	+3.3 V		88	Power Supply
BYPCLK_GND	GND		85	Ground (0 V)
TSCLK_VCC	+3.3 V		113, 116	Power Supply
TSCLK_GND	GND		112, 117	Ground (0 V)
TSD_VCC	+3.3 V		120, 123	Power Supply
TSD_GND	GND		119, 124	Ground (0 V)

Figure 5. S3457 128 TQFP Pinout

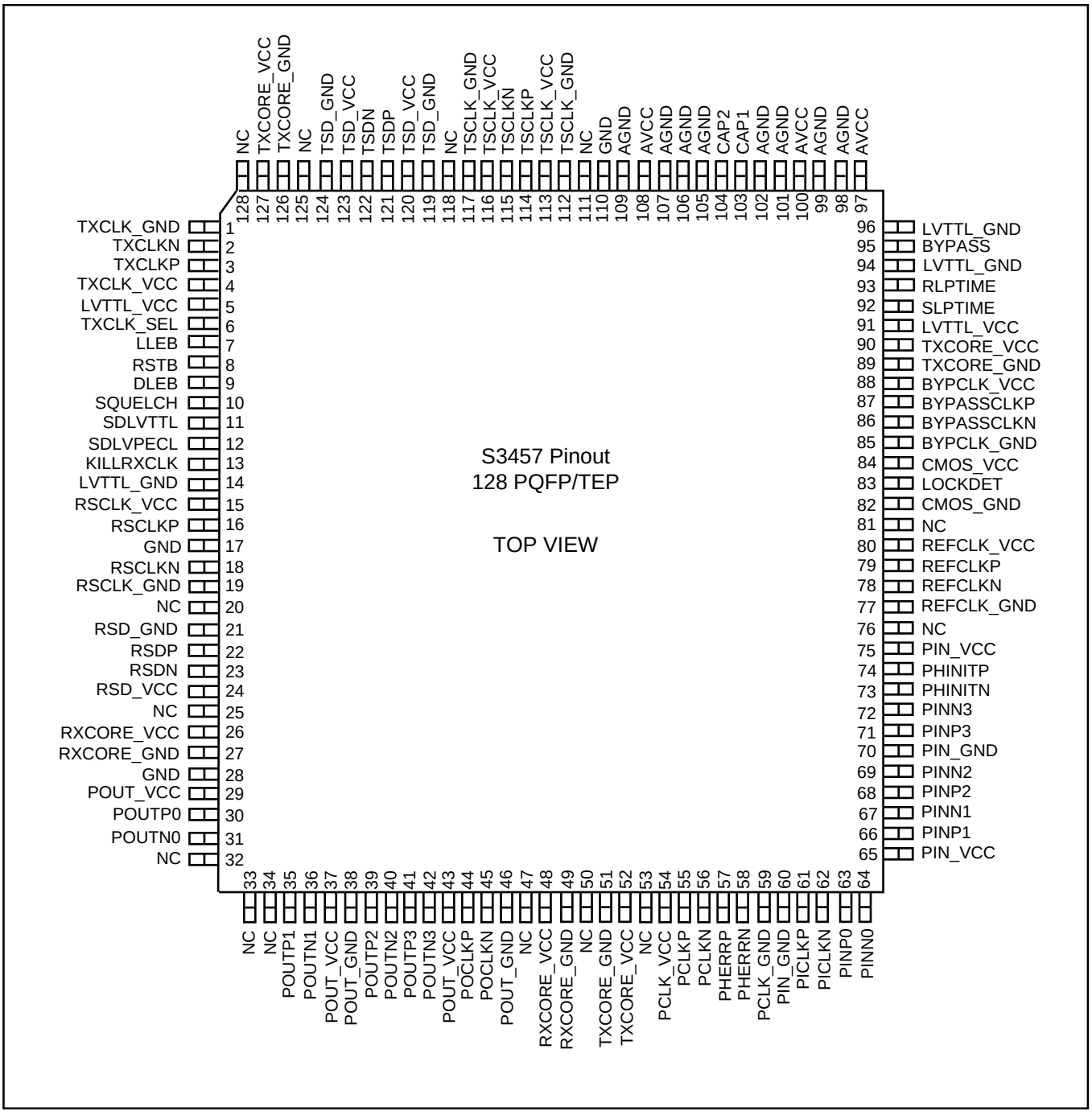
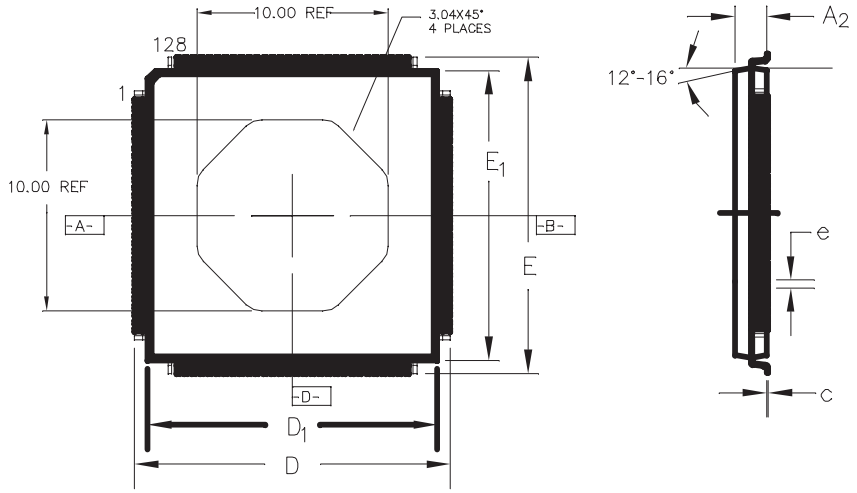
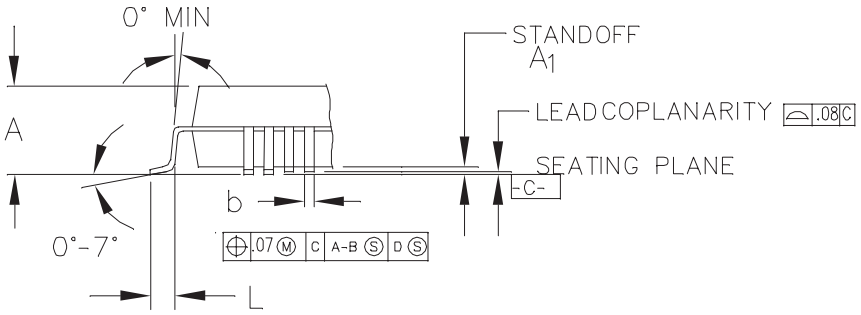


Figure 6. Compact 128 TQFP Package Drawing

DW0098-62 128 TQFP/TEP (14 x 14 x 1.4 mm)-Thin Quad Flat Pack



TOP VIEW SIDE VIEW



DIMENSIONS (are in millimeters)

UNIT	A	A_1	A_2	D	D_1	E	E_1	L	e	b	c
MIN		0.05	1.35	16.00 BSC.	14.00 BSC.	16.00 BSC.	14.00 BSC.	0.45	0.40 BSC.	0.13	
NOM			1.40					0.60		0.18	
MAX	1.60	0.15	1.45					0.75		0.23	0.17

Table 6. Thermal Management

Device	Max Package Power	Θja (Still Air)
S3457	1.9 W	23.5 ° C/W

Table 7. Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency Clock Synthesyzing Unit (CSU)		2.488		GHz	
Output Jitter STS-48			0.007	UI (rms)	Note: Output jitter measured at SONET operating rate using appropriate filter. rms jitter, in lock.
Reference Clock Frequency Tolerance	-100		+100	ppm	± 20 is required to meet SONET output frequency specification.
Reference Clock Input Duty Cycle	45		55	%	
Reference Clock Rise and Fall Times			1.5	ns	10% to 90% of amplitude.

Table 8. Absolute Maximum Ratings

Parameter	Min	Typ	Max	Units
Storage Temperature	-65		150	˚C
Voltage on V_{CC} with respect to GND	-0.5		+3.6	V
Voltage on any LVPECL/LVDS Input Pin	0		V_{CC}	V
High Speed LVPECL Output Source Current			24	mA

Electrostatic Discharge (ESD) Ratings

The S3457 is rated to the following voltages based on the human body model:

1. All pins are rated 100 Volts except pin # 77(REFCLK_GND), 80(REFCLK_VCC), 103(CAP1), and 104(CAP2).

Adherence to standards for ESD protection should be taken during the handling of the devices to ensure that the devices are not damaged. The standards to be used are defined in ANSI standard ANSI/ESD S20.20-1999, "Protection of Electrical and Electronic Parts, Assemblies and Equipment." Contact your local FAE or sales representative for applicable ESD application notes.

Table 9. Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Ambient Temperature Under Bias	-20		85	˚C
Voltage on V_{CC} with respect to GND	3.135	3.3	3.465	V
Voltage on any LVPECL/LVDS Input Pin	V_{CC} -2		V_{CC}	V
Voltage on any LVTTL Input Pin	0		V_{CC}	V
ICC[1]		450	548	mA

1. Outputs terminated.

Table 10. LVTTL Input/Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IH}	Input High Voltage	2.0		LVTTL V_{CC}	V	LVTTL V_{CC} = Max
V_{IL}	Input Low Voltage	0.0		0.8	V	LVTTL V_{CC} = Max
I_{IH}	Input High Current			50	µA	V_{IN} = 2.4 V
I_{IL}	Input Low Current	-500			µA	V_{IN} = 0.5 V
V_{OH}	Output High Voltage	2.4			V	V_{CC} = Min I_{OH} = -100 µA
V_{OL}	Output Low Voltage			0.5	V	V_{CC} = Min I_{oL} = 1 mA

Table 11. Internally Biased Differential LVPECL Input DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	LVPECL Input Low Voltage	V_{CC} - 2		V_{CC} - 1.4	V	
V_{IH}	LVPECL Input High Voltage	V_{CC} -1.25		V_{CC} - 0.55	V	
$\Delta V_{INSINGLE}$	Single Ended Input Voltage Swing	200		1200	mV	See Figure 11.
ΔV_{INDIFF}	Differential Input Voltage Swing	400		2400	mV	See Figure 11.
V_{BIAS}	Input DC Bias	V_{CC} - 0.65	V_{CC} - 0.5	V_{CC} - 0.35	V	
I_{IL}	Input Low Current	-220		-50	µA	V_{IL} = V_{CC} - 2
I_{IH}	Input High Current	-20		50	µA	V_{IH} = V_{CC} - 0.5

Table 12. Differential LVPECL Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
$\Delta V_{OUTSINGLE}$	Single Ended Output Voltage Swing	500		950	mV	See Figure 11.
$\Delta V_{OUTDIFF}$	Differential Output Voltage Swing	1000		1900	mV	See Figure 11.
V_{OH}	Output High Voltage	V_{CC} -1.2		V_{CC} -0.65	V	
V_{OL}	Output Low Voltage	V_{CC} -1.95		V_{CC} -1.50	V	

Table 13. Single-Ended LVPECL Input DC Characteristics[1]

Parameter	Description	Min	Typ	Max	Units	Conditions
V_{IL}	PECL Input Low Voltage	V_{CC} -2.0		V_{CC} -1.5	V	Guaranteed at -20˚ C.
V_{IL}	PECL Input Low Voltage	V_{CC} -2.0		V_{CC} -1.441	V	Guaranteed at 85˚ C.
V_{IH}	PECL Input High Voltage	V_{CC} -1.2		V_{CC} -0.75	V	Guaranteed at -20˚ C.
V_{IH}	PECL Input High Voltage	V_{CC} -1.023		V_{CC} -0.55	V	Guaranteed at 85˚ C.
I_{IL}	Input Low Current	-100		0	µA	$V_{IL} = V_{CC}$ - 2
I_{IH}	Input High Current	+50		350	µA	$V_{IH} = V_{CC}$ - 0.5

1. The AMCC LVPECL inputs (V_{IL} and V_{IH}) are non-temperature compensated I/O which vary at 1.3 mV/˚C.

Table 14. LVDS Input DC Characteristics

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{IH}	Input High Voltage	1.2		2.9	V	Over process, voltage and temperature range.
V_{IL}	Input Low Voltage	0.6		2.8	V	Over process, voltage and temperature range. See Figure 11.
V_{INDIFF}	Input Voltage Differential	200		2600	mV	Over process, voltage and temperature range. See Figure 11.
$V_{INSINGLE}$	Input Single Ended Voltage	100		1300	mV	Over process, voltage and temperature range.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	Over process, voltage and temperature range.
I_{IL}	Input Low Current	-300		0	µA	$V_{IL} = V_{CC}$ -2
I_{IH}	Input High Current	-50		100	µA	$V_{IH} = V_{CC}$ -0.5

Table 15. LVDS Output DC Characteristics[1]

Parameter	Description	Min	Typ	Max	Unit	Conditions
V_{OH}	Output High Voltage	1.25		1.8	V	Over process, voltage and temperature range.
V_{OL}	Output Low Voltage	0.85		1.4	V	Over process, voltage and temperature range.
$V_{OUTDIFF}$	Output Differential Voltage	440	740	1100	mV	Over process, voltage and temperature range. See Figure 11.
$V_{OUTSINGLE}$	Output Single Ended Voltage	220	370	550	mV	Over process, voltage and temperature range. See Figure 11.

1. Output loading is 100 Ω line-to-line.

Table 16. Differential CML Output DC Characteristics

Parameter	Description	Min	Typ	Max	Units	Condition
V_{OL} (Data)	CML Output Low Voltage	V_{CC} -1.0		V_{CC} -0.65	V	100 Ω line-to-line.
V_{OH} (Data)	CML Output HighVoltage	V_{CC} -0.35		V_{CC} -0.2	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Data)	CML Serial Output Differential Voltage Swing	800		1600	mV	100 Ω line-to-line. See Figure 11.
$\Delta V_{OUTSINGLE}$ (Data)	CML Serial Output Single Ended Voltage Swing	400		800	mV	100 Ω line-to-line at 2.488 Gbps. See Figure 11.
V_{OL} (Clock)	CML Output Low Voltage	V_{CC} -1.5		V_{CC} -0.85	V	100 Ω line-to-line.
V_{OH} (Clock)	CML Output High Voltage	V_{CC} -0.5		V_{CC} -0.25	V	100 Ω line-to-line.
$\Delta V_{OUTDIFF}$ (Clock)	CML Serial Output Differential Voltage Swing	800		1800	mV	100 Ω line-to-line. See Figure 11.
$\Delta V_{OUTSINGLE}$ (Clock)	CML Serial Output Single Ended Voltage Swing	400		900	mV	100 Ω line-to-line at 2.488 GHz. See Figure 11.

Table 17. Differential CML Input DC Characteristics

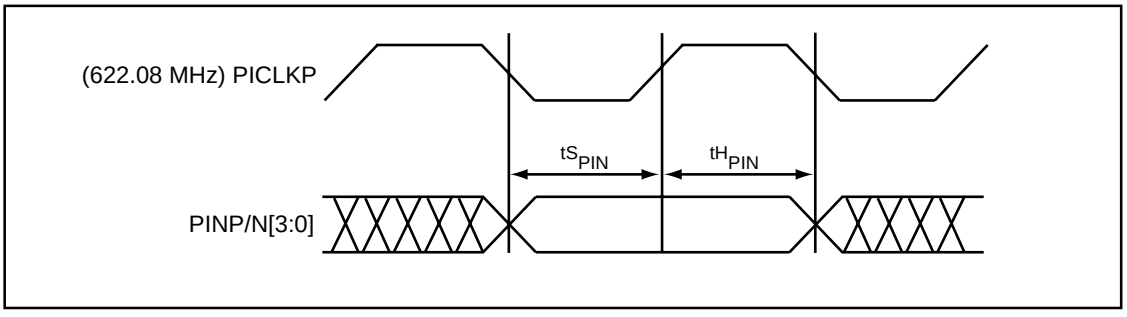
Parameter	Description	Min	Typ	Max	Units	Comments
V_{IL}	CML Input Low	V_{CC} -1.7		V_{CC} -0.6	V	
V_{IH}	CML Input High	V_{CC} -0.55		V_{CC} -0.15	V	
ΔV_{INDIFF}	Differential Input Voltage Swing	300		2400	mV	See Figure 11.
$\Delta V_{INSINGLE}$	Single Ended Input Voltage Swing	150		1200	mV	See Figure 11.
R_{DIFF}	Differential Input Resistance	80	100	120	Ω	

Table 18. AC Transmitter Low Speed Timing Characteristics (PICLKP/N = 622.08 MHz)

Parameter	Description	Min	Typ	Max	Units
	PICLKP/N Duty Cycle (See Figure 7)	40		60	%
tS_{PIN}	PINP/N[3:0] Set-up Time w.r.t. rising edge of PICLKP (See Figure 7)	200			ps
tH_{PIN}	PINP/N[3:0] Hold Time w.r.t. rising edge of PICLKP (See Figure 7)	200			ps
	PCLKP/N Duty Cycle	45		55	%
	LVDS Output Rise and Fall Time (20% - 80%)			300[1]	ps
	TXCLKP/N Duty Cycle	45		55	%
	PCLK to PICLK drift after FIFO is centered			2	ns

1. Assume 2 pF load.

Figure 7. AC Transmitter Input Timing



1. When a setup time is specified on LVDS signals between an input and a clock, the set-up time is the time in picoseconds from the crossover of the input to the crossover point of the clock.
2. When a hold time is specified on LVDS signals between an input and a clock, the hold time is the time in picoseconds from the crossover point of the clock to the crossover of the input.

Table 19. AC Transmitter High Speed Timing Characteristics

Parameter	Description	Min	Typ	Max	Units
	TSCLK Frequency			2.488	GHz
	TSCLK Duty Cycle	45		55	%
	TSCLK Duty Cycle Distortion w.r.t. RSCLK or BYPASSCLK (In SLPTIME, LLEB or BYPASS modes)			5.0	%
tS_{TSD}	TSD Setup Time w.r.t. TSCLKP Rising (See Figure 8)	145			ps
tH_{TSD}	TSD Hold Time w.r.t. TSCLKP Rising (See Figure 8)	100			ps
	CML Output Rise and Fall Time (20% - 80%)			150	ps

Figure 8. AC Transmitter Output Timing

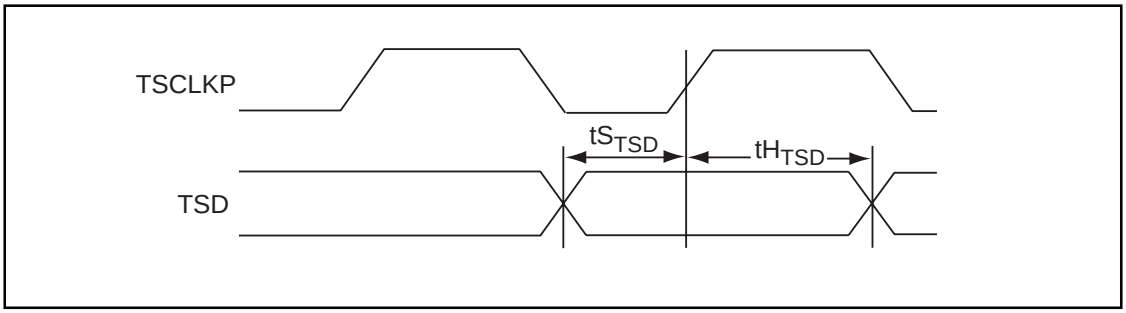


Table 20. AC Receiver Characteristics

Parameter	Parameter	Min	Typ	Max	Units	Test Conditions
	POCLKP/N / TX_CLKP/N Duty Cycle	45		55	%	100 Ω line-to-line.
	POCLKP/N Rise Time	100		300	ps	20%-80%, 100 Ω line-to-line.
	POUTP/N Rise Time	100		300		
	POCLKP/N Fall Time	100		300	ps	20%-80%, 100 Ω line-to-line.
	POUTP/N Fall Time	100		300		
t_{PD}	POUTP/N Delay from POCLKP/N	600		1000	ps	See Figure 9.
t_{SU}	POUTP/N[3:0] Set-Up Time w.r.t. POCLK	600			ps	See Figure 9.
t_H	POUTP/N[3:0] Hold Time w.r.t. POCLK	600			ps	See Figure 9.
tS_{RSD}	RSDP/N Setup Time w.r.t. RSCLKP	75			ps	See Figure 10.
tH_{RSD}	RSDP/N Hold Time w.r.t. RSCLKP	75			ps	See Figure 10.
	RSCLK Duty Cycle	40		60	%	
	RSCLK Frequency			2.488	GHz	

Figure 9. Parallel Data Output Delay from POCLK

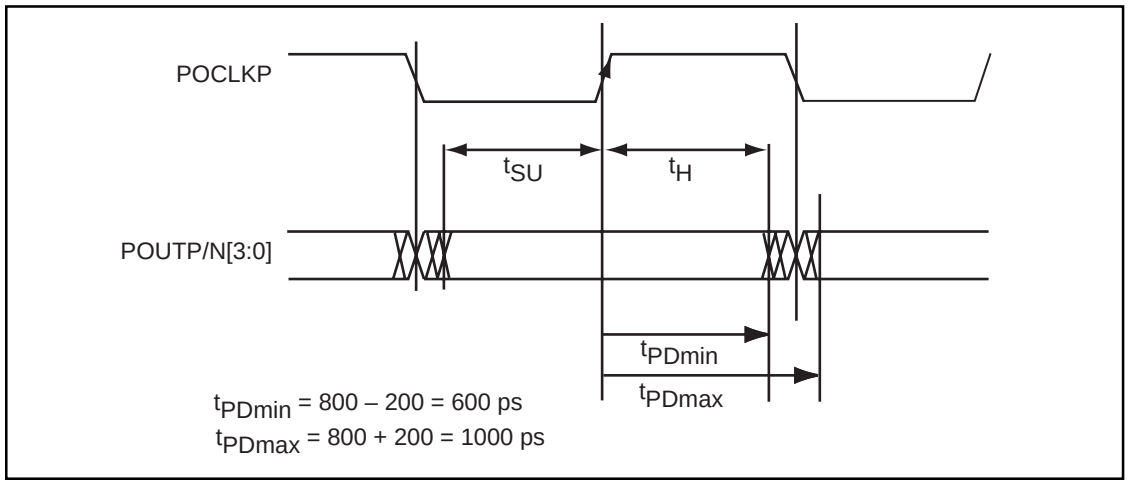


Figure 10. Receiver Input Timing Diagram

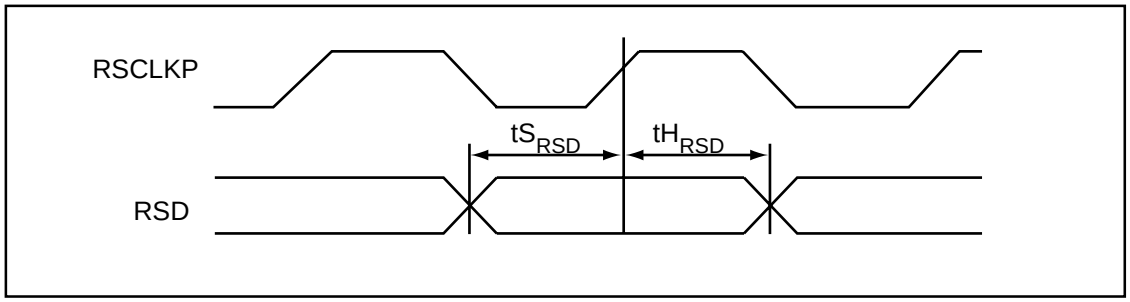


Figure 11. Differential Voltage Measurement

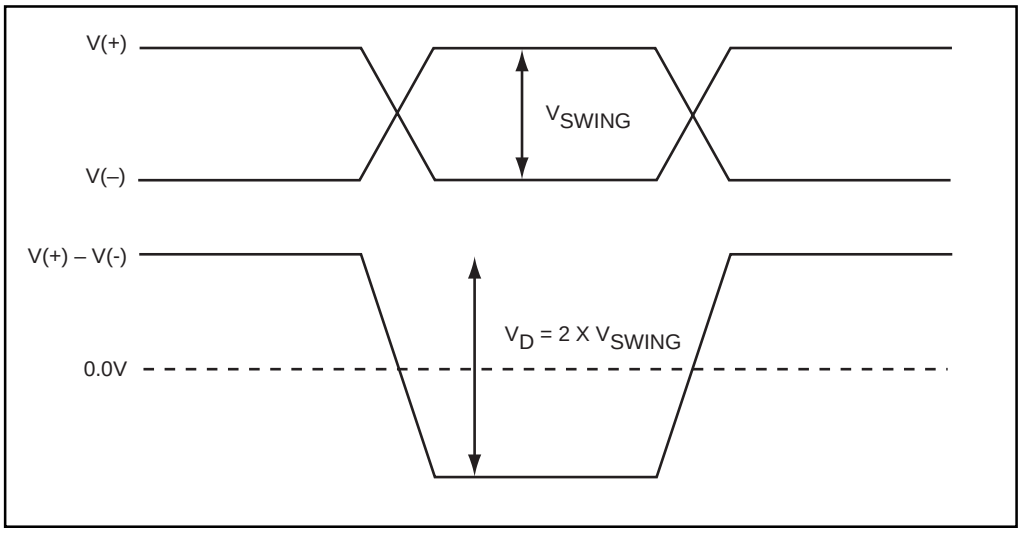
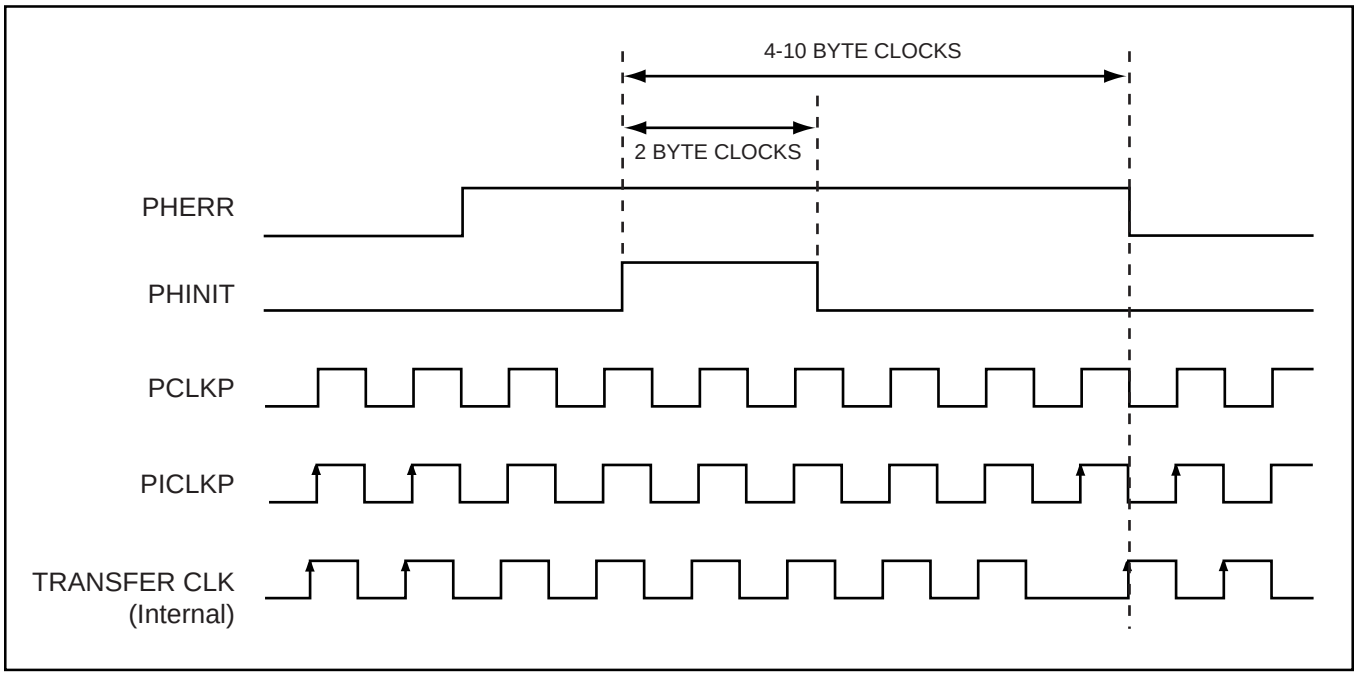


Figure 12. Phase Adjust Timing



Note: The byte clock = 622.08 MHz.

Figure 13. Differential CML Output to +5V PECL Input AC Coupled Termination

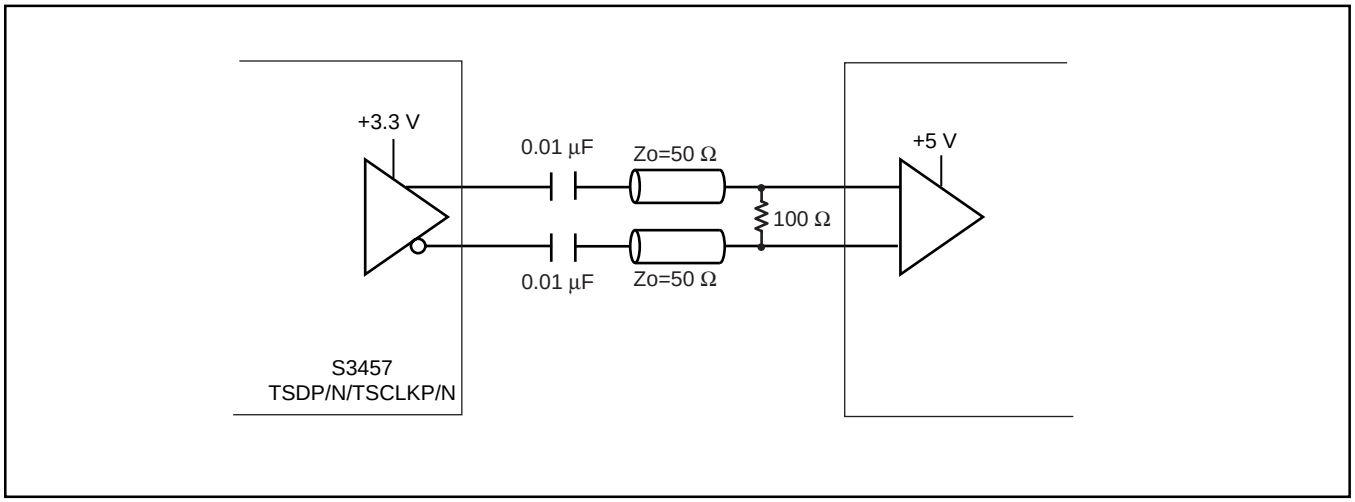


Figure 14. Differential CML Output to +3.3V LVPECL Input DC Coupled Termination

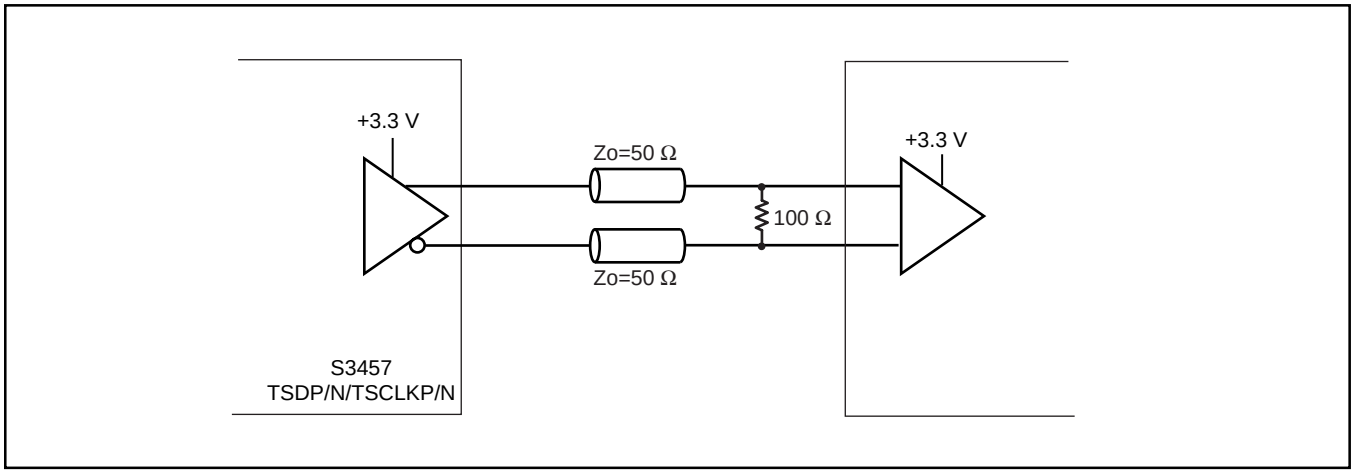


Figure 15. Differential LVPECL Driver to Differential LVPECL Input Termination

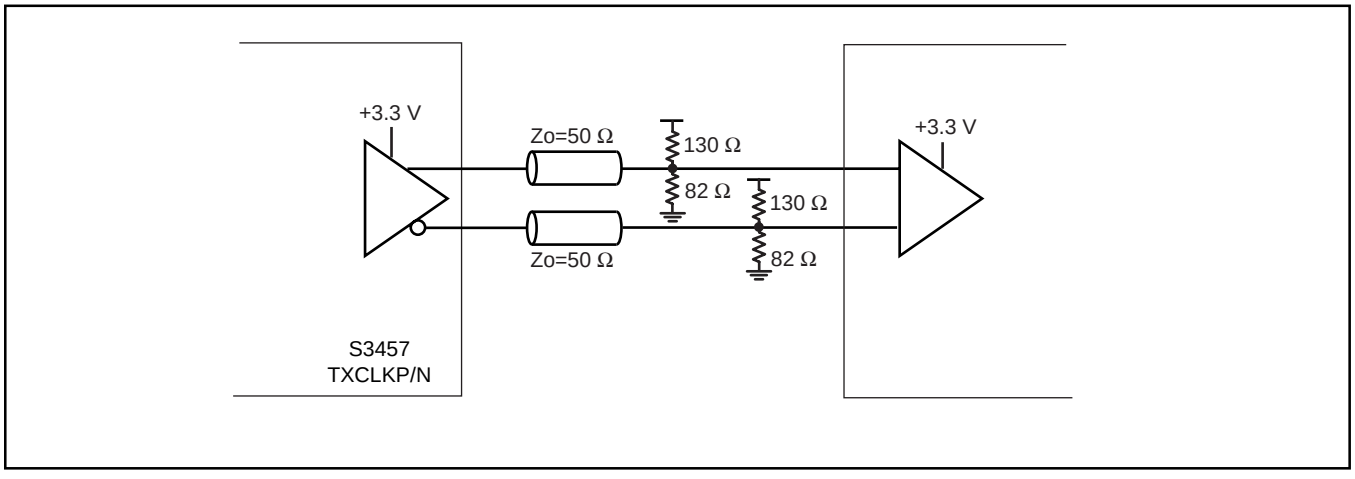


Figure 16. +5V Differential PECL Driver to S3457 Differential CML Input AC Coupled Termination

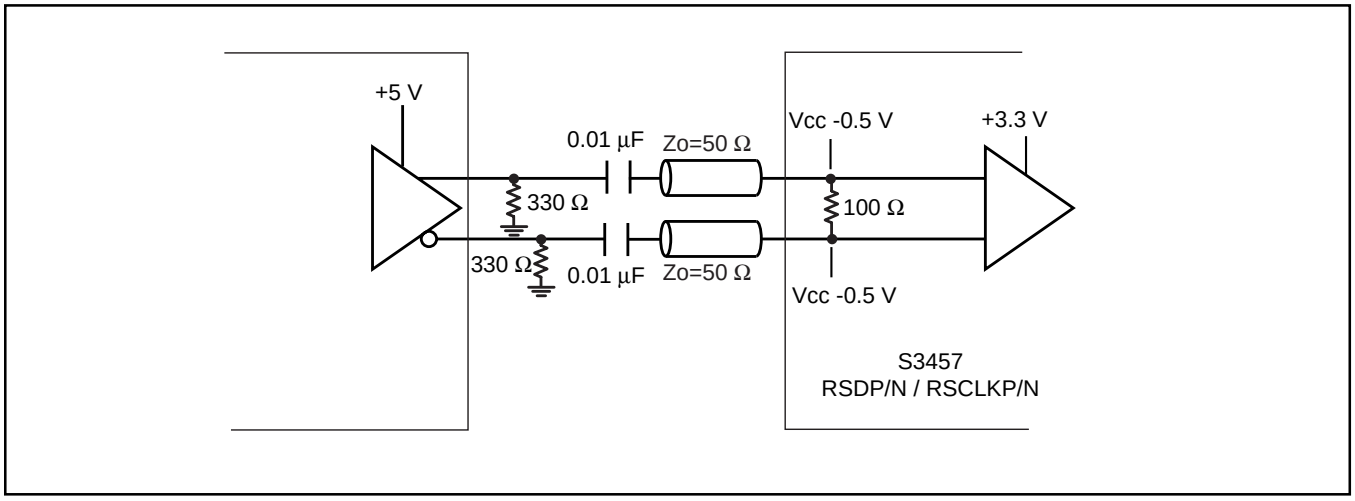


Figure 17. +3.3V Differential CML Driver to S3457 Differential CML Input Direct Coupled Termination

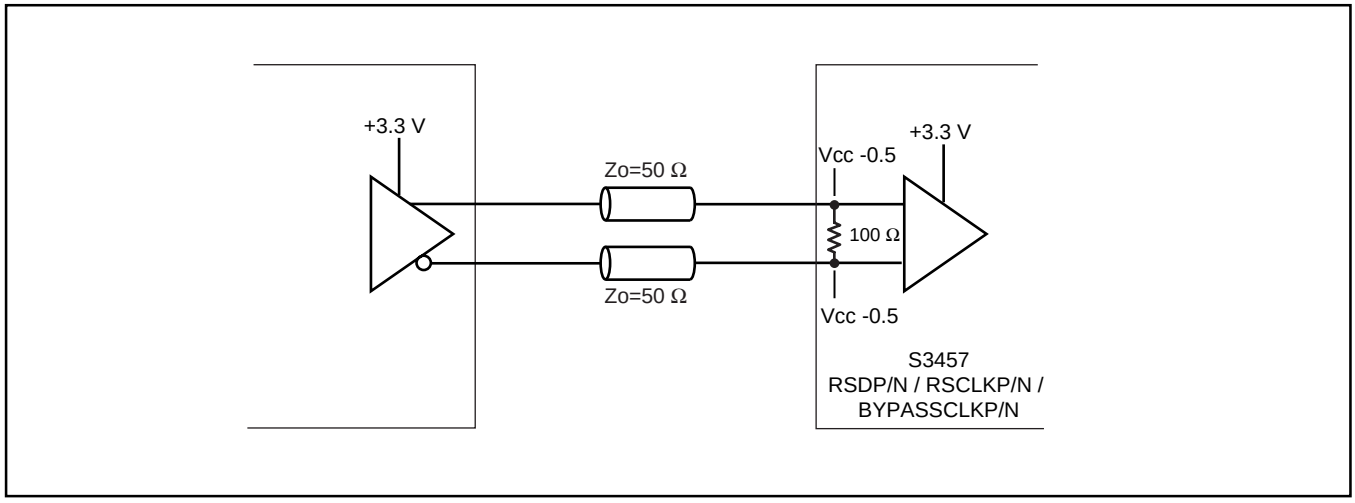


Figure 18. +5V Differential PECL Driver to S3457 Internally Biased Differential LVPECL Input AC Coupled Termination

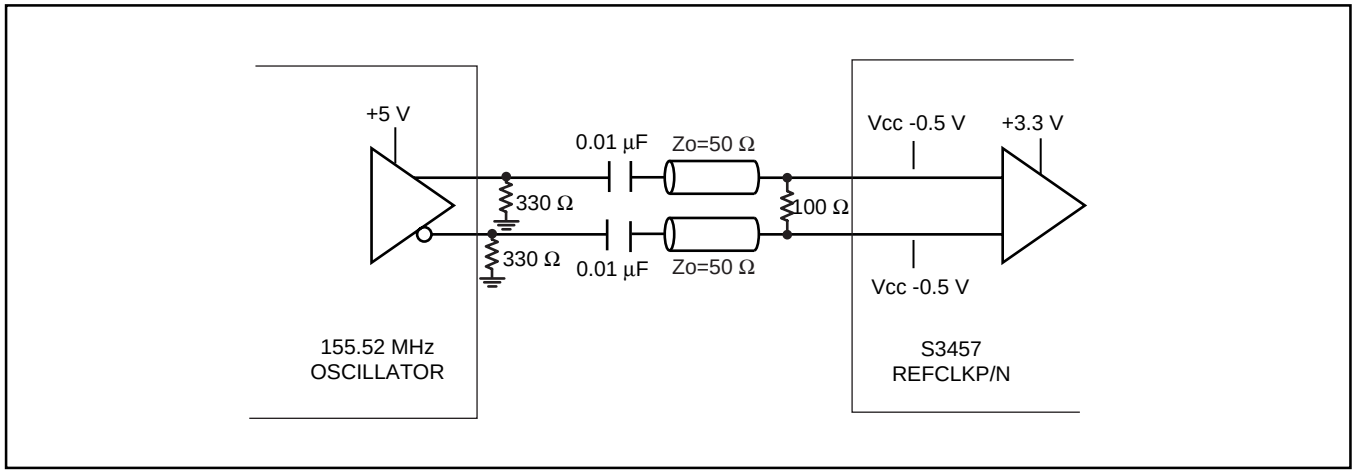


Figure 19. +3V Differential LVPECL Driver to S3457 Internally Biased Differential LVPECL Input DC Coupled Termination

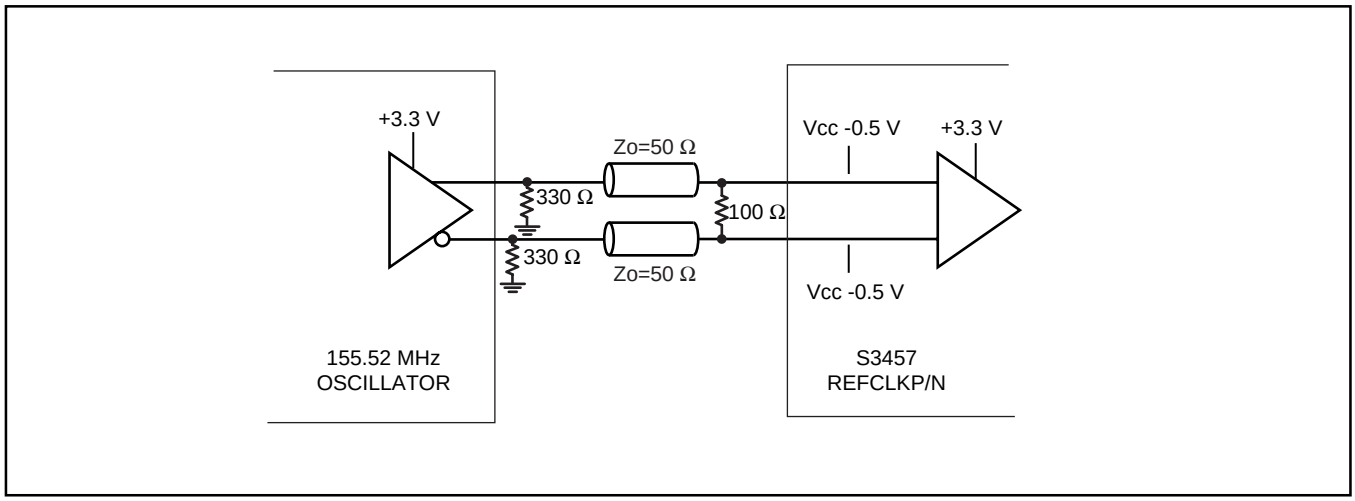


Figure 20. S3457 LVDS Driver to LVDS Input

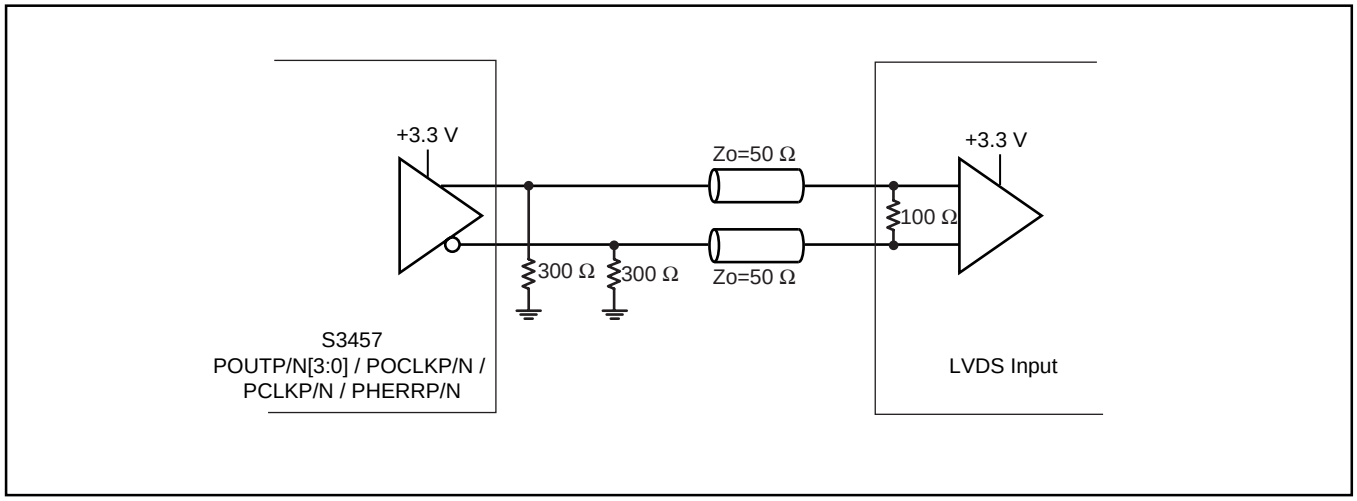


Figure 21. LVDS Driver to S3457 LVDS Inputs

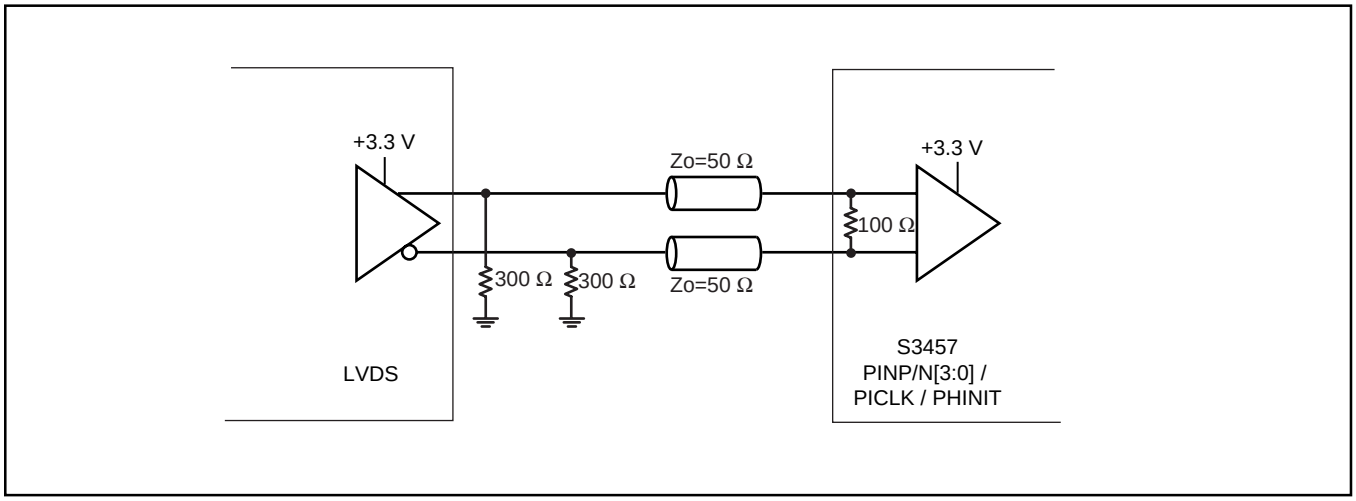
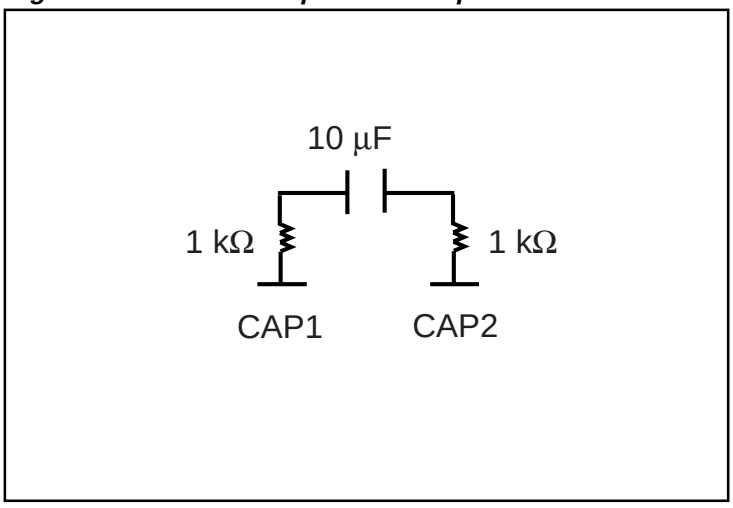


Figure 22. External Loop Filter Components



Ordering Information

PREFIX	DEVICE	PACKAGE
S – Integrated Circuit	3457	TT – 128 TQFP

X Prefix XXXX Part No. XX Package

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