DEVICE
SPECIFICATION

FIBRE CHANNEL AND GIGABIT ETHERNET TRANSCEIVER S2054

FEATURES

- Functionally compliant with ANSI X3T11 Fibre Channel physical and transmission protocol standards and IEEE 802.3z Gigabit Ethernet Applications
- Transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed differential LVPECL or LVTTL reference
- Receiver PLL configured for clock and data recovery
- 1250 and 1062 Mb/s operation
- 10-bit parallel LVTTL compatible interface
- 1.1mW typical power dissipation
- +3.3V power supply
- Low-jitter serial LVPECL compatible interface
- Lock detect
- Dual serial inputs and outputs
- Local loopback
- Compact 10mm x 10mm 64 PQFP package
- Fibre Channel framing performed by receiver
- Continuous downstream clocking from receiver
- Low jitter LVPECL reference clock input option

APPLICATIONS

High-speed data communications

- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes
- RAID drives
- Mass storage devices

GENERAL DESCRIPTION

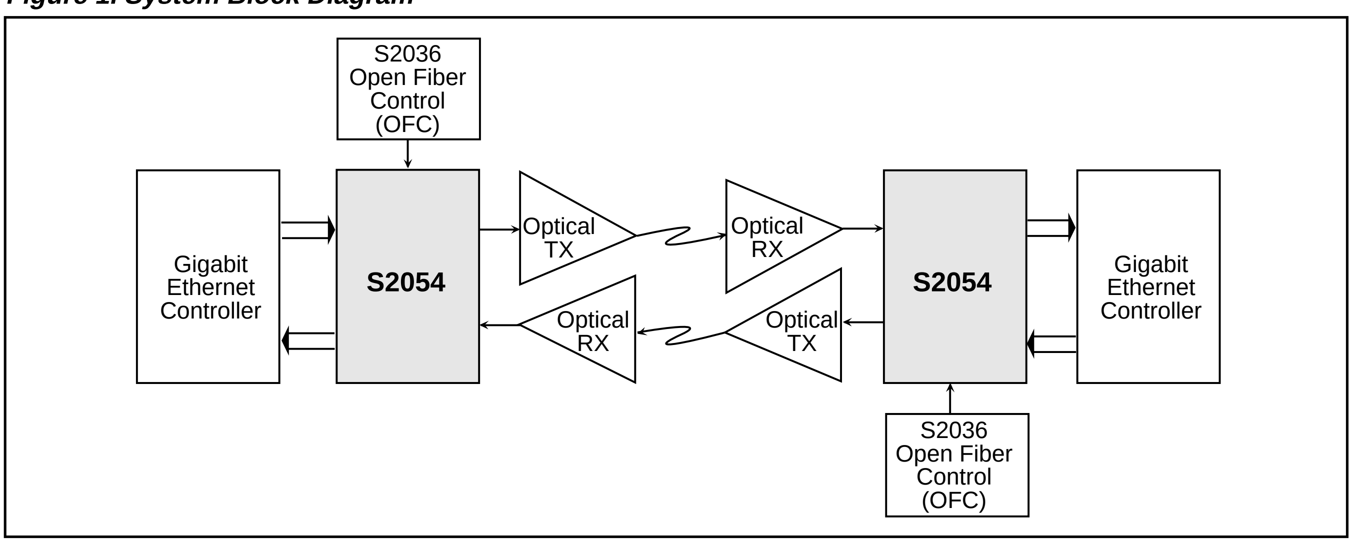
The S2054 transmitter and receiver chip is designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T11 Fibre Channel specification and IEEE 802.3z Gigabit Ethernet. The chip runs at 1250.0, and 1062.5 Mbit/s data rates with associated 10-bit data word.

The S2054 is similar to the S2052. The S2054 provides dual transmit and receive serial I/O in addition to an optional LVTTL or differential LVPECL reference clock input and high drive LVTTL outputs. The dual transmit and receive serial I/O are useful for backbone applications in which redundant optical or electrical links are required. The differential LVPECL reference clock provides the lowest transmitter output jitter solution. The high drive LVTTL outputs allow longer trace lengths or connectors to be used between the S2054 and the Media Access Controller.

The chip performs parallel-to-serial and serial-to-parallel conversion and framing for block-encoded data. The transmitter's on-chip PLL synthesizes the high-speed clock from a low-speed reference. The receiver's on-chip PLL synchronizes directly to incoming digital signal to receive the data stream. The transmitter and receiver each support differential LVPECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local line loopback mode is provided for system diagnostics. Dual serial inputs and dual serial outputs facilitate redundant design and provide maximum flexibility.

Figure 1 shows a typical configuration incorporating the chip, which is compatible with AMCC's S2036 Open Fiber Control (OFC) device (for 1062 operation only).

Figure 1. System Block Diagram



S2054 OVERVIEW

The S2054 transmitter and receiver provide serialization and deserialization functions for block-encoded data to implement a Fibre Channel interface. Operation of the S2054 is straightforward, as depicted in Figure 2. The sequence of operations is as follows:

Transmitter
1. 10-bit parallel input
2. Parallel-to-serial conversion
3. Serial output

Receiver
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10-bit parallel output

The 10-bit parallel data handled by the S2054 device should be from a DC-balanced encoding scheme, such as the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into 10-bit transmission characters[1], and be compliant with ANSI X3.230 FC-PH (Fibre Channel Physical and Signaling Interface).

Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 4. A block diagram showing the basic chip operation is shown in Figure 3.

Loopback

Local loopback is supported by the chip, and provides a capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics.

Figure 2. Interface Diagram

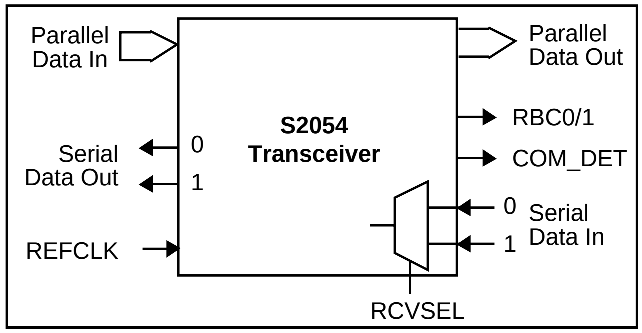
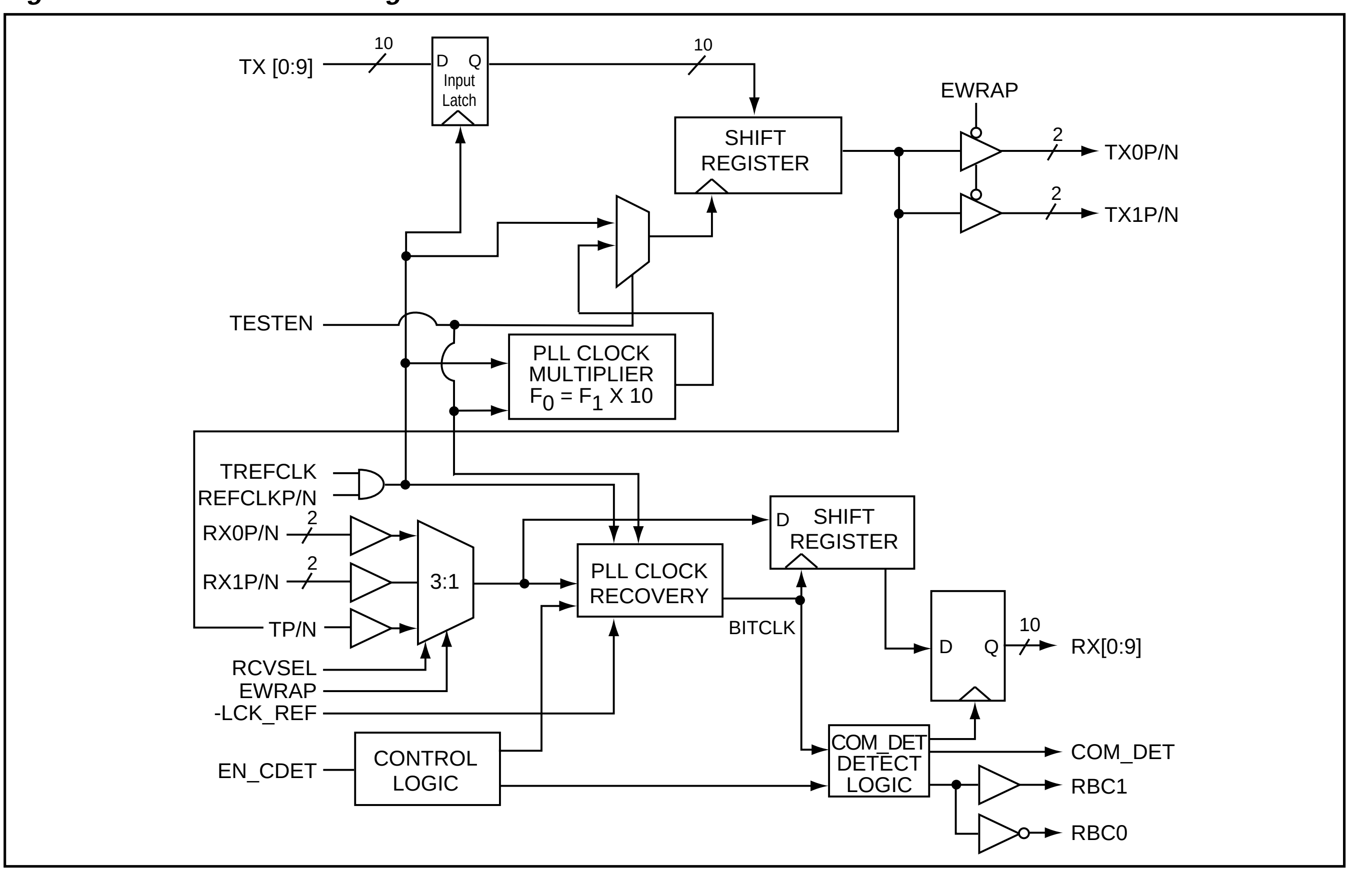


Figure 3. Functional Block Diagram



1. A.X. Widmer and P.A. Franaszek, “A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code,” IBM Research Report RC 9391, May 1982.

TRANSMITTER FUNCTIONAL DESCRIPTION

The S2054 transmitter accepts parallel input data and serializes it for transmission over fiber optic or coaxial cable media. The chip is fully compatible with the ANSI X3T11 Fibre Channel standard, and supports the Fibre Channel and Gigabit Ethernet data rates of 1250 and 1062 Mbit/sec. (See Figure 3.)

Data Input

Transmit data is provided to the S2054 as 10-bit wide LVTTL. Data is clocked into the S2054 on the rising edge of REFCLK.

Parallel/Serial Conversion

The parallel-to-serial converter takes in 10-bit wide data from the input latch and converts it to a serial data stream. Parallel data is latched into the transmitter using the reference clock. The data is then clocked synchronous to the clock synthesis unit serial clock into the serial output shift register. The shift register is clocked by the internally generated bit clock which is 10x the reference clock input frequency. D0 is transmitted first as described in annex N and Tables 22 and 23 of FC-PH. Table 1 shows the mapping of the parallel data to the 8B/10B codes. Two serial data outputs are provided.

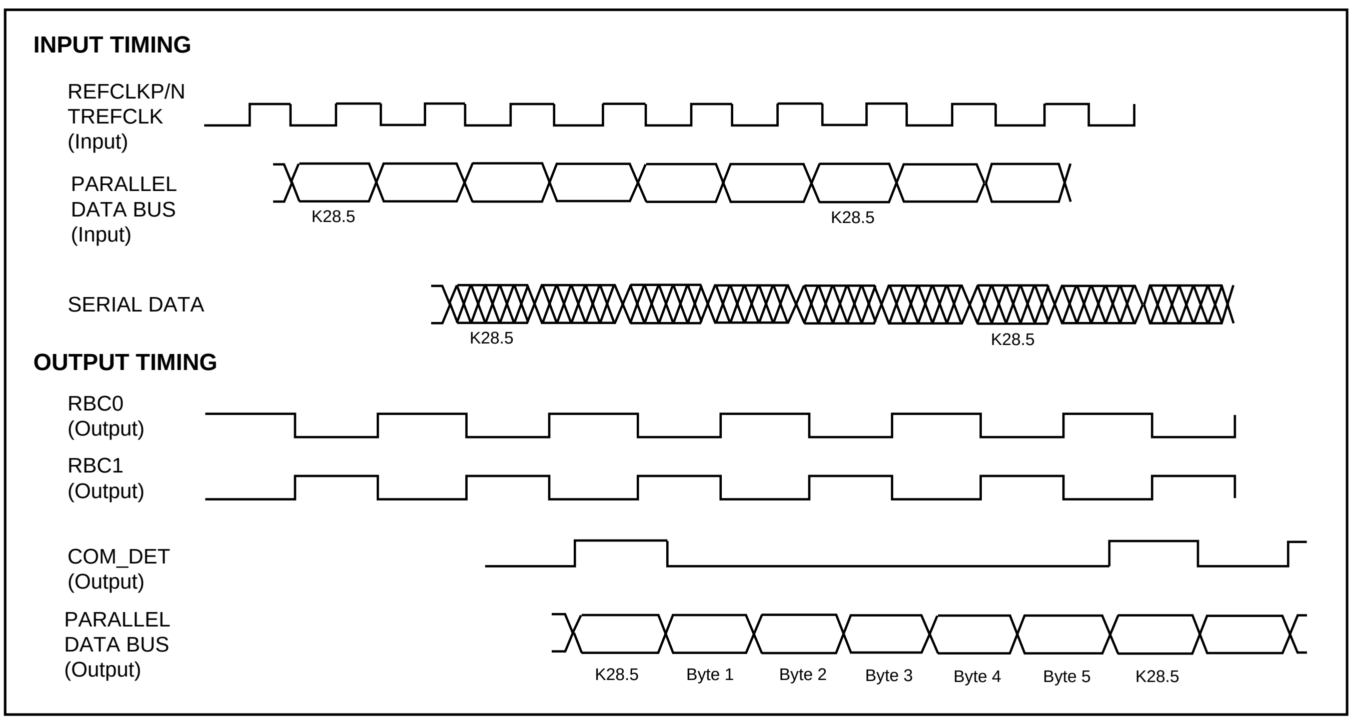
Reference Clock Input

The reference clock input must be supplied with either a differential LVPECL (REFCLKP/N) or single-ended LVTTL (TREFCLK) clock source with 100 PPM tolerance to assure that the transmitted data meets the Fibre Channel frequency limits. The internal serial clock is frequency locked to the reference clock (125.00 or 106.25 MHz).

Table 1. Data Mapping to 8b/10b Alphabetic Representation

	Data Byte									
TX[0:9] or RX[0:9]	0	1	2	3	4	5	6	7	8	9
8b/10b alphabetic representation	a	b	c	d	e	i	f	g	h	j

Figure 4. Functional Waveform (1250 and 1062.5 Mbit/sec)



RECEIVER FUNCTIONAL DESCRIPTION

The S2054 receiver is designed to implement the ANSI X3T11 Fibre Channel specification and the IEEE 802.3z Gigabit Ethernet receiver functions. A block diagram showing the basic chip function is provided in Figure 3.

Two serial inputs are provided by the S2054. The RCVSEL pin is used to select the active input. Whenever a signal is present on the selected pin, the S2054 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. Received data from the incoming bit stream is provided on the device's parallel data outputs.

The S2054 accepts serial encoded data from a fiber optic or coaxial cable interface. The serial input stream is the result of the serialization of 8B/10B encoded data by an FC compatible transmitter. Clock recovery is performed on-chip, with the output data presented to the Fibre Channel transmission layer as 10-bit parallel data.

Serial/Parallel Conversion

Serial data is received on the RX[0:1]P/N pins. The PLL clock recovery circuit will lock to the data stream if the clock to be recovered is within ±100 PPM of the internally generated bit rate clock. The recovered clock is used to retime the input data stream. The data is then clocked into the serial to parallel output registers on the edge of RBC1. Data is clocked out on the rising edge of RBC1 and RBC0. The parallel data out is 10 bits wide. The word clock (RBC1) is synchronized to the incoming data stream word boundary by the detection of the Fibre Channel comma character (0011111XXX, positive running disparity).

Framing

The S2054 provides COM_DET character recognition and data word alignment of the LVTTL compatible output data bus. In systems where the COM_DET function is undesired, a LOW on the EN_CDET input disables the COM_DET function and the data will be "un-framed".

When framing is disabled by low EN_CDET, the S2054 simply achieves bit synchronization within 250 bit times and begins to deliver parallel output data words whenever it has received full transmission words. No attempt is made to synchronize on any particular incoming character.

The COM_DET output signal will go high whenever a K28.5 character (positive disparity) is present on the parallel data outputs and EN_CDET is High. If EN_CDET is Low, comma characters will not be reported. The COM_DET output signal will be low at all other times.

Lock Detect

The S2054 lock detect function monitors the state of the receiver phase-locked loop (PLL) clock recovery unit. The PLL will lock within 250 bit times after the start of receiving serial data inputs. If the serial data inputs have an instantaneous phase jump (from a serial switch, for example) the PLL will not indicate an out-of-lock state, but will recover the correct phase alignment within 50 to 250 bit times, depending on the input eye opening. (See Fig. 13). If a run length of 80-160 bits is exceeded, or if the input data rate varies by more than approximately 600 ppm compared to the reference clock, the loop will be declared out of lock. When lock is lost, the PLL will shift from the serial input data to the reference clock, so that the downstream clock will maintain the correct frequency.

In any transfer of PLL control from the serial data to the reference clock, the RBC1/RBC0 output remains phase continuous and glitch free, assuring the integrity of downstream clocking.

Lock to Reference

The S2054 can be forced to lock to the REFCLK by holding the –LCK_REF signal Low. For normal operation, –LCK_REF must be held High.

OTHER OPERATING MODES

Loopback

When local loopback is enabled, serial data from the transmitter is internally routed to the receiver, where the clock is extracted and the data is deserialized. The parallel data is then sent to the subsystem for verification. The high speed serial outputs are disabled during loopback. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium. It also allows system diagnostics.

Operating Frequency Range

The S2054 is optimized for operation at 1250 and 1062 Mbit/s. Operation at other rates is possible if the rate falls between the nominal rates. REFCLK must be selected to be within 100 ppm of the desired byte or word clock rate.

Table 2. S2054 Transmitter Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
TX9 TX8 TX7 TX6 TX5 TX4 TX3 TX2 TX1 TX0	LVTTL	I	11 10 9 8 7 6 5 4 3 2	Transmit data. Parallel data on this bus is clocked in on the rising edge of REFCLK (TTL or PECL). TX0 is transmitted first.
REFCLKP REFCLKN	LVPECL	I	22 23	Differential LVPECL. Reference clock and transmit byte clock. A crystal-controlled reference clock for the PLL clock multiplier. The frequency of REFCLKP/N is the bit rate divided by 10. When TTL REFCLK (TREFCLK) is used, tie REFCLKP to VCC. Let REFCLKN float. (Internally biased for AC coupling.)
TREFCLK	LVTTL	I	26	TTL reference clock and transmit byte clock, a crystal-controlled reference clock for the PLL multiplier. The frequency of the TREFCLK is the bit rate divided by 10. When PECL REFCLK is used, let TREFCLK float or hold High (internal pull-up).
TX0P TX0N	Diff. LVPECL	O	60 59	Differential LVPECL outputs that send out the serial transmitter data and drive 75Ω or 50Ω termination to Vcc–2V. TX0P is the positive output, and TX0N is the negative output.
TX1P TX1N	Diff. LVPECL	O	63 62	Differential LVPECL outputs that send out the serial transmitter data and drive 75Ω or 50Ω termination to Vcc–2V. TX1P is the positive output, and TX1N is the negative output.

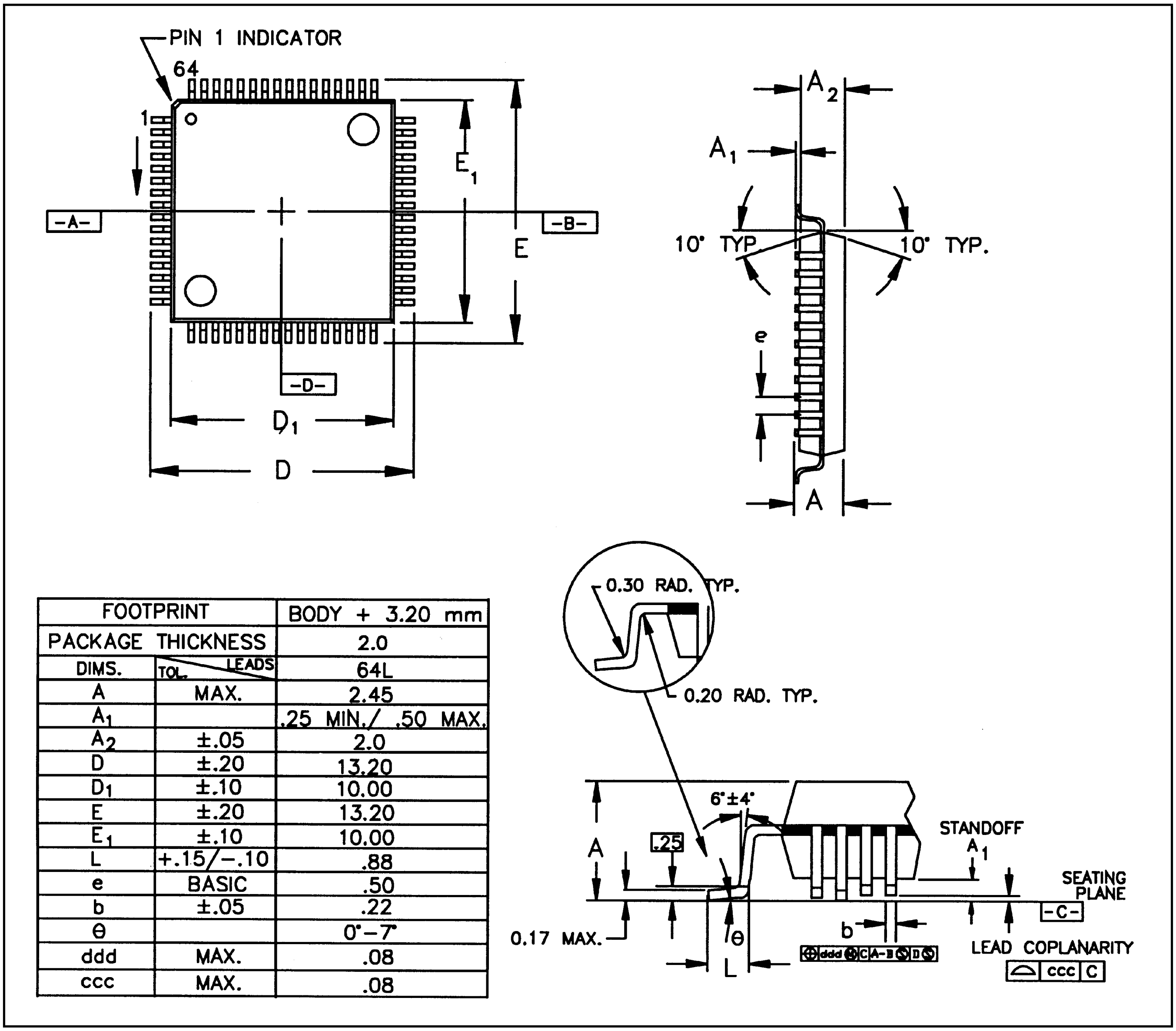
Table 3. S2054 Receiver Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
RX9 RX8 RX7 RX6 RX5 RX4 RX3 RX2 RX1 RX0	LVTTL	O	34 35 36 38 39 40 41 43 44 45	Receive data outputs. Parallel data on this bus is valid on the rising edge of RBC0 and RBC1. RX0 is the first bit received.
RBC1 RBC0	Diff. LVTTL	O	30 31	Receive clock. Parallel data is valid on the rising edge of RBC0 and RBC1 (see timing diagram in Figure 8). After a sync word is detected, the period of the current RBC1 and RBC0 is stretched to align with the word boundary.
EN_CDET	LVTTL	I	24	Enable comma detect. When High, enables sync detection. Detection of the 7-bit comma + character sync pattern, RX(0-9) = (K28.5:0011111XXX), will enable the word boundary for the data to follow. When Low, data is treated as unframed data.
RX0P RX0N	Diff. LVPECL	I	53 52	Primary Differential LVPECL received serial data inputs. RXP is the positive input, and RXN is the negative input. (Internally biased for AC coupling.)
RX1P RX1N	Diff. LVPECL	I	56 55	Secondary Differential LVPECL received serial data inputs. RXP is the positive input, and RXN is the negative input. (Internally biased for AC coupling.)
–LCK_REF	Static	I	27	Multi-level Static Lock to reference input. When Low, the RX PLL will lock to the REFCLK input. When High, the RX PLL will lock to the incoming data.
COM_DET	LVTTL	O	47	Comma detect. Upon detection of a valid sync symbol, this output goes high for one RBC1 period. When sync is active, the sync character shall be present on the parallel data bus bits RX0–RX9.
RCVSEL	LVTTL	I	13	Receiver input select. When Low, RX0P-RX0N is selected as the serial receiver input. When High, RX1P-RX1N is selected.
EWRAP	Static	I	19	Wrap input. When High, selects the transmitter serial output data to be routed to the receiver. When Low, the serial data is selected by the RCVSEL input. TXP, TXN are static when EWRAP is High.

Table 4. S2054 Common Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
ECLVCC	+3.3V	–	28, 20	Core Power Supply (+3.3V).
TTLGND	GND	–	33, 32, 46	TTL Ground.
TTLVCC	3.3V	–	29, 37, 42	TTL Power Supply (3.3V).
ECLIOVCC	3.3V	–	54, 58, 61, 64	PECL I/O Power Supply (3.3V).
ECLIOVEE	GND	–	1, 57	PECL I/O Ground.
AVCC	3.3V	–	18, 50	Analog Power Supply (3.3V).
AVEE	GND	–	15, 51	Analog Ground.
ECLVEE	GND	–	21, 25	Core Ground.
GND	GND	–	14	These pins require connection to Ground.
NC	–	–	12	No Connection. This pin has no electrical connection.
TESTEN	LVTTL	I	16	When LOW, REFCLK replaces internal TX and RX bit clock to facilitate factory testing. When High the TX PLL will lock to the REFCLK input and the RX PLL will lock to receive data.
RESET	LVTTL	I	17	When LOW, the S2054 is held in reset. This pin should be held High for normal operation.
TEST20	LVTTL	I	48	Factory Test Mode. This pin should be held High for normal operation.

Figure 5. 64 PQFP Package



FOOTPRINT		BODY + 3.20 mm
PACKAGE THICKNESS		2.0
DIMS.	TOL. / LEADS	64L
A	MAX.	2.45
A_1		.25 MIN./ .50 MAX.
A_2	±.05	2.0
D	±.20	13.20
D_1	±.10	10.00
E	±.20	13.20
E_1	±.10	10.00
L	+.15/−.10	.88
e	BASIC	.50
b	±.05	.22
θ		0°−7°
ddd	MAX.	.08
ccc	MAX.	.08

Thermal Management

Device	Θja (Still Air)
S2054	45 °C/W

Figure 6. S2054 Pin Assignment

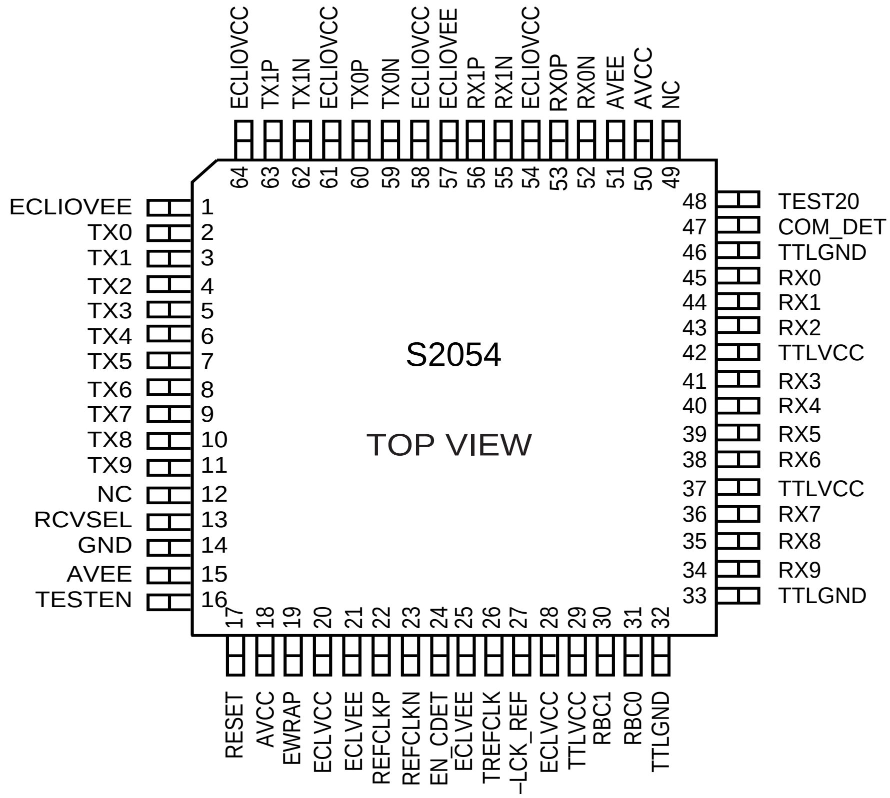


Table 5. Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	-55		125	°C
Junction Temperature under Bias	-55		150	°C
Storage Temperature	-65		150	°C
Voltage on VCC with Repect to GND	-0.5		+7.0	V
Voltage on any LVTTL Input Pin except Tx [0:9]	-0.5		3.47	V
Voltage on LVTTL input pin TX [0:9]			+5.5	V
Voltage on any PECL Input Pin	0		VCC	V
LVTTL Output Sink Current			8	mA
LVTTL Output Source Current			8	mA
High Speed LVPECL Output Source Current			50	mA
Static Discharge Voltage	500			V

Table 6. Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	0		70	°C
Junction Temperature under Bias			130	°C
Voltage on TTLVCC, ECLVCC, ECLIOVCC, and AVCC with respect to GND/VEE	3.13	3.3	3.47	V
Voltage on LVTTL Input Pin except TX [0:9]	0		3.47	V
Voltage on any LVPECL Input Pin	VCC -1.0V		VCC	V
Voltage on LVTTL data TX [0:9]	0		5.0	

Table 7. Reference Clock Requirements

Parameters	Description	Min	Max	Units	Conditions
FT	Frequency Tolerance	-100	+100	ppm	—
TD_{1-2}	Symmetry	40	60	%	Duty Cycle at 50% pt.
T_{RCR}, T_{RCF}	REFCLK Rise and Fall Time	—	2	ns	20 – 80%
—	Random Jitter		18	ps	rms (In 12 KHz to 1 MHz Band)

Table 8. S2054 DC Characteristics

Parameters	Description	Min	Typ	Max	Units	Conditions
V_{OH}	Output HIGH Voltage (LVTTL)	2.2	2.5	VCC	V	V_{CC} = min, I_{OH} = -400 µA
V_{OL}	Output LOW Voltage (LVTTL)	GND	.025	0.5	V	V_{CC} = min, I_{OL} = 1 mA
V_{IH}	Input HIGH Voltage (LVTTL)	2.0	—	—	V	
V_{IL}	Input LOW Voltage (LVTTL)	GND	—	0.8	V	—
I_{IH}	Input HIGH Current (LVTTL)	—	—	40	µA	V_{IN} = 2.4V, V_{CC} = max
I_{IL}	Input LOW Current (LVTTL)	—	—	600	µA	V_{IN} = 0.4V, V_{CC} = max
I_{CC}	Supply Current		310	380	mA	Outputs open, V_{CC} = V_{CC} max
P_D	Power Dissipation		1.1	1.325	W	Outputs open, V_{CC} = V_{CC} max
V_{DIFF}	Min. differential input voltage swing for differential LVPECL inputs	100		1300	mV	
ΔV_{OUT}	Serial Output Voltage Swing	600	—	1600	mV	50Ω to V_{CC} -2.0V
C_{in}	Input capacitance	—		4	Pf	

Note: All LVTTL/CMOS AC measurements are assumed to have the output load of 10pF.

Table 9. S2054 Performance Summary

Parameter	S2054		Units
Operating Frequency *	1250	1062.5	Mbit/s
Serial clock period	.800	.941	ns
Byte clock period	8.00	9.41	ns
Acquisition Time	250	250	ns
Reference clock	125.0	106.25	MHz
Word width	10	10	Bits

* ±10% lock range, nominal frequency is per FC-PH standard.

Table 10. S2054 Transmitter Timing

Parameters	Description	Min	Max	Units	Conditions
T_1	Data setup w.r.t.↑REFCLKP/N	1.5	—	ns	See note.
T_2	Data hold w.r.t.↑REFCLKP/N	1.0	—	ns	
T_1	Data setup w.r.t. ↑ TREFCLK	1.5	—	ns	See note.
T_2	Data hold w.r.t.↑ TREFCLK	1.0	—	ns	
T_{SDR} , T_{SDF}	Serial data rise and fall	—	300	ps	20% to 80%, tested on a sample basis.
Transmitter Output Jitter Allocation					
T_JRMS	Serial data output random jitter (RMS)	—	20	ps	RMS, tested on a sample basis. Measured with K28.7 pattern at 1250 Mbps.
T_{DJ}	Serial data output deterministic jitter (p-p)	—	100	ps	Peak-to-peak, tested on a sample basis. Measured with K28.5 ± pattern at 1250 Mbps.

Note: All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Table 11. S2054 Receiver Timing

Parameters	Description	Min	Max	Units	Conditions
T_3	RBC0 to RBC1 skew	7.5	8.5	ns	Tested on a sample basis.
T_4	Data setup w.r.t. RBC0, RBC1	3.0		ns	1.0625 GHz Mode
T_5	Data hold w.r.t. RBC0, RBC1	1.5		ns	1.0625 GHz Mode
T_6	Data setup w.r.t. RBC0, RBC1	2.5		ns	1.250 GHz Mode
T_7	Data hold w.r.t. RBC0, RBC1	2.0		ns	1.250 GHz Mode
T_{RCR} , T_{RCF}	RBC0, RBC1 rise and fall time	—	3.0	ns	Measured from .8V to 2.0V.
T_{DR} , T_{DF}	Data Output rise and fall time	—	3.0	ns	Measured from .8V to 2.0V.
T_{SDR} , T_{SDF}	Serial data input rise and fall	—	300	ps	20% to 80%. (See Figure 10.)
T_{LOCK}	Data acquisition lock time @ <1.0625Gb/s	—	2.4	µs	8B/10B IDLE pattern sample basis
Duty Cycle	RBC0/RBC1 Duty Cycle	40%	60%		
Input Jitter Tolerance	Input data eye opening allocation at receiver input for BER ≤1E–12	30%	—	bit time	As specified in Fibre Channel FC–PH standard eye diagram jitter mask.

Note: Max. Load = 15 pF. All AC measurements are made from the reference voltage level of the clock (1.4V) to the valid input or output data levels (.8V or 2.0V).

Figure 7. Transmitter Timing Diagram

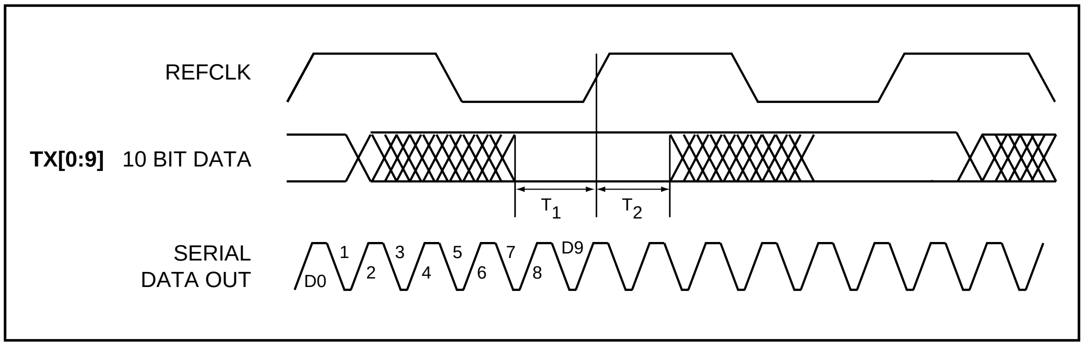


Figure 8. Receiver Timing Diagram (1062.5 Mbits/sec mode)

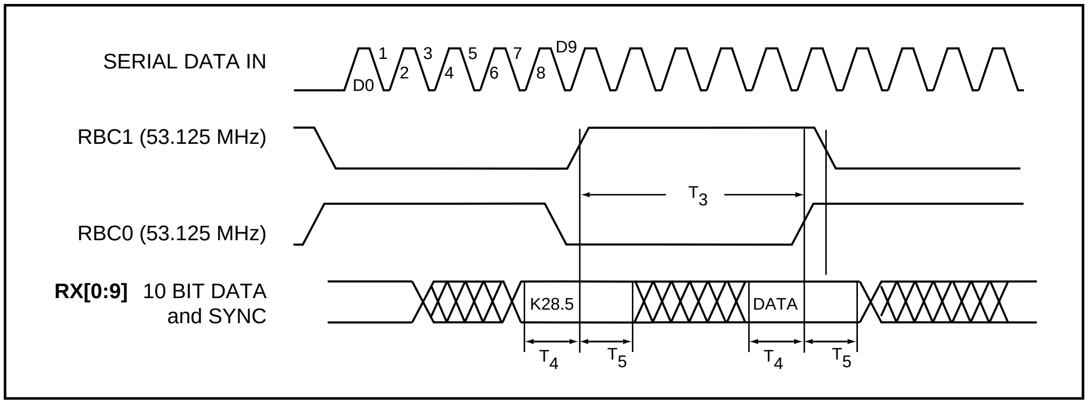


Figure 9. Receiver Timing Diagram (1250 Mbits/sec mode)

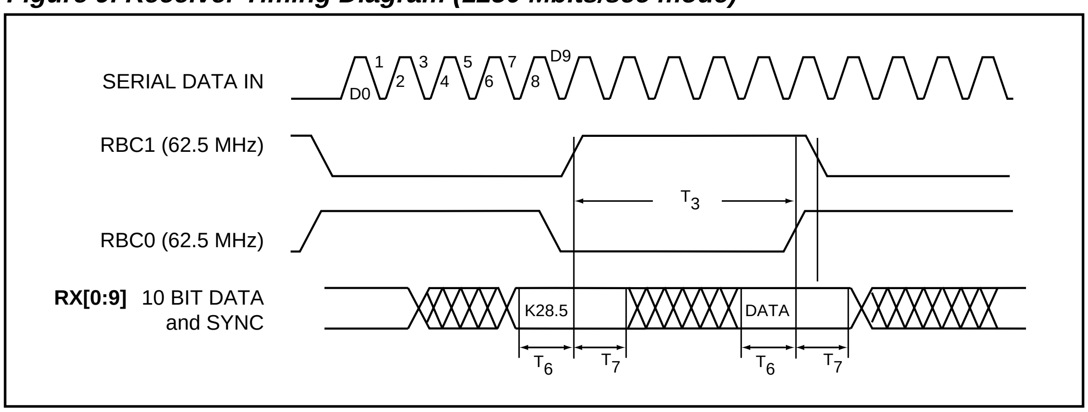


Figure 10. Serial Input Rise and Fall Time

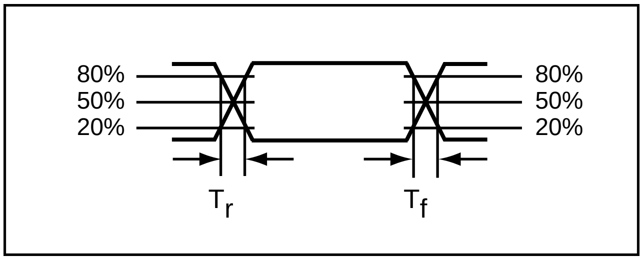


Figure 11. Serial Output Load

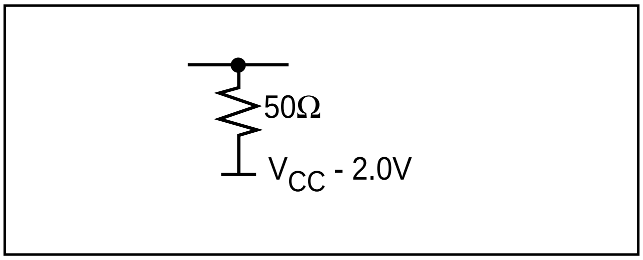


Figure 12. LVTTL Input and Output Rise and Fall Time

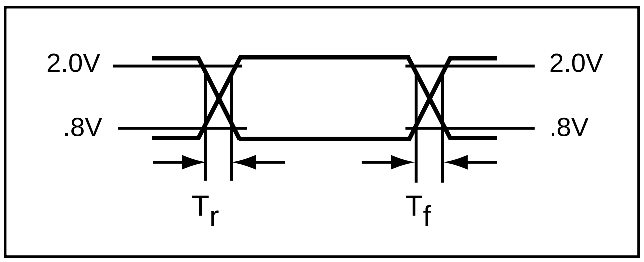
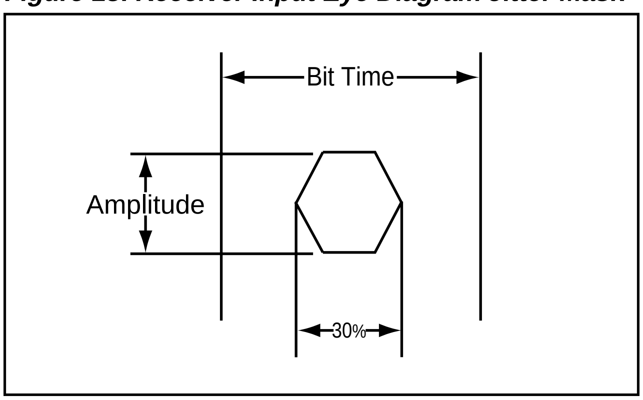


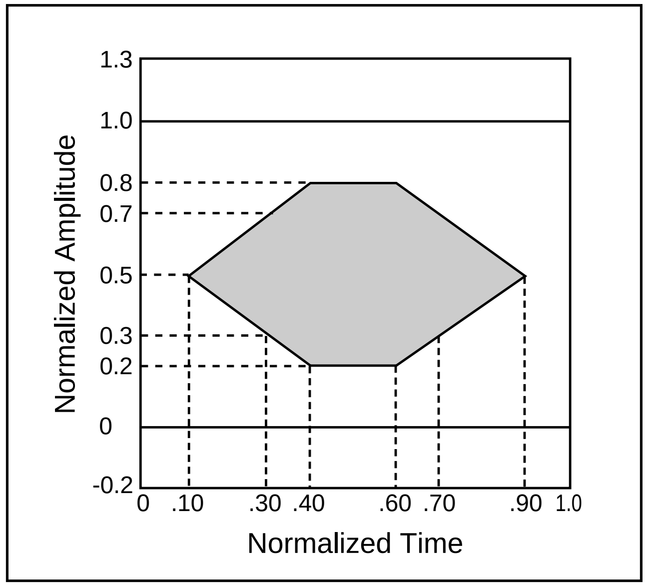
Figure 13. Receiver Input Eye Diagram Jitter Mask



ACQUISITION TIME

With the input eye diagram shown in Figure 14, the S2054 will recover data with a 10^{-9} BER within 50 bit times after an instantaneous phase shift of the incoming data.

Figure 14. Acquisition Time Eye Diagram



Ordering Information

GRADE	DEVICE	PACKAGE
S – commercial	2054	C – 64 PQFP (10mm)

X XXXX X

Grade Part number Package

ISO 9001 CERTIFIED

Applied Micro Circuits Corporation • 6290 Sequence Dr., San Diego, CA 92121
Phone: (619) 450-9333 • (800) 755-2622 • Fax: (619) 450-9885
http://www.amcc.com

D273/R484