SL763

1394a PCI Link Layer Core with DMA

Product Brief ***Innovative Semiconductors, Inc.***

FlexFire™
1394a Core Family

- **SL755: General purpose Link**
- **SL758: Link compatible with Texas Instrument's GPLynx™**
- **SL763: PCI Link Layer Core with DMA**
- **SL770: Audio/Video Link**
- **SL730: Mixed Signal PHY**
- **SL738: Backplane PHY**
- **iL700: 1394a Test Bench & Validation Suite**

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IEEE 1394

IEEE 1394 is a high-speed serial bus standard that allows video and audio consumer devices to communicate quickly, reliably, and inexpensively with a PC and with each other.

FlexFire™ Architecture

Innovative Semiconductors' ***FlexFire*** architecture is based on a set of parameterized building blocks that can be quickly and easily configured to support a wide range of 1394 applications.

The ***FlexFire*** 1394a core family includes general purpose and application-specific cores for both Link Layer and PHY Layer controllers.

FlexFire offers the fastest and most reliable way to incorporate 1394 capabilities into products such as digital cameras, audio/video devices, disk controllers, and other PC peripherals.

SL763 PCI Link Core with DMA

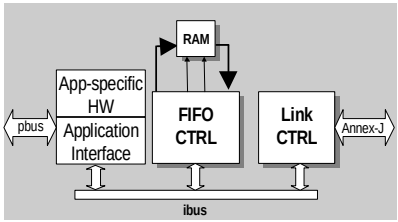
The SL763 provides the interface to connect devices to the high speed 1394 serial bus, at speeds up to 400 Mbits/sec. It offers easy adaptability to peripheral and consumer device applications, and has been proven in silicon.

The SL763 can be integrated with Innovative's SL730 1394a Mixed Signal PHY Layer core for a single-chip 1394a solution.

The SL763 is available in synthesizable RTL, and includes a comprehensive test bench and validation suite, synthesis scripts, and user documentation.

Features

- Compliant with IEEE 1394a Link Layer specification



- Verified in silicon
- Has a DMA unit with bus mastering capability. This DMA unit implements transactions layer functions
- The DMA unit support three Asynchronous channels and two isochronous channels
- The DMA unit implements a master plug for attachment to a local or a system bus adapter such as a PCI interface
- Supports segmented and contiguous buffers with minimal overhead
- Supports 100, 200, and 400 Mbits/sec transfer rates
- Operates at 50 MHz on commercial .5µ digital CMOS processes
- Works with Innovative's SL730 Mixed Signal PHY core, or with commercial PHY chips
- Cycle master capable
- 8, 16, or 32-bit application bus interfaces to common embedded processors
- Dynamically configurable FIFO functionality, number, and size
- RAM-based dual port FIFO can also be accessed at random
- Intelligent FIFO pointers implement *restore* and *discard* to simplify implementation of Retry
- Detects late packet and sequence errors
- Performs 32-bit CRC generation and checking