# **SL758**

## 1394a Link Layer Core Compatible with TI GPLynx™



**Product Brief** 

Innovative Semiconductors, Inc.

## FlexFire™ 1394a Core Family

- SL755: General purpose Link
- SL758: Link compatible with Texas Instrument's GPLynx™
- SL760: PCI to 1394a Link
- SL770: Audio/Video Link
- SL730: Mixed Signal PHY
- SL738: Backplane PHY
- iL700: 1394a Test Bench & Validation Suite



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#### **IEEE 1394**

IEEE 1394 is a high-speed serial bus standard that allows video and audio consumer devices to communicate quickly, reliably, and inexpensively with a PC and with each other.

#### FlexFire <sup>™</sup> Architecture

Innovative Semiconductors' *FlexFire* architecture is based on a set of parameterized building blocks that can be quickly and easily configured to support a wide range of 1394 applications.

The *FlexFire* 1394a core family includes general purpose and application-specific cores for both Link Layer and PHY Layer controllers.

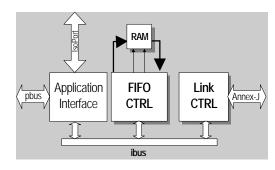
*FlexFire* offers the fastest and most reliable way to incorporate 1394 capabilities into products such as digital cameras, audio/video devices, disk controllers, and other PC peripherals.

#### SL758 GPLynx-Compatible Core

The silicon-proven SL758 provides the interface to connect devices to the high speed 1394 serial bus, at speeds up to 400 Mbits/sec.

The core is register and pin compatible with the Texas Instruments TSB12LV31 GPLynx chip, and includes support for the Isochronous Port Date Mover and Byte Stacker Microprocessor Interface. The SL758 interoperates with commercially-available PHY layer chips, and with Innovative's SL730 Mixed Signal PHY Layer core.

The SL758 is available in synthesizable RTL, and includes a comprehensive test bench and validation suite, synthesis scripts, and user documentation.



#### **Features**

- Compliant with IEEE 1394a Link Layer specification
- Verified in silicon
- Register and pin compatible with Texas Instruments GPLynx chip
- Provides a superset of Texas Instruments' IsoPort functionality including support for \$400
- Processor interface can be configured to 8 or 16 bits wide, and can operate at up to 50 MHz
- FIFO can be configured for up to 256 quadlets
- Interoperable with Texas Instruments' TSB11LV01 and TSB21LV03 PHY Layer Controller chips
- Interoperable with Texas Instruments' software drivers
- Supports 100, 200, and 400 Mbits/sec transfer rates
- Operates at 50MHz on commercial .5μ digital CMOS processes
- Based on parameterized building blocks that can be configured for a wide range of Link Layer applications
- Performs 32-bit CRC generation and checking