SL755

1394a General Purpose Link Layer Core

Product Brief   *Innovative Semiconductors, Inc.*

FlexFire™
1394a Core Family

- SL755: General purpose Link

- SL758: Link compatible with Texas Instrument's GPLynx™

- SL760: PCI to 1394a Link

- SL770: Audio/Video Link

- SL730: Mixed Signal PHY

- SL738: Backplane PHY

- iL700: 1394a Test Bench & Validation Suite

IEEE 1394

IEEE 1394 is a high-speed serial bus standard that allows video and audio consumer devices to communicate quickly, reliably, and inexpensively with a PC and with each other.

FlexFire™ Architecture

Innovative Semiconductors' **FlexFire** architecture is based on a set of parameterized building blocks that can be quickly and easily configured to support a wide range of 1394 applications.

The **FlexFire** 1394a core family includes general purpose and application-specific cores for both Link Layer and PHY Layer controllers.

FlexFire offers the fastest and most reliable way to incorporate 1394 capabilities into products such as digital cameras, audio/video devices, disk controllers, and other PC peripherals.

SL755 General Purpose Link Core

The SL755 provides the interface to connect devices to the high speed 1394 serial bus, at speeds up to 400 Mbits/sec. It offers easy adaptability to peripheral and consumer device applications, and has been proven in silicon.

The core is a programmed I/O-style controller which is well-suited to peripheral applications.

The SL755 can be integrated with Innovative's SL730 1394a Mixed Signal PHY Layer core for a single-chip 1394a solution.

The SL755 is available in synthesizable RTL, and includes a comprehensive test bench and validation suite, synthesis scripts, and user documentation.
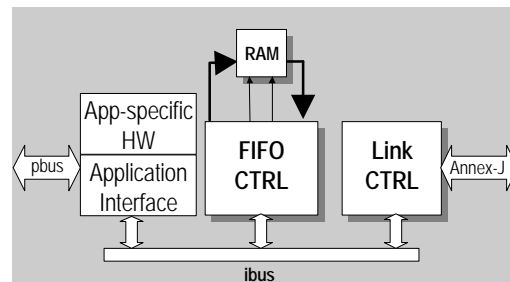
Features

- Compliant with IEEE 1394a Link Layer specification

- Verified in silicon

- Supports 100, 200, and 400 Mbits/sec transfer rates

- Operates at 50 MHz on commercial .5μ digital CMOS processes

- Works with Innovative's SL730 Mixed Signal PHY core, or with commercial PHY chips

- Provides full Link Layer support, plus some Transaction Layer and Bus Management functions

- Supports asynchronous and isochronous transfers, including multi-channel isochronous receive

- Cycle master capable

- 8, 16, or 32-bit application bus interfaces to common embedded processors

- Dynamically configurable FIFO functionality, number, and size

- RAM-based dual port FIFO can also be accessed at random

- Intelligent FIFO pointers implement *restore* and *discard* to simplify implementation of Retry

- Detects late packet and sequence errors

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