SL738

1394 Backplane PHY Core

Product Brief

Innovative Semiconductors, Inc.

FlexFire™
1394a Core Family

- SL755: General purpose Link
- SL758: Link compatible with Texas Instrument's GPLynx™
- SL760: PCI to 1394a Link
- SL770: Audio/Video Link
- SL730: Mixed Signal PHY
- SL738: Backplane PHY
- iL700: 1394a Test Bench & Validation Suite

Innovative Semiconductors, Inc.

465 Fairchild Drive
Suite 227
Mountain View, CA 94043
Tel 650-934-0170
Fax 650-934-0174
www.isi96.com

Japan
Kanematsu
Design Technology Corp
Ichikawa Bldg, 5-13-3 Ginza
Chuo-ku, Tokyo 104-0061
Tel 81-3-3543-7404
Fax 81-3-3543-7407

IEEE 1394

IEEE 1394 is a high-speed serial bus standard that allows video and audio consumer devices to communicate quickly, reliably, and inexpensively with a PC and with each other.

FlexFire™ Architecture

Innovative Semiconductors' ***FlexFire*** architecture is based on a set of parameterized building blocks that can be quickly and easily configured to support a wide range of 1394 applications.

The ***FlexFire*** 1394a core family includes general purpose and application-specific cores for both Link Layer and PHY Layer controllers.

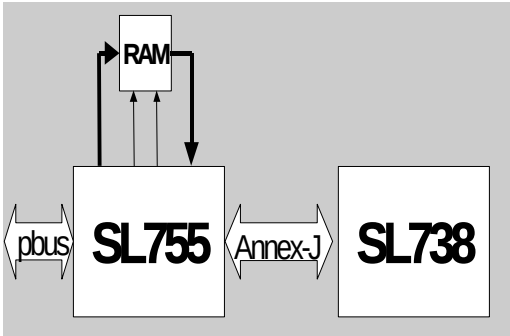
FlexFire offers the fastest and most reliable way to incorporate 1394 capabilities into products such as digital cameras, audio/video devices, disk controllers, and other PC peripherals.

SL738 Backplane PHY Core

The SL738 provides the transceiver functions to implement a single-port node in a backplane-based 1394 network, and supports transfer speeds of 50 or 100 Mbits/sec.

The SL738 is pin and register-compatible with Texas Instruments' TSB14C01 Backplane PHY chip, for use in IEEE 1394-1995-based systems. A single bit can be set to configure the SL738 for use in 1394a-based systems, in which the backplane PHY register set is defined.

The SL738 provides two terminals for transmitting, two for receiving, and a single terminal to control drivers for data and strobe. The core does not drive the backplane directly – this function must be provided externally.



Features

- Operates in both 1394-1995 and 1394a backplanes
- Implements 1394a Backplane PHY register set
- Single bit configures core for 1394-1995 operation or 1394a operation
- Supports 50 and 100 Mbits/sec transfer rates
- Performs clock recovery and synchronizes incoming data to local clock
- Performs system initialization and arbitration
- Separate transmitter and receiver
- Includes encode and decode functions for data strobe bit-level encoding
- Interoperates with Innovative's line of application-specific Link Layer cores, and with commercially-available Link Layer Controller chips
- Available in synthesizable RTL
- Includes a comprehensive test bench and validation suite, synthesis scripts, and user documentation