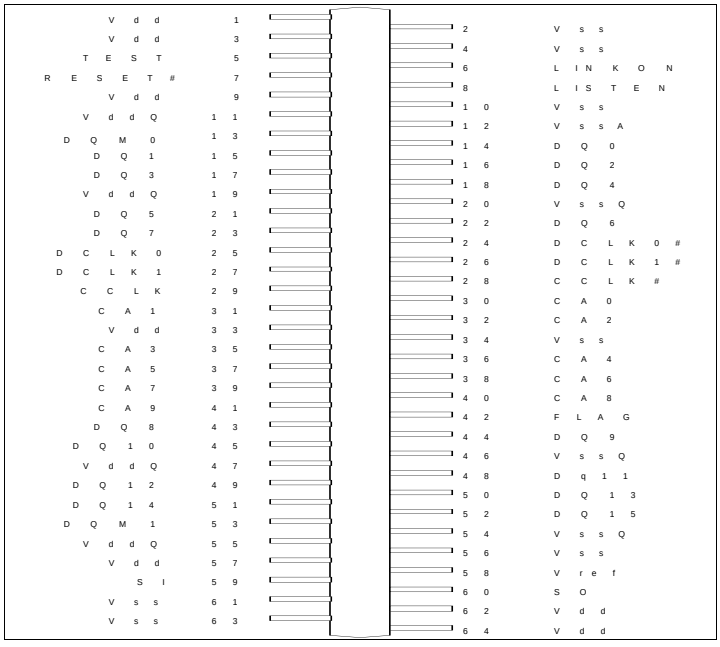
FEATURES

- Very High Speed – 400 MHz data rate
- 800 Mb/s peak I/O Bandwidth-provides very high bandwidth over narrow system memory bus
- Pipelined (Concurrent) Operation – Up to 8 transactions (in one bank, or spread across multiple banks)
- Eight (this data sheet) or more internal banks for hiding row access/precharge
- Programmable burst lengths of 4 or 8
- 100% peak bandwidth sustainable over random row as well as random column accesses, even with 8 byte bursts
- Packet Oriented Protocol – Provides pin compatibility across multiple densities
- Auto Refresh and Self Refresh
- Command Clock for commands and addresses; Bidirectional Data Clocks for read and write data
- Dual Data Clocks provide smooth handoff from one data source to another
- Programmable Offset between Data and Data Clocks
- Programmable Read Delays – Adjustable in coarse increments equal to one data bit time, and fine increments which are a fraction of a bit time; allows for specific temporal placement of data at the memory controller data pins
- Programmable Write Delays – Adjustable in coarse increments equal to one data bit time. Allows for optimally adjusted write data temporal placement by the memory controller
- Supports bank accesses (bank initially idle) and page accesses (bank active, row open)
- 64ms, 8192-cycle refresh
- SLIO Interface Technology – Drivers: calibrated VOH and VOL levels, Receivers: narrow set-up and hold windows
- Single +2.5V $\pm$ 5% power supply

OPTIONS MARKING

- Timing
  400 MHz data rate -400
- Plastic Package
  64-pin VSMP (400mil width, .4/.8mm pitch) VS
- Part Number Example: SLD4M18DR400VS-400



GENERAL DESCRIPTION

The SLD4M18DR400 SLDRAM is a synchronous, very high-speed, packet-oriented, pipelined dynamic random access memory containing 75, 497, 472 bits. The SLD4M18DR400 SLDRAM is internally configured as eight banks of 128Kx72; each of the 128Kx72 banks is organized as 1024 rows by 128 columns by 72 bits. The 72 bits per column access are transferred over the I/O interface in a burst of four 18-bit words.

All transactions begin with a request packet. Read and write request packets contain the specific command and address information required. Read and write data are transferred in packets; a single-column access involves the transfer of a single data packet, which is a burst of four 18-bit words. Data from either one or two columns in a page may be accessed with a single request packet; the latter results in a continuous burst of eight 18-bit data words.

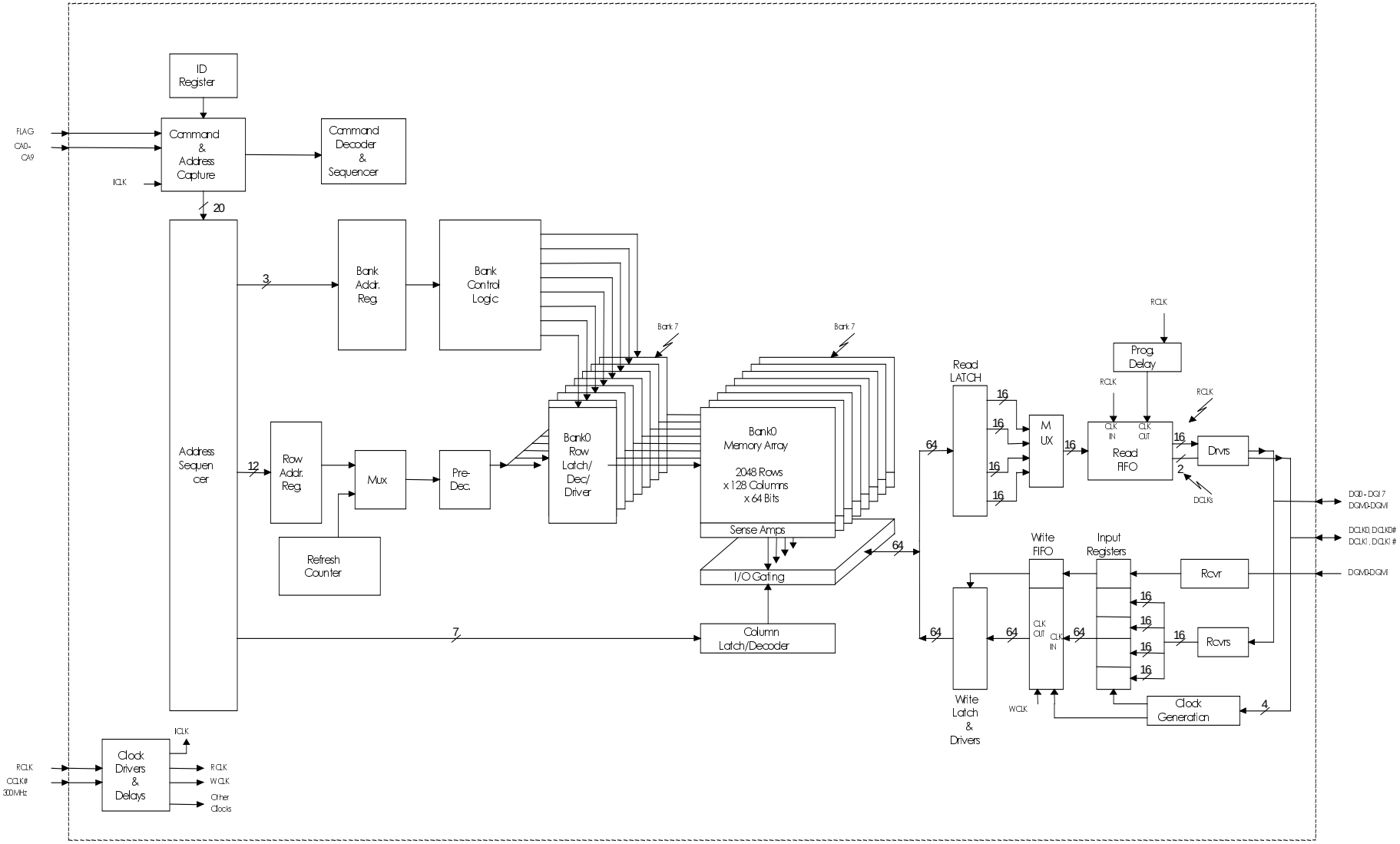
Read or write requests may be issued to idle banks, or to the open row in active banks. Read or write request indicate whether to leave the row open after the access, or to perform a self-timed precharge at the completion of the access (auto-precharge).

The SLD4M18DR400 uses a pipelined architecture and multiple internal banks to achieve high-speed operation and high effective bandwidth. Precharging one bank while accessing another bank will hide the precharge cycles, and provide seamless high-speed random access operation.

The SLD4M18DR400 is designed to operate in 2.5V memory systems. An auto-refresh mode is provided along with two power saving modes, standby and shutdown. Self-refresh is provided in the shutdown mode. The SLD4M18DR400 includes SLIO interface technology.

SLDRAMs offer substantial advances in DRAM operating performance, including the ability to synchronously burst data at a very high data rate with automatic column-address generation, the ability to interleave between several internal banks in order to hide pre charge time, and the capability to provide a continuous burst of data across random row and/or column locations, even with 8-byte granularity.

Terminology – the term “tick” is used throughout this data sheet as the equivalent of one-half of the CCLK clock period. Also, for simplicity, the clocks will be referred to and shown as CCLK, DCLK0 and DCLK1. It should be understood that these are differential clocks and that each has a complementary signal. Any reference to a specific edge of a particular clock refers to the true version of that clock (e.g. CCLK) not the complement (e.g. CCLK#).


ID Register
FLAG
CA0-CA9
CLK
Command & Address Capture
Command Decoder & Sequencer
20
Address Sequencer
3
Bank Addr. Reg.
Bank Control Logic
12
Row Addr. Reg.
Mux
Pre-Dec.
Refresh Counter
Bank 7
Bank0 Row Latch/ Dec/ Driver
Bank0 Memory Array
2048 Rows
x 128 Columns
x 64 Bits
Sense Amps
I/O Gating
7
Column Latch/Decoder
64
Read LATCH
16
MUX
RCLK
Prog. Delay
CLK IN
CLK OUT
Read FIFO
Drvrs
2
DCLKs
DQ0 - DQ17
DQM0-DQM1
DCLK0, DCLK0#
DCLK1, DCLK1#
DQM2-DQM3
Write FIFO
Input Registers
Rcvr
Rcvrs
Write Latch & Drivers
WCLK
Clock Generation
4
Clock Drivers & Delays
RCLK
OCLK#
300MHz
ICLK
WCLK
Other Clocks

VSMP PIN NUMBERS	SYMBOL	TYPE	DESCRIPTION
29, 28	CCLK, CCLK#	SLIO Input	Command Clock (differential): CCLK is driven by the memory controller (or a separate clock chip) coincident with the leading edges of the command bits. SLDRAM command input signals are effectively sampled at each crossing of internally delayed versions of CCLK/CCLK#. Read clocks, write clocks, and other internal clocks are derived from CCLK.
25, 24, 27, 26	DCLK0, DCLK0#, DCLK1, DCLK1#	SLIO Input/ Output	Data Clocks (differential): For a read access, the specified pair of DCLK0/DCLK0# or DCLK1/DCLK1# is driven by the SLDRAM, and for write accesses, the specified pair is driven by the memory controller. During read accesses, the SLDRAM provides 2 crossings on the selected DCLK pair prior to, and then 1 crossing coincident with, the beginning of each valid data word. During write accesses, the SLDRAM uses a delayed version of the DCLK pair received with the data to capture the data.
59, 60	SI/SO	LVCMOS Input, Output	Select In, Select Out: The controller and all SLDRAMs on a channel are connected in series using these pins. This connection is used to initialize the SLDRAMs.
6	LINKON	LVCMOS Input	Link On: Used to enter and exit Shutdown mode.
7	RESET#	LVCMOS Input	Reset#: Provides a hardware reset; resets all logic, including the ID register. Memory contents are not affected. An SLDRAM must be initialized following a hardware reset.
8	LISTEN	LVCMOS Input	Listen: Used to enter and exit Standby mode.
42	FLAG	SLIO Input	Flag: FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time is interpreted as a NOP.
30-32, 35-41	CA0-CA9	SLIO Input	Command, Address: Commands, Addresses and/or Register Write Data are transferred on these signals, in packets of four words.
14-18, 21-23, 43-45, 48-53, 13	DQ0-DQ17	SLIO Input/ Output	Data I/O: Data bus.
5	TEST	---	Test Pin: Should be tied to V_{SS} during normal operation.
58	V_{REF}	---	Reference Voltage.
11, 19, 47, 55	$V_{DD}Q$	Supply	DQ Power: Provide isolated power to DQs for improved noise immunity.
12, 20, 46, 54	$V_{SS}Q$	Supply	DQ Ground: Provide isolated ground to DQs for improved noise immunity.
1, 3, 9, 33, 57, 62, 64	V_{DD}	Supply	Power Supply: +2.5V $\pm$ 5%.
2, 4, 10, 34, 56, 61, 63	V_{SS}	Supply	Ground.

FUNCTIONAL DESCRIPTION

The specific SLDRAM described in this data sheet is an octal 128K x 72 DRAM which operates at 2.5V and includes a high speed, packet-oriented, synchronous 18-bit interface, and a pipelined architecture. Each of the 128K x 72 bit banks is organized as 1024 rows by 128 columns by 72 bits.

Read and write accesses begin with the application of a request packet which includes all necessary address bits. The request packet is followed, after a specific programmed delay, by a data packet, to complete the transaction.

Prior to normal operation, the SLDRAM must be initialized. The following sections provide detailed information covering device initialization, packet definition, command descriptions, register definition, and device operation.

Initialization

Power-Up/Hardware Reset

SLDRAMs must be powered-up and initialized in a predefined manner. Operational procedures other than those specified may result in undefined operation. Power must first be applied to VDD and VDDQ, then after a delay of tVTD, power must be applied to system VTERM. VTERM must be applied after VDDQ to avoid device latch-up, which may cause permanent damage to the device. VREF can be applied any time after VDDQ, but is expected to be nominally coincident with VTERM. Inputs are not recognized as valid until after VREF is applied. Upon power-up, the SLDRAM DQ and DCLK outputs will be High-Z and SO output will be driven LOW. The RESET# input should be held active for at least tRST. This hardware reset sets the internal ID Register to a value of 255, the SUB-ID Register to a value of 15, and sets programmable read and write delays to the minimum values.

Exit Shutdown/Controller Driver Adjust

A LOW level on LINKON, and a stable CCLK, must be applied prior to deasserting RESET#; then after deasserting RESET#, continue the initialization sequence as if exiting the Shutdown mode (LISTEN LOW before LINKON HIGH, bring LINKON HIGH, wait tLHHC for DLLs to lock, then bring LISTEN HIGH). [Note: external buffer devices may require that LISTEN be LOW prior to deasserting RESET#, and that an additional lock delay must occur between LINKON going HIGH and LISTEN going HIGH]. After the exit Shutdown sequence, the device is active, and the command and write timing synchronization should be
performed.

At some point prior to the start of command and write timing synchronization, the controller must perform a self-calibration of VOH and VOL on it's SLIO outputs and I/O

Command And Write Timing Synchronization

For command and write timing synchronization, the controller transmits the specified pattern on the FLAG, CA, DQ and DCLK signals, repetitively, until a LOW-to-HIGH transition is eventually detected on it's SI input (which occurs only after all devices on the channel are successfully synchronized). The controller brings it's SO output HIGH after transmitting the first cycle of the specified pattern. The pattern is broadcast to all devices connected directly to the controller and is identified by successive "1" levels on the FLAG input. During this operation, the SLDRAM devices use the SI/SO daisy-chain link to communicate to the controller that command and write timing synchronization has been completed. This is achieved by passing a LOW-to-HIGH transition from the controller SO output to the first SLDRAM SI input, and then from the first SLDRAM SO
output to the second SLDRAM SI input, etc. through the last SLDRAM SO output driving SI input of the controller. Each SLDRAM device begins command and write timing synchronization upon detecting the specified pattern but does not drive it's SO output until both the transition at it's SI input, and the completion of command and write timing synchronization have occurred.

The receipt of the special pattern on FLAG prior to the LOW-to-HIGH transition on SI differentiates this activity on the SI/SO link from the similar procedure used during ID assignment. The controller stops sending the specified pattern after detecting SI HIGH, and then waits 16 ticks before sending a valid command or resetting the SI/SO link

(the FLAG signal should be LOW for 16 ticks). This delay allows the SLDRAM devices to detect the absence of the special pattern on the FLAG input and to recognize the next HIGH level on the FLAG input as being the start of a valid command packet. The controller resets the SI/SO link by bringing it's SO LOW and waiting for it's SI to go LOW; HIGH-to-LOW transitions propagate through the link in-dependent of device status or operation.

Although this data sheet describes a 400 Mb/s/p device, it is noted for future designs that faster devices up through 800 Mb/s/p will include the capability to synchronize at the 400 Mb/s/p rate.

ID Assignment

Next, each SLDRAM on the channel(s) is sequentially assigned a unique ID and SUB-ID combination. Each SLDRAM is individually selected in turn by using the SI/SO link. This mode of operation is identified by a LOW-to-HIGH transition on SI followed by an ID Register Write Request Packet. Each ID Register Write Request will be followed by a corresponding SUB-ID Register Write Request Packet (meeting tCC), and n of these request pairs will be issued (where n equals the number of SLDRAM devices in the system). Only the SLDRAM which has SI High, ID=255 and SUB-ID=15 will react to the ID Register Write Request Packet in any given request pair. The corresponding SUB-ID Register Write Request Packet in each request pair must use the device ID just assigned by the ID Register Write Request Packet in that pair. Only the SLDRAM with that ID, with SI High, and with SUB-ID=15 will react to the SUB-ID Register Write Request Packet.

The selected SLDRAM reacts by writing the ID contained in the first packet to its internal ID Register, writing the SUB-ID contained in the second packet so its internal SUB-ID Register, and then driving its SO HIGH. The controller provides enough delay (tID plus related maximum routing delays) between the assertion of its SO output HIGH and the first issued request pair (and between subsequent issued request pairs) to allow for SO to propagate to the SI of the next device. ID assignment is complete when SI of the controller goes HIGH. Then the controller again resets the SI/SO link, as before.

Pre-Configuration/Sldram Driver Adjust

At this point the SLDRAMs can receive commands, and each SLDRAM is uniquely addressable. Next, the SLDRAM operating frequency should be programmed, and then the V_{OH} and V_{OL} calibration should be performed. The information indicating the appropriate operating frequency will either be contained in the controller itself, or can be obtained by the controller by polling some other component (jumpers, Serial Presence Detect device, etc.). The appropriate values are then written to the respective registers of each SLDRAM. For programmed operating frequencies other than 200 MHz (400 Mb/s/p) the command and write synchronization would be repeated at this point for the new frequency.

V_{OH} calibration is performed for each SLDRAM by sending a Drive DCLKs HIGH command and iteratively sending Increment/Decrement V_{OH} commands and observing the output level until the desired level is achieved. V_{OL} calibration is performed similarly using the Drive DCLKs LOW and Increment/Decrement V_{OL} commands. The controller should then issue a Disable DCLKs command packet.

Read Timing Synchronization

At this point the controller can send commands to individual SLDRAMs, and the operating frequency is selected, so read timing synchronization can be performed.

For each SLDRAM, the controller should first send at least 16 Increment Fine Read Vernier commands for DQs and DCLK0 so that the coarse counter is incremented from the reset value (minimum). This allows room for subsequent adjustments. Then the controller should send a Read Sync Request packet to that SLDRAM. The specified data patter is returned by the SLDRAM, with a delay equal to the Actual Page Read Delay. The specific delays are unknown to the controller at this point, so the controller should enable the data synchronization circuitry immediately after sending a Read Sync Request command.

The controller should then adjust internal timing to capture data. This is accomplished by adjusting the Fine Read and Data Offset Verniers until the known data pattern is captured and the capture timing is optimized. Although several approaches are possible, one suggested approach would be as follows. The first step would be to achieve data capture of the sync pattern using DCLK0, by sending Increment/Decrement Data Offset Vernier commands. Then, issue Increment/Decrement Fine Read Vernier commands for DQs and DCLK0 until the desired relationship between DCLK0 and an internal clock within the controller is achieved. Note that the capture relationship between DCLK0 and DQs established in the first step above is not changed by this second step. Next (or along with the Increment/Decrement Fine Read Vernier commands for DQs and

DCLK0), issue Increment/Decrement Fine Read Vernier commands for SCLK1 to align DCLK1 with DCLK0. The final adjustment for placing read data at the controller is the programming of the coarse latency, which is performed later.

At this point, the controller should issue a Stop Read Sync Packet, which instructs the SLDRAM to discontinue sending the sync pattern. After this is done for each SLDRAM, the controller can read data from each SLDRAM, but at an unspecified latency.

Command and Write Timing Synchronization, Write Timing Synchronization, Read Timing Synchronization or output level calibration may be repeated periodically if necessary for a given system design and environment. Such re-synchronization or re-calibration should be performed when no accesses are in progress.

Detecting And Re-Programming Read and Write Latencies

The controller may now detect the actual read latency in the system for each SLDRAM by sending a DRIVE DCLKs HIGH command followed (after tDD) by a Read Status Register Request. The controller should start monitoring the appropriate DCLK immediately after issuing the Read Status Register Request and should count clocks between sending the command and detecting the first HIGH-to-LOW transition on that DCLK. The read latency can be derived from this number. After detecting the latency, the controller should issue a Disable DCLKs command to prepare the DCLKs for normal operation.

With the latency (including system delays) now known, the remaining status registers can be read as in normal operation (i.e. without first issuing the DRIVE DCLKs HIGH command). Data from status registers is provided in a burst of 4 by the SLDRAM, at the Actual Read Latency of the device (which appears as the observed system latency at the controller).

After reading the status registers of all SLDRAMs, the controller uses the data provided, as well as the observed latencies, to determine the appropriate read latency to be programmed into the SLDRAMs.

In one suggested system design approach, the devices with shorter observed read latencies would be programmed with additional latency so as to match that of the SLDRAM(s) with the longest observed latency (for both bank and page accesses). This way, all read data arrives at the controller with the same latency from command to data, regardless of which SLDRAM device provides the data.

At this point, the controller determines the optimum write latency corresponding to the above read latecy at the controller I/O pins (optimizing the tradeoff of internal bus turnaround time and external bus turnaround time) and then must determine the corresponding write latency value for each SLDRAM (the write latency at a given SLDRAM may be different than that at the controller I/O pins, and may be different from that of other SLDRAMs). There are several possible methods for determining the appropriate values, depending on system configuration; these will be covered in separate documentation.

Once the Ids have been assigned and the timing adjusted for each SLDRAM, the channel is ready for normal operation.

FIGURE 1
Command and Data Sync Patterns

SIGNAL	REPEATING PATTERN
Flag	111101011001000…
CA9	000010100110111…
CA8	111101011001000…
CA7	000010100110111…
CA6	111101011001000…
CA5	000010100110111…
CA4	111101011001000…
CA3	000010100110111…
CA2	111101011001000…
CA1	000010100110111…
CA0	111101011001000…
DQ17	000010100110111…
DQ16	111101011001000…
DQ15	000010100110111…
DQ14	111101011001000…
DQ13	000010100110111…
DQ12	111101011001000…
DQ11	000010100110111…
DQ10	111101011001000…
DQ9	000010100110111…
DQ8	111101011001000…
DQ7	000010100110111…
DQ6	111101011001000…
DQ5	000010100110111…
DQ4	111101011001000…
DQ3	000010100110111…
DQ2	111101011001000…
DQ1	000010100110111…
DQ0	111101011001000…
DCLK1	10…
DCLK0	10…

Packet Definition

General definitions for the various packets included in the protocol are shown in the following figures. More specific definitions are included, when necessary, in the Register Definition, Command Description and Device Operation sections of this data sheet.

Read, Write, Or Row OP Request Packet

The Read, Write, or Row Op Request Packet is used to initiate any Read or Write Access, or to open or close a specific row in a specific bank.

A Read or Write request will result in the transfer of a Data Packet on the data bus at a specific time later. The Data Packet is driven by the SLDRAM for a READ, or by the memory controller for a Write. An Open Row or Close Row request generates no response.

Although unused address bits are not recognized by the SLDRAM device, zeroes should be applied for those bits, as shown.

Register Read Request Packet

The Register Read Request Packet is used to initiate a Read access to a register address. In response to a Register Read Request Packet, the SLDRAM will provide a Data Packet on the data bus at a specific time later.

Although bits REG6-REG4, and other unused bits of the packet are not needed or recognized by the SLDRAM, zeroes should be applied for those bits, as shown.

FIGURE 2
Read, Write, or Row Op Request Packet Definition

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	X	X	X	X	X	X	X	X	X	X
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	BNK2	BNK1	BNK0	ROW9	ROW8
0	ROW7	ROW6	ROW5	ROW4	ROW3	ROW2	ROW1	ROW0	0	0
0	0	0	0	COL6	COL5	COL4	COL3	COL2	COL1	COL0

ID8-ID0 = Device ID Value
CMD5-CMD0 = Command Code
BNK2-BNK0 = Bank Address
ROW9-ROW0 = Row Address
COL6-COL0 = Column Address
0 = Unused, apply 0 for this bit

FIGURE 3
Register Read Packet Definition

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	X	X	X	X	X	X	X	X	X	X
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	REG6=0	REG5=0	REG4=0	REG3	REG2
0	REG1	REG0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0

ID8-ID0 = Device ID Value
CMD5-CMD0 = Command Code
REG6-REG0 = Register Address
0 = Unused, apply 0 for this bit

Register Write Request Packet

The Register Write Request Packet is used to initiate a Write access to a register address. This packet consists of four words, with the latter two being the data to be written to the selected register.

Although bits REG6-REG4, and other unused bits of the packet are not needed or recognized by the SLDRAM, zeroes should be applied for those bits, as shown.

Event Request Packet

The Event Request Packet is used to initiate a hard or soft reset, an Autorefresh, or a Close All Rows command, or to enter or exit Self Refresh, adjust output voltage levels, adjust the Fine Read Vernier or adjust the Data Offset Vernier.

The output voltage levels, or the fine read or data offset verniers can be adjusted using a dedicated Adjust Settings Event Request Packet or as part of an Autorefresh Event. In either case, the bits ADJ0-ADJ4 and DO0-DO4 determine the specific adjustment to be made, according to Truth Table 3. An Autorefresh without adjustment is performed when ADJ0-ADJ4 are all 0.

The default values shown should be applied to the unused bits. For events other than Autorefresh or Adjust Settings, the ADJ0-ADJ4 bits are unused and zeroes should be applied to these bits. Note: bits DO0-DO4 are defined for future use, the default value for these bits is, and will be, all ones.

FIGURE 4
Register Write Packet Definition

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	X	X	X	X	X	X	X	X	X	X
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0
0	REG6=0	REG5=0	REG4=0	REG3	REG2	REG1	REG0	0	0	0
0	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0

ID8-ID0 = Device ID Value
SID4-0 = Device Sub-ID Value
RD9-RD0 = Register Data

CMD5-CMD0 = Command Code
REG6-REG0 = Register Address

FIGURE 5A
Event Packet Definition

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	X	X	X	X	X	X	X	X	X	X
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0
0	E6	E5	E4	E3	E2	E1	E0	0	0	0
0	ADJ4*	ADJ3*	ADJ2*	ADJ1*	ADJ0*	DO4*	DO3*	DO2*	DO1*	DO0*

* = For Autorefresh and Adjust Settings events only, otherwise unused (ADJx=0, Dox=1)

ID8-ID0 = Device ID Value
SID4-0 = Device Sub-ID Value
ADJ4-0 = Adjust Setting Code

CMD5-CMD0 = Command Code
E6-E0 = Event Index Code
DO4-0 = Data Offset DQ Select (future use)

Data Sync Request Packet

A Data Sync Request Packet is used to control the output logic values and patterns used for level adjustment, latency detection, and timing synchronization.

FIGURE 5B
Data Sync Request Packet Definition

Flag	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0
0	X	X	X	X	X	X	X	X	X	X
1	ID8	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	CMD5
0	CMD4	CMD3	CMD2	CMD1	CMD0	SID4	SID3	SID2	SID1	SID0

ID8-ID0 = Device ID Value
SID4-0 = Device Sub-ID Value

CMD5-CMD0 = Command Code

Data Packet

A Data Packet is provided by the controller for each Write Request, and by the SLDRAM for each Read Request. Each Data Packet contains either 8 bytes or 16 bytes, depending on whether the burst length was set to 4 or 8, respectively, in the corresponding request packet. There are no output disable or write masking capabilities within the data packet.

When the burst length of 8 is selected, the first 8 bytes in the packet correspond to the column address contained in the request packet, and the second 8 bytes correspond to the same column address except with an inverted LSB (i.e. the burst 'wraps').

FIGURE 6
Data Packet Definition (For Burst Length = 4)

DQ17 DQ16 DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9	DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
Byte 0	Byte 1
Byte 2	Byte 3
Byte 4	Byte 5
Byte 6	Byte 7

FIGURE 7
Data Packet Definition (For Burst Length = 8)

DQ17 DQ16 DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9	DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0
Byte 0	Byte 1
Byte 2	Byte 3
Byte 4	Byte 5
Byte 6	Byte 7
Byte 8	Byte 9
Byte 10	Byte 11
Byte 12	Byte 13
Byte 14	Byte 15

Truth Table 1 – Commands

CMD5	CMD4	CMD3	Command	CMD2	CMD1	CMD0	Subcommand
0	0	0		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	0	0		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	0	0		0	1	0	Read Access, Close Row, Drive DCLK0
0	0	0	Page Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	0	0	Burst of 4	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	0	0		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	0	0		1	1	0	Write Access, Close Row, Use DCLK0
0	0	0		1	1	1	Write Access, Close Row, Use DCLK1
0	0	1		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	0	1		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	0	1		0	1	0	Read Access, Close Row, Drive DCLK0
0	0	1	Page Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	0	1	Burst of 8	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	0	1		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	0	1		1	1	0	Write Access, Close Row, Use DCLK0
0	0	1		1	1	1	Write Access, Close Row, Use DCLK1
0	1	0		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	1	0		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	1	0		0	1	0	Read Access, Close Row, Drive DCLK0
0	1	0	Bank Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	1	0	Burst of 4	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	1	0		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	1	0		1	1	0	Write Access, Close Row, Use DCLK0
0	1	0		1	1	1	Write Access, Close Row, Use DCLK1
0	1	1		0	0	0	Read Access, Leave Row Open, Drive DCLK0
0	1	1		0	0	1	Read Access, Leave Row Open, Drive DCLK1
0	1	1		0	1	0	Read Access, Close Row, Drive DCLK0
0	1	1	Bank Access,	0	1	1	Read Access, Close Row, Drive DCLK1
0	1	1	Burst of 8	1	0	0	Write Access, Leave Row Open, Use DCLK0
0	1	1		1	0	1	Write Access, Leave Row Open, Use DCLK1
0	1	1		1	1	0	Write Access, Close Row, Use DCLK0
0	1	1		1	1	1	Write Access, Close Row, Use DCLK1
1	0	0		0	0	0	Reserved
1	0	0		0	0	1	Open Row
1	0	0	Register	0	1	0	Close Row
1	0	0	Access,	0	1	1	Register Write
1	0	0	Row Op,	1	0	0	Register Read, Use DCLK0
1	0	0	Or Event	1	0	1	Register Read, Use DCLK1
1	0	0		1	1	0	Reserved
1	0	0		1	1	1	Event
1	0	1		0	0	0	Read Sync (Drive both DCLKs)
1	0	1		0	0	1	Stop Read Sync
1	0	1		0	1	0	Drive DCLKs LOW
1	0	1	Data	0	1	1	Drive DCLKs HIGH
1	0	1	Sync	1	0	0	Reserved
1	0	1		1	0	1	Reserved
1	0	1		1	1	0	Disable DCLKs
1	0	1		1	1	1	Drive DCLKs Toggling
1	1	0	Reserved	X	X	X	NOP (See Note)
1	1	1	Reserved	X	X	X	Reserved

NOTE: Reserved for buffer-only commands; must be treated as NOP by SLDRAM's

FIGURE 8
Event Index Codes

*Index Range	Description
0-15	Defined Events – See Event Truth Table
16-63	Reserved
64-127	Vendor Dependent

*Index = value of E6-E0 in Event Request Packet

Truth Table 2 - Events

E6-E3	E2	E1	E0	Event
0	0	0	0	Set ID Register to 255, SUB-ID to 15, reset device
0	0	0	1	Reset device, except ID and SUB-ID Registers
0	0	1	0	Autorefresh
0	0	1	1	Close all rows
0	1	0	0	Enter Self Refresh
0	1	0	1	Exit Self Refresh
0	1	1	0	Adjust Settings
0	1	1	1	Reserved

Truth Table 3 – Adjust Settings

ADJ4	ADJ3	ADJ2	ADJ1	ADJ0	ADJUSTMENT
0	0	0	0	0	No Adjustment
0	0	0	0	1	Decrement Data Offset Vernier (move DQs sooner in time relative to DCLK0)
0	0	0	1	0	Increment Data Offset Vernier (move to DQs later in time relative to DCLK0)
0	0	0	1	1	Reset Data Offset Vernier to Zero
0	0	1	0	0	Reserved
0	0	1	0	1	Decrement Fine Read Vernier for DQs and DCLK0
0	0	1	1	0	Increment Fine Read Vernier for DQs and DCLK0
0	0	1	1	1	Reset Fine Read Vernier for DQs and DCLK0 to Zero
0	1	0	0	0	Reserved
0	1	0	0	1	Decrement Fine Read Vernier for DCLK1
0	1	0	1	0	Increment Fine Read Vernier for DCLK1
0	1	0	1	1	Reset Fine Read Vernier for DCLK1 to Zero
0	1	1	0	0	Reserved
0	1	1	0	1	Decrement VOH Level
0	1	1	1	0	Increment VOH Level
0	1	1	1	1	Reset VOH to center of range
1	0	0	0	0	Reserved
1	0	0	0	1	Decrement VOL Level
1	0	0	1	0	Increment VOL Level
1	0	0	1	1	Reset VOL to center of range
1	0	1	0	0	Reserved
1	0	1	0	1	Reserved
1	0	1	1	0	Reserved
1	0	1	1	1	Reserved
1	1	0	0	0	Reserved
1	1	0	0	1	Reserved
1	1	0	1	0	Reserved
1	1	0	1	1	Reserved
1	1	1	0	0	Reserved
1	1	1	0	1	Reserved
1	1	1	1	0	Reserved
1	1	1	1	1	Reserved

Command Descriptions

Truth Table 1 provides a quick reference of available commands. Detailed descriptions are provided in the following sections. All command packets must start on a positive edge of CCLK (with CCLK in this context being specific, not generic).

No Operation (NOP)

FLAG HIGH indicates the start of a valid request packet; FLAG then goes LOW for the remainder of the packet. FLAG LOW at any other time results in a NO OPERATION (NOP). A NOP prevents unwanted commands from being registered during idle states. NOPs do not affect operations already in progress.

Open Row

The OPEN ROW command is used to open (or activate) a row in a particular bank in preparation for a subsequent, but separate, column access command. The row remains open (or active) for accesses until a CLOSE ROW command or an access-and-close-row type command is issued to that bank. After an OPEN ROW command is issued to a given bank, a CLOSE ROW command or an access-and-close-row type command must be issued to that bank before a different row in that same bank can be opened.

The OPEN ROW command may be useful when a page access is anticipated, but the column address is not yet known, or when splitting a bank access into two components will facilitate scheduling.

Close Row

The CLOSE ROW command is used to close a row in a specific bank.

The CLOSE ROW command is used when it is desired to close a row that was previously left open in anticipation of subsequent page accesses.

Read

Page Read commands and Bank Read commands are used to initiate a read access to an open row, or to a closed row, respectively. The commands indicate the burst length, the selected DCLK, and whether to leave the row open after the access. Read data appears on the DQs subject to the corresponding Ready Delay Register value and Fine Read Vernier and Data Offset Vernier settings previously programmed into the device.

Write

Page Write commands and Bank Write commands are used to initiate a write access to an open row, or to a closed row, respectively. The commands indicate the burst length, the selected DCLK, and whether to leave the row open after the access. Write data is expected on the DQs at a time determined by the corresponding Write Delay Register value previously programmed into the device.

Register Read

Used to read the contents of the device status registers. The register data is available on the DQs after the delay determined by the Page Read Delay Register value and the Fine Read Vernier and Data Offset Vernier settings previously programmed into the devices.

Register Write

Used to write to the control registers of the device. The register data is included within the request packet containing the command.

Event

Used to issue commands not requiring a specific address within a device or devices.

Hard Reset – Sets ID register to 255, SUB-ID register to 15, and resets device, except VOH/VOL levels.

Soft Reset – Resets device, except ID and SUB-ID registers and VOH/VOL levels.

Autorefresh – Performs a refresh operation to the row or group of rows addressed by the internal refresh counter. All banks must be idle prior to performing an autorefresh event. The same adjustments that are possible with an Adjust Settings event may also be performed during an Autorefresh event.

Close All Rows – Closes any open rows in any banks.

Enter Self Refresh – Causes the device to enter the Self Refresh mode of operation.

Exit Self Refresh – Causes the device to exit the Self Refresh mode of operation.

Adjust Settings – Used to adjust the Data Offset Vernier, Fine Read Verniers, VOH levels, and VOL levels.

Read Sync (Stop Read Sync)

Instructs the SLDRAM to start (stop) transmitting the specified synchronization pattern to be used by the controller to adjust input capture timing.

Drive DCLKs Low (High)

Instructs the SLDRAM to drive the DCLK outputs LOW (HIGH) until overridden by another DRIVE DCLK or READ command. DCLK is specific in this context; the DCLK# outputs will be in the opposite state.

Drive DCLKs Toggling

Instructs the SLDRAM to drive the DCLK outputs toggling at the operating frequency of the device (i.e. DCLKn and DCLKn# will cross every tCK/2ns) until overridden by another DRIVE DCLK or READ command.

Disable DCLKs

Instructs the SLDRAM to disable (High-Z) the DCLK/DCLK# outputs until overridden by another DRIVE DCLK or READ command.

Register Definition

The SLDRAM includes two sets of registers, the control registers and the status registers. The control registers are write-only registers which are logically 20-bits wide. Physically, all control registers are currently 8-bits or less, so the remaining bits are 'don't care' to the SLDRAM. However, to allow for future revision, the controller should write a 0 to each 'don't care' bit. Data to be written to a control register is provided via the Command/Address bus as part of the Register Write Packet.

The status registers are read-only registers which are logically 72-bits wide. Physically, all status registers are currently 32-bits, so the remaining bits are driven LOW during status register reads. Data being read from a status register is provided in a burst of 4, after a delay equal to the Actual Page Read Delay previously programmed into the device.

FIGURE 9
Register Names And Addresses

REG3	REG2	REG1	REG0	Control Register	Status Register
0	0	0	0	ID	Configuration
0	0	0	1	SUB-ID	Actual Delays
0	0	1	0	Operating Frequency	Minimum Delays
0	0	1	1	Test	Maximum Delays
0	1	0	0	Page Read Delay	Test
0	1	0	1	Page Write Delay	TRAS/tRP
0	1	1	0	Bank Read Delay	TRC1/tRC2
0	1	1	1	Bank Write Delay	TRRD/tXSR
1	0	0	0	Reserved	TWR/tWRD
1	0	0	1	Reserved	TPR/tBR
1	0	1	0	Reserved	TPW/tBW
1	0	1	1	Reserved	Reserved

Figure 9 - Register Names And Addresses cont'd.

REG3	REG2	REG1	REG0	Control Register	Status Register
1	1	0	0	Reserved	Reserved
1	1	0	1	Reserved	Reserved
1	1	1	0	Reserved	Reserved
1	1	1	1	Reserved	Reserved

ABSOLUTE MAXIMUM RATINGS*

Voltage on V_{DD}/V_{DDQ} supply
relative to V_{SS}……-0.5V to +3.6V
Voltage on Inputs
relative to V_{SS}……...-0.5V to +3.6V
Voltage on SLIO Outputs or SLIO I/O pins
relative to V_{SS}…… -0.5V to VDDQ+0.5V
Voltage on LVCMOS Outputs
relative to V_{SS}……..-0.5V to VDD+0.5V
Operating Temperature, T_A (ambient)…….0'C to +70'C
Storage Temperature (plastic)……-55'C to +150'C
Power Dissipation……..1.3W
Short Circuit Output Current……50mA

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS
(Note: 1,4) (0'C$\leq$ 70'C; V_{DD}/V_{DDQ} = +2.5V$\pm$0.125V)

PARAMETER/CONDITION	SYMBOL	MIN	MAX	UNITS	NOTES
Supply Voltage	V_{DD}/V_{DDQ}	2.375	2.625	V	2
Input High (Logic 1) Voltage, SLIO	V_{IH}	V_{REF}+0.2	V_{DDQ}+0.3	V	
Input Low (Logic 0) Voltage, SLIO	V_{IL}	V_{SSQ}-0.3	V_{REF}-0.2	V	
Input High (Logic 1) Voltage, LVCMOS	V_{IH}	0.7-V_{DD}	V_{DD}+0.3	V	
Input Low (Logic 0) Voltage, LVCMOS	V_{IL}	V_{SS}-0.3	0.3V_{DD}	V	
Input Reference Voltage (SLIO)	V_{REF}	0.5V_{DD}-0.05	0.5V_{DD}+0.05	V	3
INPUT LEAKAGE CURRENT Any input 0V $\leq V_{IN} \leq V_{DD}$+0.3 (All other pins not under test = 0V)	I_I	-2	2	µA	
OUTPUT LEAKAGE CURRENT (DQs are disabled; 0V $\leq V_{OUT} \leq V_{DD}$Q + 0.3V LVCMOS, 0V $\leq V_{OUT} \leq V_{DD}$Q + 0.3V SLIO)	I_{OZ}	-10	10	µA	
OUTPUT LEVELS – SLIO Output High Voltage Output Low Voltage Calibrated Output High Voltage Calibrated Output Low Voltage	 V_{OH} V_{OL} V_{OH} V_{OL}	 1.6 1.6 0.875	 0.9 1.625 0.9	 V V V V	 10
OUTPUT LEVELS – LVCMOS Output High Voltage (I_{OH} = -100uA) Output Low Voltage (I_{OL} = 100uA)	 V_{OH} V_{OL}	 V_{DD}-0.2 	 V_{SS}+0.2	 V V	

CAPACITANCE

PARAMETER	SYMBOL	MAX	UNITS	NOTES
Input Capacitance: SLIO Inputs	C_{IS}	3	pF	5
Input Capacitance: LVCMOS Inputs	C_{IL}	5	pF	5
Input/Output Capacitance: SLIO I/O	C_{IOS}	3	pF	5
Input/Output Capacitance: LVCMOS I/O	C_{IOL}	6.5	pF	5

I_{DD} SPECIFICATIONS AND CONDITIONS
(Note: 1, 6, 13) (0'C $\leq$ T_A $\leq$ 70'C; V_{DD}/V_{DDQ} = +2.5V $\pm$0.125V)

PARAMETER/CONDITION	SYMBOL	-400 MAX @400Mb/s/p	UNITS
OPERATING CURRENT: Random Bank Reads and/or Bank Writes, Burst Length = 4, $^tRC1 \geq {}^tRC1$ MIN	I_{DD1}	256	mA
OPERATING CURRENT: Page Reads and/or Page Writes to open rows, Burst Length=4, tPR MIN, tPW=tPR	I_{DD2}	209	mA
AUTO REFRESH CURRENT: $^tRC2 \geq {}^tRC2$ MIN	I_{DD3}	192	mA
STANDBY CURRENT: Standby mode, LISTEN $\leq$ V_{IL} (MAX)	I_{DD4}	54	mA
STANDBY CURRENT: Shutdown mode, LINKON $\leq$ V_{IL} (MAX)	I_{DD5}	2.5	mA
SELF REFRESH CURRENT:	I_{DD6}	151	uA
STANDBY CURRENT: Standby-Self Refresh Mode, LISTEN $\leq$ V_{IL} (MAX)	I_{DD7}	55	uA
STANDBY CURRENT: Shutdown-Self Refresh Mode, LINKON $\leq$ V_{IL} (MAX)	I_{DD8}	3	uA

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
(0'C $\leq$ T_A $\leq$ +70'C)

AC CHARACTERISTICS		-400			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Command Input (CAn, FLAG) Valid time	^tCIV	950		ps	11
Command Input, (CAn, FLAG) Skew	^tCIS		775	ps	11
Command Clock (CCLK) Input Valid time	^tCCV	1380		ps	11
Command Clock (CCLK) Input Skew	^tCCS		560	ps	11
Clock Cycle time	^tCK	4.5	12.5	ns	
CCLK Frequency Stability/Long Term Jitter	-		4	%	
CCLK/DCLK Short Term (edge-to-edge) Jitter	-		1	%	12
Command to DCLK Delay (for DCLK HIGH, LOW, TOGGLING, or HIGH-Z)	^tDD		20	ns	
Data Input (DQn) Valid Time	^tDIV	950		ps	11
Data Input (DQn) Skew	^tDIS		775	ps	11
Data Clock Input (DCLKn) Valid Time	^tDCIV	1380		ps	11
Data Clock Input (DCLKn) Skew	^tDCIS		560	ps	11
Data Output (DQn) Valid Time	^tDOV	1900		ps	11
Data Output (DQn) Skew	^tDOS		300	ps	11
Data Clock Output (DCLKn) Valid Time	^tDCOV	2080		ps	11
Data Clock Output (DCLKn) Skew	^tDCOS		210	ps	11
Data-out high-impedance time	^tHZ		125	ps	6, 11
Data-out low-impedance time	^tLZ	125		ps	6, 11
Open Row to Close Row command period (same bank)	^tRAS	50	64	ns/us	7, 14

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS (0'C ≤ T_A ≤ +70'C) cont'd.

AC CHARACTERISTICS		**-400**			
PARAMETER	**SYM**	**MIN**	**MAX**	**UNITS**	**NOTES**
Open Row to Open Row command period (same bank)	$^tRC1$	80		ns	7
Auto Refresh to Auto Refresh Command period	$^tRC2$	80		ns	7
Refresh period (8, 192 cycles)	^tREF		64	ms	
Close Row (precharge) command period	^tRP	25		ns	7
Open Row to Open Row command period (different bank)	^tRRD	10		ns	7
Reset Inactive to Linkon Active Set Up Time	^tRL	0		ns	
Write recovery time	^tWR	14		ns	7
Exit SELF REFRESH to Open Row command	^tXSR	80		ns	7
Minimum Page Read Delay	$^tPR(^tAA)$		26-30	ns	7
Minimum Bank Read Delay	^tBR (^tRAC)		56-64	ns	7
Minimum Page Write Delay	^tPW	15		ns	7
Minimum Bank Write Delay	^tBW	30		ns	7
Maximum Page Read Delay	^tPR_MAX		32	ticks	
Maximum Bank Read Delay	^tBR_MAX		64	ticks	
Maximum Page Write Delay	^tPW_MAX		32	ticks	
Maximum Bank Write Delay	^tBW_MAX		64	ticks	
Minimum Read to Write Delay (external I/O turnaround)	^tRWD	5		ns	
Minimum Write to Read Delay	^tWRD	45		ns	7,8
VDD/VDDQ to Vterm Set Up Time	^tVTD	2		us	
VREF to Inputs Valid Set Up Time	^tIV	0		ns	
Reset# Pulse Width	^tRST	100		ns	
Input Set Up Time	^tSI	10		ns	11
ID Write Request to SO Output Delay	^tID		18	ns	
Listen to Linkon Low Set Up Time	^tLLS	5		ns	
Listen to Linkon Low Hold Time	^tLLH	5		ns	
Listen to Linkon High Set Up Time	^tLHS	0		ns	
Listen to Linkon High Hold Time – Cold	^tLHHC	13.5		us	11,13
Listen to Linkon High Hold Time – Warm	^tLHHW	100		ns	11,13
Input to Listen Set Up Time	^tILS	0		Ns	
Input to Listen Hold Time	^tILH	5		ns	
Listen to Next Command Set Up Time	^tLSC	10		ns	
Vernier Adjust to Output Delay (no accesses in progress)	^tVO		10	ns	
VOH/VOL Adjust to Output Delay (no accesses in progress)	^tLO		10	ns	
Control Register Write to Next Command Set Up Time (all banks closed)	^tCC	10		ns	15
Clock Stable to Reset# Inactive Set Up Time	^tCSI	100		ns	9
Clock Stable to Linkon High Set Up Time	^tCS	1		^tCK	
Last Command to Listen Low Set Up Time	^tPLI	0		ns	
Close Row to Last Data Out Set Up Time	^tCRDO		3	ticks	
Last Previous Data to Next DCLK Preamble Delay	^tDDC	4		ticks	
VDD to RESET# High Set Up Time	^tVRST	50		us	

NOTES

1. All voltages referenced to V_{SS}.
2. $V_{DDQ} \leq V_{DD}$.
3. $[V_{TERM} – V_{REF}] \leq 50mV$.
4. Variations in V_{DDQ}, V_{TERM}, and V_{REF} must track each other.
5. This parameter is sampled. V_{DD}, V_{DDQ}=+2.5V $\pm$0.125V; f = 1 MHz, tA = 25 deg. C.
6. tHZ and tLZ specifications reflect the transition time between the V_{TERM} voltage to which the signal is terminated in the system and the valid input logic levels. These parameters are not tested directly, but are indirectly verified in testing the skew of the output signals.

7. This parameter may consist of analog and digital components, such that the total value can be optimized at different clock frequencies. The values of the analog and digital components can be obtained from the corresponding Timing Parameter register. The total value contained in this table is calculated using tCK = tCK MIN.
8. This parameter includes margin to cover tAA guardband and possible rounding error.
9. An external buffer device in the system may have a more restrictive value for this parameter.
10. The output voltage is measured on the bus side of the series (stub) resistor, with a parallel resistor to VTERM. The output voltages are shown for a series resistor value of 20 ohms and a parallel resistor value of 28 ohms.
11. This value is specific to 400 Mb/s/p operation and must be recalculated for other data rates.
12. This specification is actually a combined jitter and “duty cycle” specification. The value shown represents that portion of the total output uncertainty appearing on DCLK or CCLK signals which is allocated to jitter and/or “duty cycle” variation. This is accounted for in the output valid and output skew specifications for those signals.
13. Cold applies when following reset; Warm applies after exiting shutdown (with no reset).
14. Min is in ns, Max is in us. Only the Min value is represented in the corresponding Timing Parameter register.
15. Measured from end of one command packet to start of next command packet.