16Mbit Enhanced SDRAM Family
4Mx4, 2Mx8, 1Mx16

Product Brief

Features

- 100% Pin, Function, and Timing Compatible with JEDEC standard SDRAM
- Integrated 8Kbit SRAM Row Cache
- Synchronous Operation up to 150MHz
- 24ns Row Access Latency, 11ns Column Latency
- Early Auto-Precharge
- Programmable Burst Length (1, 2, 4, 8, full page)
- Programmable CAS Latency (1, 2, 3)
- Hidden Auto-Refresh without closing Read Pages
- Low Power Suspend, Self-Refresh, and Power Down Modes
- Optional No Write Transfer Mode
- Single 3.3V Power Supply
- Flexible V_{DDQ} Supports LVTTL and 2.5V I/O
- Packages: 44-pin TSOP-II (400 mils wide)
  50-pin TSOP-II (400 mils wide)

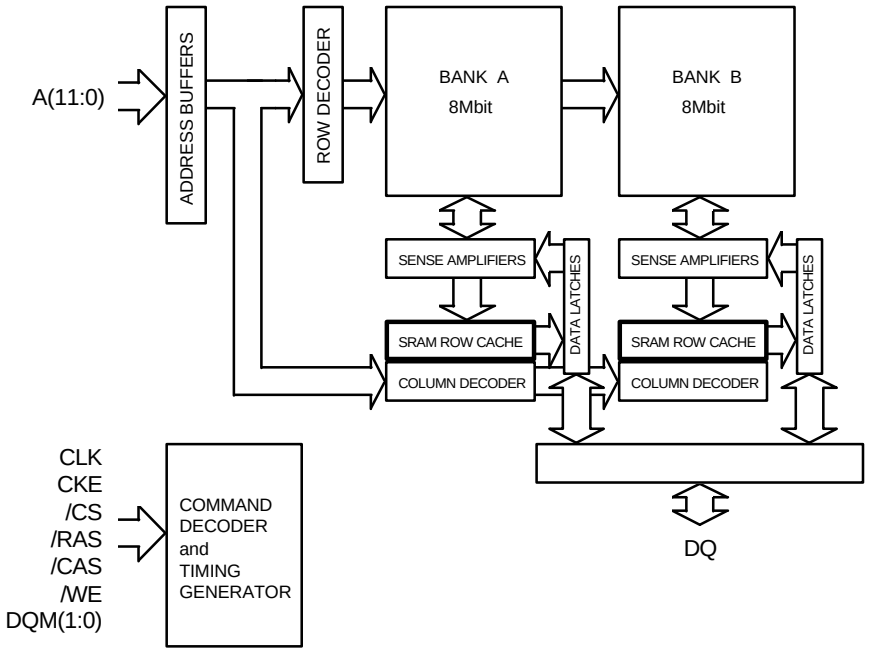
Description

The Enhanced Memory Systems 16Mb enhanced SDRAM (ESDRAM) family combines raw speed with innovative architecture to optimize system price-performance in high performance computer and embedded control systems.

The ESDRAM is pin compatible with JEDEC standard SDRAM. It is also function and timing compatible with JEDEC standard SDRAM.

The two bank architecture combines 24ns DRAM arrays with a 11ns SRAM row cache per bank. The ESDRAM is a superset technology of JEDEC standard SDRAM. Its two key functional features include early auto-precharge (close DRAM page while burst reads are performed) and an optional No Write Transfer mode. The ESDRAM is capable of maintaining two open read pages and two open write pages simultaneously via the No Write Transfer mode.

FUNCTIONAL BLOCK DIAGRAM



Product	Cache Size
4Mx4	1Kx4
2Mx8	512x8
1Mx16	256x16

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Architecture

The ESDRAM architecture combines two banks of fast 24ns DRAM with two banks of 11ns SRAM row register cache on one chip to improve memory latency. On a page read miss, a DRAM bank is activated and data is developed by the DRAM sense amplifiers in 13.3ns. The sense amplifiers now hold an entire row of data (4K bits). On a read command, the entire row is latched into the SRAM row register and the specified starting address is output in 11ns (CAS Latency 1 at clock frequencies up to 83MHz, and CAS Latency 2 up to 150MHz). The architecture allows fast 11ns latency to any of the constantly open rows on page hits.

Early auto-precharge can be performed since row data is latched separately in the SRAM row cache from the DRAM sense amplifiers. The precharge time can be hidden behind a burst read from cache. This minimizes subsequent page miss latency. The auto-precharge begins one clock cycle after the Read-Autoprecharge command and completes early enough to allow the next pipelined random access to complete by the end of the current burst cycle.

At 150MHz, all but one cycle of the next random access to any location in the same bank can be hidden to increase sustained bandwidth by up to two times over standard SDRAM. For interleaved burst read accesses, the entire precharge time is hidden and output data can be driven without any wait states.

The ESDRAM architecture also offers the designer two different cache load strategies via the mode register set for write cycles. In Write Transfer mode, the row register cache is always loaded with the sense amplifier contents (DRAM row data) on a write command. This ensures coherency between the row cache and the DRAM array. This allows read-modify-write cycles and simplified memory control logic.

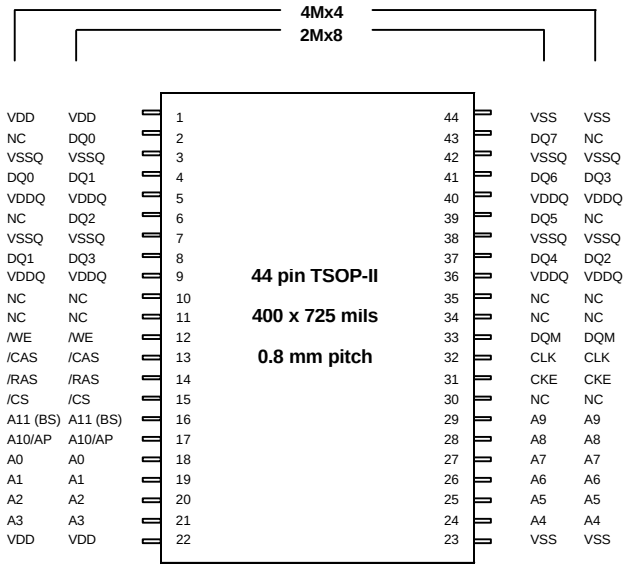
In No Write Transfer mode, the row register caches are not loaded during writes. Data is written to the DRAM sense amplifiers and the prior row contents are maintained in the row cache (for write page misses). If the on-chip page hit/miss comparator determines that the write is to the same row latched in the SRAM row cache, the write updates the row cache as well as the DRAM sense amplifiers to maintain coherency. No Write Transfer mode allows immediate return to the prior cached read page without otherwise incurring a page miss penalty. Write page precharge and a bank activate times can be hidden during cache reads. The ESDRAM's fast precharge time minimizes latency between the end of a write and the next read or write miss cycle. If a cache read follows a write cycle, write precharge time can be hidden.

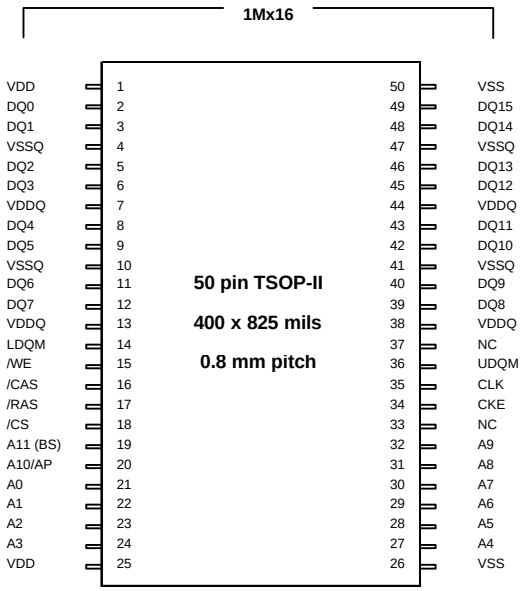
The synchronous interface of the ESDRAM allows operation at clock rates up to 150MHz with 2.5V I/O levels. Fast input set-up and clock-to-output times allow actual system operation at the specified clock rate.

Compatibility

By making the ESDRAM exactly pin-compatible with JEDEC standard SDRAM, it is possible for the memory controller to support both types of memory with a simple mode selection. Both SDRAM and ESDRAM use identical memory footprints on the planar and identical DIMM module wiring. Systems designed to support both memory types can provide two distinct price/performance points and a simple field upgrade with the ESDRAM.

PINOUTS





Basic Operating Modes

The ESDRAM operating modes are specified in the following text and in the table below.

Hit and Miss Terminology - "Hit" and "miss" refer to whether or not a new row address presented to the ESDRAM matches a row already activated in the device. There are up to two rows or "pages" that can be open at any given point in time. The row data or page contents consist of 4096 bits and are held in each bank's sense amplifiers. Each page is selected by the bank select pin A11 (BS). Each bank's SRAM row cache is loaded only when a read command is issued. The ESDRAM's on-chip row address comparator is used only in No Write Transfer mode of operation.

The memory controller typically stores page (row) address tags in order to determine which command to issue based on the tag compare result.

Mode Register Set - Two mode registers are loaded from pins A11 (BS) and A10-A0 when /CS, /RAS, /CAS, and /WE are low. The standard mode register specifies the burst length, burst type, CAS latency, and write transfer mode.

Bank Activate - A11 (BS) specifies one of the two banks and the row address A10-A0 specifies which of the 2048 rows to load into its sense amplifiers. In No Write Transfer mode, the ESDRAM compares the last row read address to the current row address. If the two row addresses match, a subsequent write updates the SRAM row cache in addition to the DRAM. If the row addresses do not match, only the DRAM is written.

Write - The ESDRAM performs a write or burst write to the bank specified by A11 (BS) and begins writing at the start address specified by the column address A9-A0. If the A10/AP pin is high, the auto-precharge operation begins one cycle following the last write of the burst.
Note: In No Write Transfer mode, if the on-chip hit/miss comparator result (from ACTV cycle) indicates a page hit, then the write is performed to both the row cache and the DRAM.

Read - The ESDRAM loads the row cache and performs a read or burst read from the cache to the bank specified by A11 (BS) and begins reading at the start address specified by the column address A9-A0. If the A10/AP pin is high, the auto-precharge operation begins one cycle following this command. The first read data is output from the memory after the CAS latency (defined by the Mode Register Set) has been satisfied.

Burst Terminate - The ESDRAM terminates a burst read after a delay equal to the CAS latency. It will terminate a burst write and mask data in the current cycle.

Single Bank Precharge - The ESDRAM will perform a manual precharge of the bank specified by A11 (BS) while A10/AP is low. Manual precharge terminates a burst read after a delay equal to the CAS latency. It will also terminate a burst write and mask data in the current cycle.

Precharge All Banks - The ESDRAM will precharge both open banks if A10/AP is high. It will terminate burst cycles exactly the same as the Single Bank Precharge command.

Auto Refresh (CBR) - The ESDRAM will perform an internal refresh cycle on both DRAM banks. Both banks must be closed before this command is executed. Unlike standard SDRAM, this command can be executed while performing cache burst reads. The contents of each row cache are not lost during Auto Refresh cycles.

Self Refresh Entry - The ESDRAM enters a self refresh mode with refresh cycles automatically generated by an internal clock. Self Refresh mode continues as long as CKE is low. All input buffers except CKE are disabled. The chip is in a low power standby mode.

Device Deselect - When /CS is high, the command decoder is disabled but the prior command will be completed (i.e. a burst will complete).

Clock Suspend/Standby Mode - When CKE is low, the internal execution of the current command is suspended until CKE returns high.

Power Down Entry/Exit - If both DRAM banks are precharged, CKE is low, and /CS is high, the chip will enter its power down mode. Once the chip is in power down mode, the chip will exit power down mode one clock after CKE is returned high.

Data Write/Output Enable - When DQM is low, write data is written to the chip during a write command and the output buffers are enabled during read commands. DQM latency is two cycles for reads and zero cycles for writes.

Data Mask/Output Disable - When DQM is high, write data is masked during a write command and the output buffers are disabled during read commands. DQM latency is two cycles for reads and zero cycles for writes.

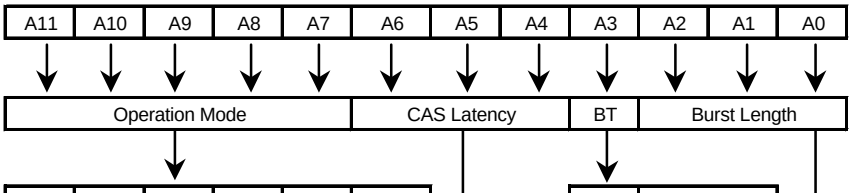
ESDRAM Command Truth Table

Function	CKE		/CS	/RAS	/CAS	/WE	DQM	A11	A10/AP	A9-A0
	Previous Cycle	Current Cycle								
Mode Register Set	H	X	L	L	L	L	X	Op Code		
Bank Activate	H	X	L	L	H	H	X	BS	Row Address	
Read	H	X	L	H	L	H	X	BS	X	Column
Read with Auto-Precharge	H	X	L	H	L	H	X	BS	X	Column
Write	H	X	L	H	L	L	X	BS	X	Column
Write with Auto-Precharge	H	X	L	H	L	L	X	BS	X	Column
Burst Termination	H	X	L	H	H	L	X	X	X	X
Single Bank Precharge	H	X	L	L	H	L	X	BS	X	X
Precharge All Banks	H	X	L	L	H	L	X	X	X	X
Auto-Refresh (CBR)	H	H	L	L	L	H	X	X	X	X
Self Refresh Entry	H	L	L	L	L	H	X	X	X	X
Self Refresh Exit	L	H	NOP or DESEL				X	X	X	X
No Operation	H	X	L	H	H	H	X	X	X	X
Device Deselect	H	X	H	X	X	X	X	X	X	X
Clock Suspend/Standby	L	X	X	X	X	X	X	X	X	X
Power Down Mode Entry	H	L	NOP or DESEL				X	X	X	X
Power Down Mode Exit	L	H	NOP or DESEL				X	X	X	X
Data Write/Output Enable	H	X	X	X	X	X	L	X	X	X
Data Mask/Output Disable	H	X	X	X	X	X	H	X	X	X

Pin Description

Symbol	Type	Function
CLK	Input	Clock: All ESDRAM input signals are sampled on the positive edge of CLK.
CKE	Input	Clock Enable: Activates the CLK signal when high and deactivates CLK internally. CKE low initiates the Power Down, Suspend, and Self-Refresh modes.
/CS	Input	Chip Select: Active low /CS enables the command decoder and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
/RAS, /CAS, /WE	Input	Command Inputs: Sampled on the rising edge of CLK, these inputs define the command to be executed.
A11 (BS)	Input	Bank Address: This input defines to which of the 2 banks a given command is being applied. This address input is also used to program the Mode Register.
A10-A0	Input	Address Inputs: A10-A0 defines the row address for the Bank Activate command. A9-A0 define the column address for Read and Write commands. A10/AP invokes the Auto-Precharge operation. During manual Precharge commands, A10/AP low specifies a single bank precharge while A10/AP high precharges all banks. The address inputs are also used to program the Mode Register.
DQ15-DQ0	Input/ Output	Data I/O: Data bus inputs and outputs. For Write cycles, input data is applied to these pins and must be set-up and held relative to the rising edge of clock. For Read cycles, the device drives output data on these pins after the CAS latency is satisfied.
UDQM, LDQM	Input	Data I/O Mask Inputs: DQM inputs mask write data (zero latency) and acts as a synchronous output enable (2 cycle latency) for read data.
V_{DD}, V_{SS}	Supply	Power (+3.3V) and ground for the input buffers and core logic.
V_{DDQ}, V_{SSQ}	Supply	Isolated power supply and ground for output buffers. V_{DDQ} may be connected to either 3.3V or 2.5V power.

Mode Register Set (Address Input for Mode Set)



M11	M10	M9	M8	M7	Mode
0	0	0	0	0	Write Transfer
0	0	1	0	0	No Write Transfer

M3	Burst Type
0	Sequential
1	Interleaved

M6	M5	M4	CAS Latency
0	0	0	Reserved
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

			Burst Length	
M2	M1	M0	Sequential	Interleaved
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

Clock Frequency

The following table specifies the operation of the ESDRAM at clock rates ranging from 66MHz to 150MHz. Clock rates up to 133MHz assume the use of LVTTL I/O levels. Clock rates from 133MHz to 150MHz assume the use of 2.5V I/O levels.

ESDRAM input setup time is 2ns at 133MHz. ESDRAM clock to output delay is 4.5ns at 133MHz. These improved I/O specifications allow ESDRAM to operate in real systems at the specified clock rate.

AC Parameters (T_A = 0°C to + 70°C)

Symbol	Parameter	-6.6		-7.5		-10		Units
		Min	Max	Min	Max	Min	Max	
Clock and CKE Parameters								
t_{CK2}	Clock Cycle Time, CL=2, 3	6.6	**150MHz**	7.5	**133MHz**	10	**100MHz**	ns
t_{CK1}	Clock Cycle Time, CL=1	13.3	**83MHz**	15	**66MHz**	15	**66MHz**	ns
t_{AC2}	Clock Access Time, CL=2, 3	-	4.3	-	4.5	-	5.0	ns
t_{AC1}	Clock Access Time, CL=1	-	11.0	-	11.5	-	11.5	ns
t_{CKH2}, t_{CKL2}	Clock High & Low Times (CL=2,3)	2.8	-	2.8	-	3.5	-	ns
t_{CKH1}, t_{CKL1}	Clock High & Low Times (CL=1)	4	-	5	-	5	-	ns
t_{CKES}	Clock Enable Set-Up Time	2.2	-	2.2	-	3.0	-	ns
t_{CKEH}	Clock Enable Hold Time	1.0	-	1.0	-	1.0	-	ns
t_{CKESP}	CKE Set-Up Time (Power down mode)	2.2	-	2.2	-	3.0	-	ns
t_T	Transition Time (Rise and Fall)	-	4	-	4	-	4	ns
Common Parameters								
t_{CS}	Command and Address Set-Up Time	2.2	-	2.2	-	3.0	-	ns
t_{CH}	Command and Address Hold Time	1.0	-	1.0	-	1.0	-	ns
t_{RCD}	RAS to CAS Delay Time	13.3	-	15	-	15	-	ns
t_{RC}	Bank Cycle Time	37.5	120K	37.5	120K	45	120K	ns
t_{RAS}	Bank Active Time	20	120K	22.5	120K	30	120K	ns
t_{RP}	Precharge Time	13.3	-	15	-	15	-	ns
t_{RRD}	Bank to Bank Delay Time (Alt. Bank)	13.3	-	15	-	15	-	ns
t_{CCD}	CAS to CAS Delay Time (Same Bank)	6.6	-	7.5	-	10	-	ns
Read and Write Parameters								
t_{OH1}	Data Output Hold Time (CL=1)	3.0	-	3.0	-	3.0	-	ns
t_{OH2}	Data Output Hold Time (CL=2,3)	2.0	-	2.0	-	2.0	-	ns
t_{LZ}	Data Output to Low-Z Time	0	-	0	-	0	-	ns
t_{HZ1}	Data Output to High-Z Time (CL=1)	-	7.0	-	7.5	-	8.0	ns
t_{HZ2}	Data Output to High-Z Time (CL=2,3)	-	4.3	-	4.5	-	5.0	ns
t_{DQZ}	DQM Data Output Disable Time	2	-	2	-	2	-	CLK
t_{DS}	Data Input Set-Up Time	2.0	-	2.0	-	2.0	-	ns
t_{DH}	Data Input Hold Time	1.0	-	1.0	-	1.0	-	ns
t_{DPL}	Data Input to Precharge	6.6	-	7.5	-	10	-	ns
t_{DAL}	Data Input to ACTV/Refresh	20	-	22.5	-	30	-	ns
t_{DQW}	Data Write Mask Latency	0	-	0	-	0	-	CLK
Refresh Parameters								
t_{REF}	Refresh Period (2048 cycles)	-	64	-	64	-	64	ms
t_{SREX}	Self Refresh Exit Time	2CLK +t_{RC}	-	2CLK +t_{RC}	-	2CLK +t_{RC}	-	ns

Clock Frequency and Latency (-6.6ns Speed Bin)

		Clock Frequency (MHz)					
Symbol	**Parameter**	**66**	**75**	**100**	**133**	**150**	**Units**
t_{CK}	Clock Cycle Time	15	13.3	10	7.5	6.6	ns
t_{AA}	CAS Latency	1	1	2	2	2	t_{CK}
t_{RCD}	RAS to CAS Delay	1	1	2	2	2	t_{CK}
t_{RL}	RAS Latency	2	2	4	4	4	t_{CK}
t_{RC}	Bank Cycle Time	3	3	4	5	6	t_{CK}
t_{RAS}	Minimum Bank Active Time	2	2	3	3	3	t_{CK}
t_{RP}	Precharge Time	1	1	2	2	2	t_{CK}
t_{DPL}	Data-In to Precharge Time	1	1	1	1	1	t_{CK}
t_{DAL}	Data-In to Active/Refresh	2	2	3	3	3	t_{CK}
t_{RRD}	Bank to Bank Delay Time	1	1	2	2	2	t_{CK}
t_{CCD}	CAS to CAS Delay Time	1	1	1	1	1	t_{CK}

Performance Comparison at 133MHz (ESDRAM vs. SDRAM*)

	Page Open		Page Closed	
	ESDRAM	**SDRAM**	**ESDRAM**	**SDRAM**
Read Page Hit	2-1-1-1	4-1-1-1	2-1-1-1	illegal
Read Page Miss	6-1-1-1	8-1-1-1	4-1-1-1, 2-1-1-1	7-1-1-1, 9-1-1-1
Write Page Hit	1-1-1-1	1-1-1-1	illegal	illegal
Write Page Miss	5-1-1-1	9-1-1-1	2-1-1-1, 5-1-1-1	3-1-1-1, 9-1-1-1

* Assumes SDRAM has fast enough clock access time to satisfy 133MHz system bus.

ESDRAM Concurrent Operations Improve System Performance

The ESDRAM's row cache allows unique concurrent operations not supported by the industry standard SDRAM. The timing diagram below describes the ability of the ESDRAM to fully pipeline random row read bursts to the same bank at 133MHz.

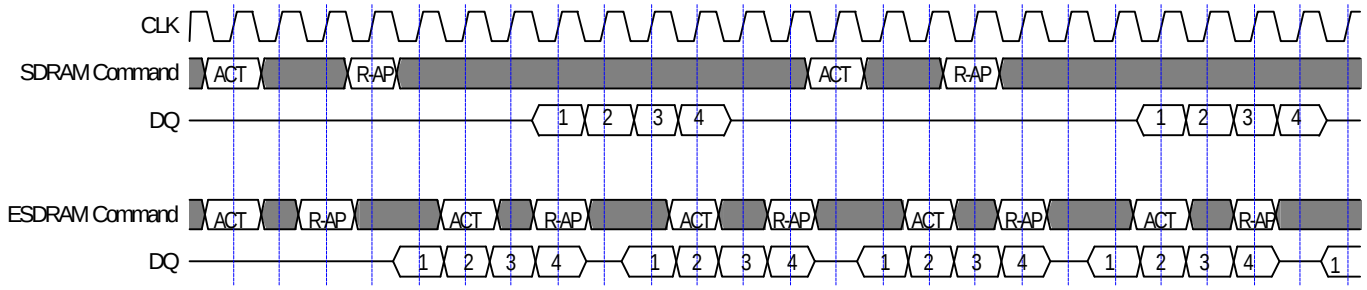
The top timing diagram shows the SDRAM performing a bank activate at T0. The SDRAM must wait until T3 for a read command (RCD Latency = 3). The first word of the four-word burst reaches the output pins 3 cycles after the read command (CAS Latency = 4). The SDRAM cannot begin to precharge the current DRAM bank until one cycle before the end of the current burst. Following the auto-precharge cycle, the next data burst from the same bank cannot start until T20. The SDRAM incurs a total of 9 dead bus cycles on back to back random reads at 133MHz.

The ESDRAM also activates its bank at T0. Because of the faster ESDRAM array, the read command can start at T2 (RCD Latency = 2). The first word of the four-word burst reaches the output pins 2 cycles after the read command (CAS Latency = 2). ESDRAM initial latency is 75% faster than SDRAM at 133MHz. The ESDRAM can begin auto-precharge of the current DRAM bank at cycle T3, one cycle after the read command. This is the direct result of having a row cache. The read command automatically loads the row cache allowing the data burst to come from the cache while the DRAM is free to prepare the next random access. The ESDRAM has completed its precharge by T5, so the ESDRAM is ready for the next random access at that time. The next read access can occur concurrently with the last few words of the first burst. The second burst read begins at T9, eleven cycles earlier than SDRAM. The ESDRAM can move 2.6 times more random data over the data bus at 133MHz due to its faster memory speed and its ability to efficiently pipeline random access cycles.

In addition to pipelining random access read cycles, ESDRAM also improves system performance by allowing:

- Hidden Refresh Cycles During Cache Reads
- Hidden Precharge and Bank Activate for a Write Miss Following Cache Reads
- Reduced Precharge and Bank Activate Latency on Back to Back Write Miss Cycles
- Immediate Access to Cache Reads while DRAM Page is Closed

Random Row Read to the Same Bank at 133MHz, BL=4



Ordering Information

Part Number	CAS Latencies	I/O Width	I/O Type	Package	Power Supply	Maximum Operating Frequency (MHz)
SM2402T-6.6	1, 2, 3	x4	LVTTL, 2.5V	44 pin TSOP-II 400 mil	3.3V	150
SM2403T-6.6	1, 2, 3	x8	LVTTL, 2.5V	44 pin TSOP-II 400 mil	3.3V	150
SM2404T-6.6	1, 2, 3	x16	LVTTL, 2.5V	50 pin TSOP-II 400 mil	3.3V	150
SM2402T-7.5	1, 2, 3	x4	LVTTL, 2.5V	44 pin TSOP-II 400 mil	3.3V	133
SM2403T-7.5	1, 2, 3	x8	LVTTL, 2.5V	44 pin TSOP-II 400 mil	3.3V	133
SM2404T-7.5	1, 2, 3	x16	LVTTL, 2.5V	50 pin TSOP-II 400 mil	3.3V	133
SM2402T-10	1, 2, 3	x4	LVTTL, 2.5V	44 pin TSOP-II 400 mil	3.3V	100
SM2403T-10	1, 2, 3	x8	LVTTL, 2.5V	44 pin TSOP-II 400 mil	3.3V	100
SM2404T-10	1, 2, 3	x16	LVTTL, 2.5V	50 pin TSOP-II 400 mil	3.3V	100