SED1278

CMOS DOT MATRIX LCD CONTROLLER DRIVER

■ DESCRIPTION

The SED1278 is a character LCD controller-driver, capable of driving displays as large as 2 lines of 8 characters (5 × 8 pixels), with minimum external components.

The SED1278 has an internal CGROM consisting of 240 characters (5 × 7) plus the underline cursor, JIS, ASCII, and eight user-programmable characters in RAM.

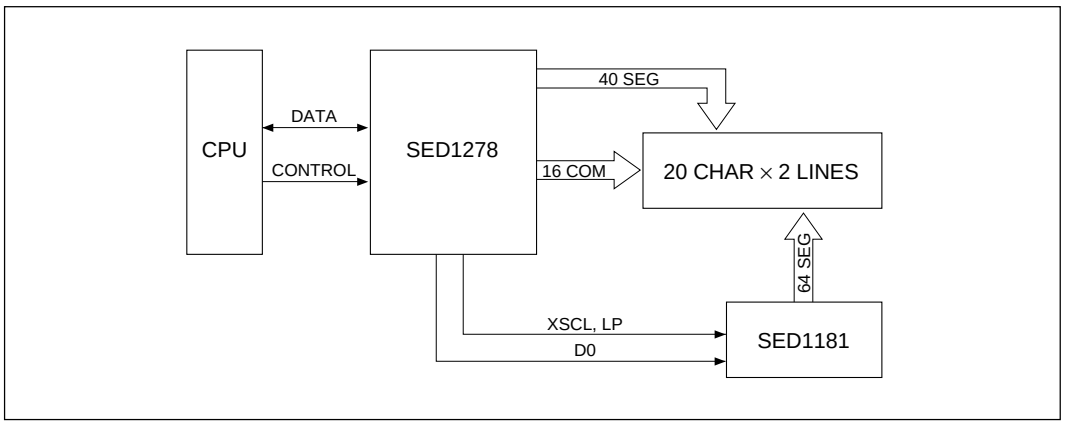
The SED1278 has 40 segment output and 16 common output built-in. Thus, one chip is capable of displaying up to 16 characters. The SED1278 can display one line of 48 characters using an SED1681F (80-bit output) as an expansion segment driver.

The SED1278 is fabricated using a silicon gate CMOS technology process and features very low power dissipation. This makes the device suitable for handheld and portable applications.

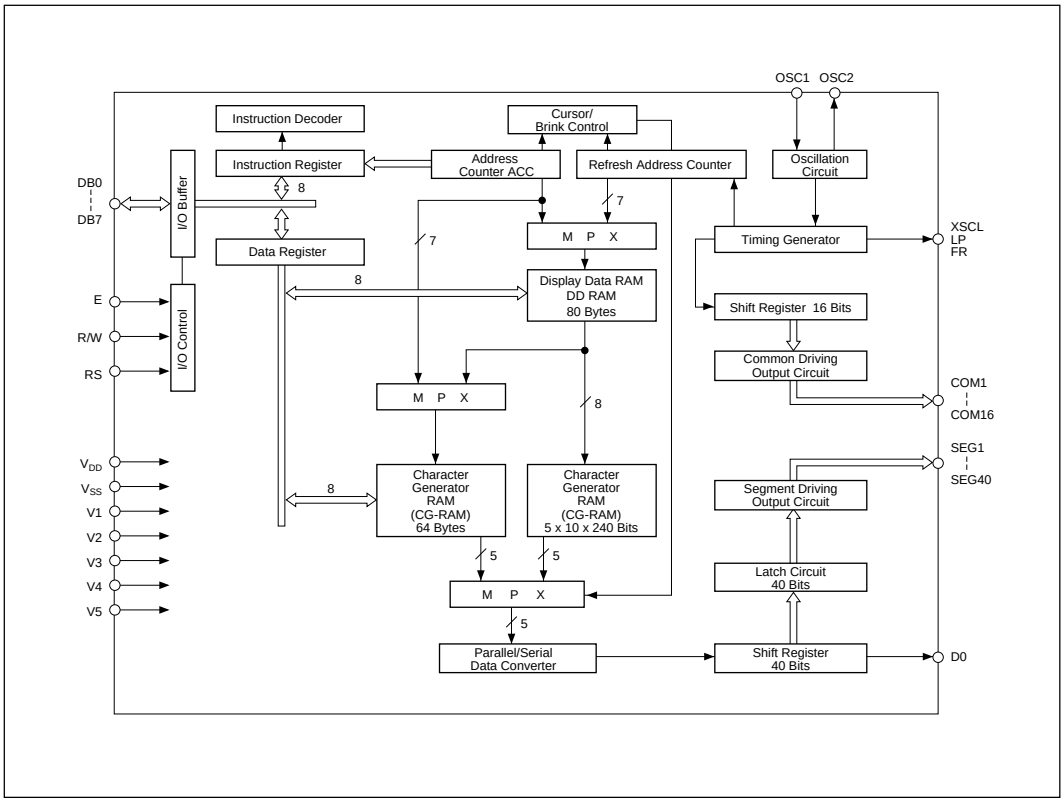
■ FEATURES

- Low-power CMOS technology
- 40 segment output
- 16 common output
- Duty: 1/8 or 1/16 (set by command)
- 4/8-bit CPU data interface, TTL compatible
- Two frame AC drive wave form
- CGROM: ..... 240 characters
- CGRAM: ..... 8 characters
- Display data RAM: ... 80 × 8 bits (80 characters)
- Recommended expansion segment driver:
  SED1181F$_{LA}$ (64 output)
  SED1681F (80 output)
- Built-in power on power-on reset
- Built-in RC oscillator
- Built-in LCD driver voltage-divider network
- TTL compatible CPU interface
- Supply voltage ..... Logic: 4.5V to 5.5V
  LCD: 3.5V to 5.5V
- Package:
  QFP5-80 pins (F$_{0A}$, F$_{0B}$, F$_{0C}$, F$_{0D}$, F$_{0G}$, F$_{0H}$)
  Al pad (D$_{0A}$, D$_{0B}$, D$_{0C}$, D$_{0D}$, D$_{0G}$, D$_{0H}$)

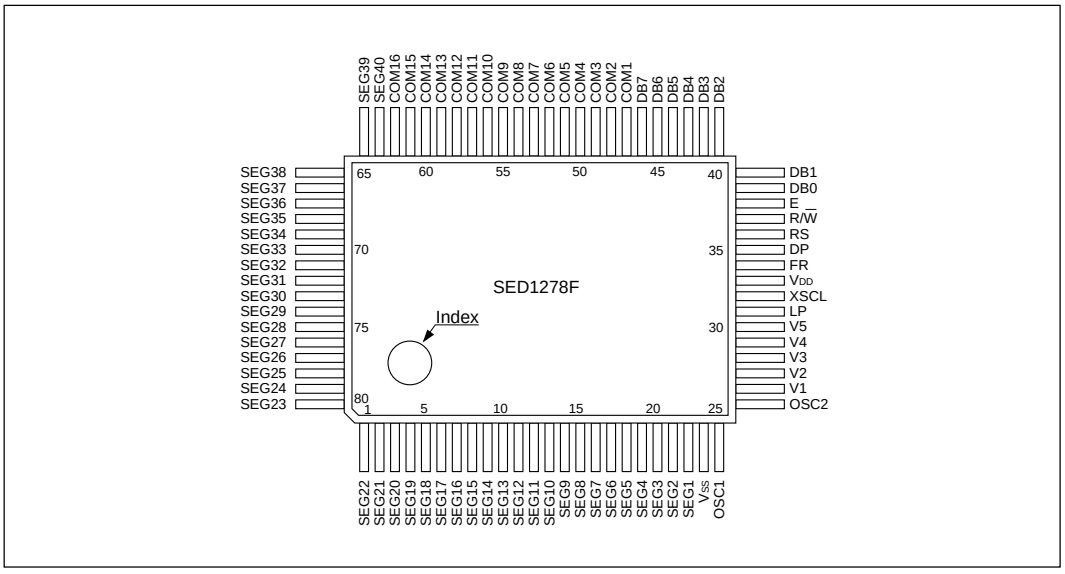
■ SYSTEM BLOCK DIAGRAM



■ BLOCK DIAGRAM



■ PIN CONFIGURATION



■ PIN DESCRIPTION

Symbol	No. of signals	Functions	
RS	1	Register select signal	∗1
R/$\overline{W}$	1	Read/write select signal	
E	1	Read/write execute signal	
DB0 to DB7	8	Data bus	
LP	1	Data latching pulse	
XSCL	1	Data transfer clock	
FR	1	LCD AC driving signal	
DO	1	Serial data	
COM1 to COM16	16	Common outputs COM9 to COM16 : non-select for 1/8 duty COM12 to COM16: non-select for 1/11 duty	
SEG1 to SEG40	40	Segment outputs	
V1 to V5	5	LCD driving power (V5≥V_{SS})	
V_{DD}	1	+5V	
V_{SS}	1	0V (GND)	
OSC1 OSC2	2	Used to connect resistor (typ. 91KΩ) for oscillation; OSC1 is for external clock input.	

∗1

RS	R/W	E	Operation
0	0	⎍	Instruction write cycle
0	1	1	Busy flag read cycle Address counter read cycle
1	0	⎍	DD RAM or CG RAM data write cycle
1	1	1	DD RAM or CG RAM data read cycle

■ ELECTRICAL CHARACTERISTICS

● Absolute Maximum Ratings

(V_{SS} = 0V, T_a = 25°C)

Parameter	Symbol	Rating	Unit
Supply voltage (1)	V_{DD}	–0.3 to 7.0	V
Supply voltage (2)	V1 to V5	–0.3 to V_{DD}+0.3	V
Input voltage	V_I	–0.3 to V_{DD}+0.3	V
Output voltage	V_O	–0.3 to V_{DD}+0.3	V
Power dissipation	P_D	300	mW
Operating temperature	T_{opr}	–20 to 75	°C
Storage temperature	T_{stg}	–65 to 150	°C
Soldering temperature and time	T_{sol}	260°C•10s (at lead)	—

Note: The following condition must always hold true: $V_{DD} \geq V1 \geq V2 \geq V3 \geq V4 \geq V5$

- **DC Characteristics**

(V_{DD} = 5.0V ±10%, V_{SS} = 0V, T_a = –20 to 75°C)

Parameter	Symbol	Condition	Applicable Pin	Min	Typ	Max	Unit
"H" level input voltage (1)	V_{IH1}		DB0~DB7	2.0	—	V_{DD}	V
"L" level input voltage (1)	V_{IL1}		RS, R/W, E	V_{SS}	—	0.8	V
"H" level input voltage (2)	V_{IH2}		OSC1	V_{DD}–1.0	—	V_{DD}	V
"L" level input voltage (2)	V_{IL2}			V_{SS}	—	1.0	V
"H" level output voltage (1)	V_{OH1}	I_{OH}=–0.205mA	DB0~DB7	2.4	—	—	V
"L" level output voltage (1)	V_{OL1}	I_{OL}=1.6mA		—	—	0.4	V
"H" level output voltage (2)	V_{OH2}	I_{OH}=–0.04mA	XSCL LP D0	0.9V_{DD}	—	—	V
"L" level output voltage (2)	V_{OL2}	I_{OL}=0.04mA		—	—	0.1V_{DD}	V
Driver-on resistor (COM)	R_{COM}	|V_{COM}–V_n|=0.5V	COM1~16	—	2	10	kΩ
Driver-on resistor (SEG)	R_{SEG}	|V_{SEG}–V_n|=0.5V	SEG1~40	—	2.5	10	kΩ
I/O leakage current	I_{IL}	V_I=0 to V_{DD}		—	—	1	µA
Pull-up MOS current	$-I_P$	V_{DD}=5V		50	125	250	µA
Supply current	I_{op}	Rf oscillation, from external clock V_{DD}=5V, f_{OSC}=f_{CP}=270kHz	V_{DD}	—	0.5	0.8	mA
External clock operation							
External clock operating frequency	f_{EXTCL}			125	250	350	kHz
External clock duty	Duty			45	50	55	%
External clock rise time	tr_{EXTCL}			—	—	0.2	µs
External clock fall time	tf_{EXTCL}			—	—	0.2	µs
Internal clock operation (Rf oscillation)							
Oscillation frequency	f_{OSC}	R_f=91kΩ±2%		190	270	350	kHz
Internal clock operation (Ceramic filter oscillation)							
Oscillation frequency	f_{OSC}	Ceramic filter		245	250	255	kHz
LCD driving voltage	V_{LCD}	V_{DD}–V5		3.0	—	V_{DD}	V

- **AC Characteristics**
  - **Read cycle**

(V_{DD} = 5.0V ± 10%, V_{SS} = 0V, T_a = –20 to 75°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}		500	—	—	ns
Enable "H" level pulse width	t_{WEH}		220	—	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	—	ns
Read data output delay	t_{RD}	C_L=100pF	—	—	120	ns
Read data hold time	t_{DHR}		20	—	—	ns

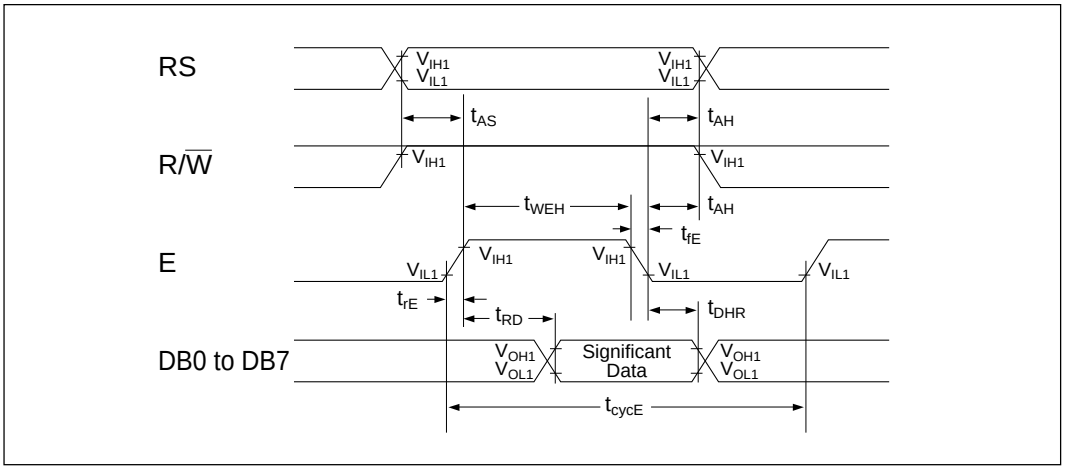
○ **Write cycle**

(V_{DD} = 5.0V±10%, V_{SS} = 0V, T_a = –20 to 75°C)

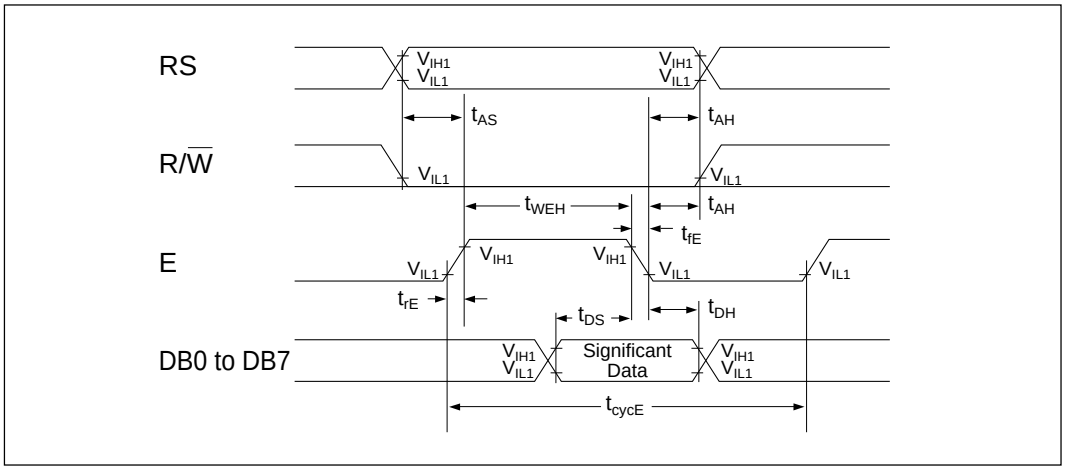
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Enable cycle time	t_{cycE}		500	—	—	ns
Enable "H" level pulse width	t_{WEH}		220	—	—	ns
Enable rise/fall time	t_{rE}, t_{fE}		—	—	25	ns
RS, R/$\overline{W}$ setup time	t_{AS}		40	—	—	ns
RS, R/$\overline{W}$ address hold time	t_{AH}		10	—	—	ns
Data setup time	t_{DS}		60	—	—	ns
Write data hold time	t_{DH}		10	—	—	ns

● **Timing Chart**

○ **Read cycle**



○ **Write cycle**

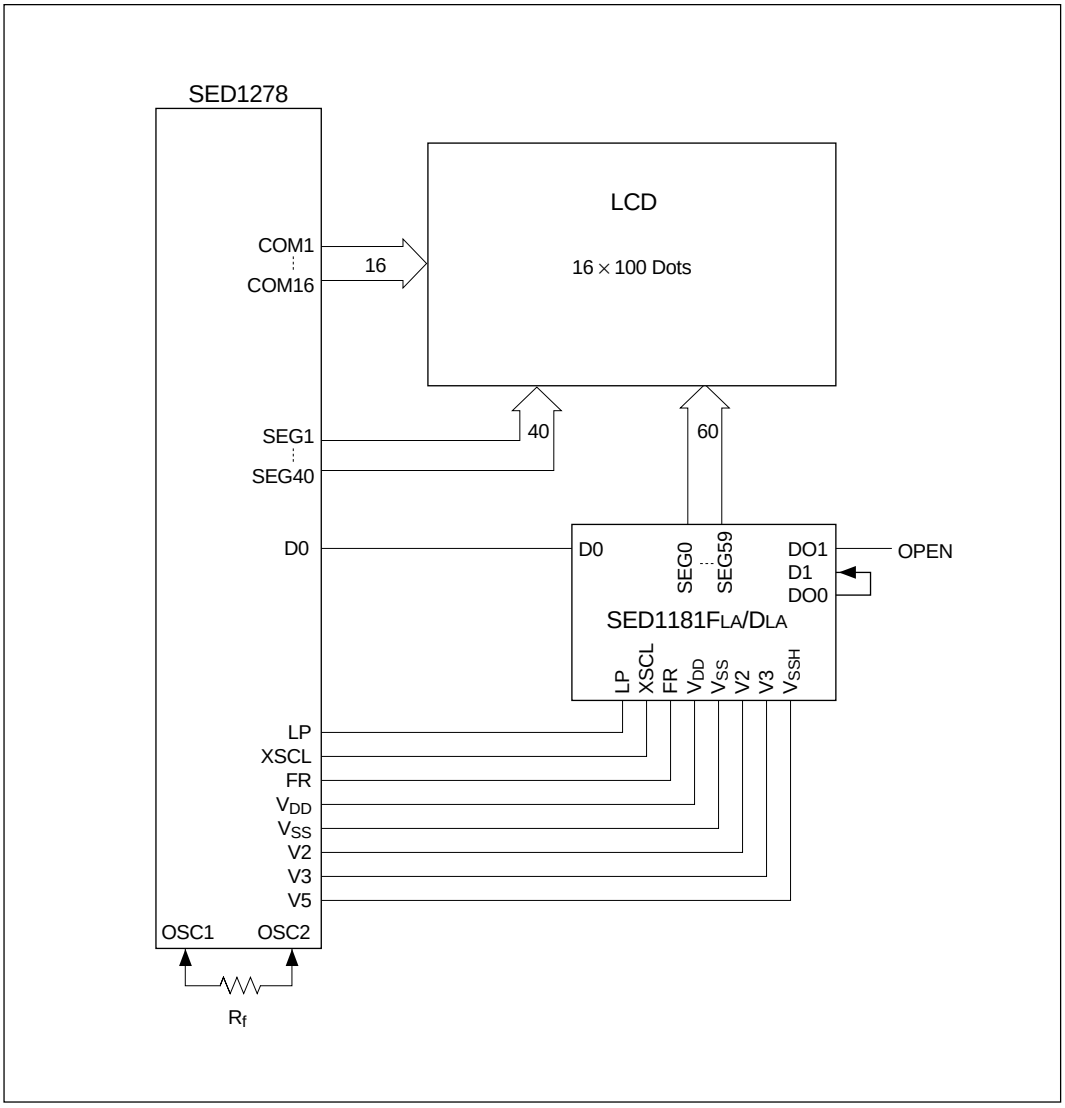


■ **DISPLAY COMMAND**

Parameter	RS	R/$\overline{W}$	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Note
CLEAR DISPLAY	0	0	0	0	0	0	0	0	0	1	
CURSOR HOME	0	0	0	0	0	0	0	0	1	*	
ENTRY MODE SET	0	0	0	0	0	0	0	1	I/D	S	DB1=1 : Increment, DB1=0 : Decrement DB0=1 : The display is shifted. DB0=0 : The display is not shifted.
DISPLAY ON/OFF	0	0	0	0	0	0	1	D	C	B	DB2=1 : Display on DB2=0 : Display off DB1=1 : Cursor on DB1=0 : Cursor off DB0=1 : Brinking on DB0=0 : Brinking off
CURSOR/DISPLAY SHIFT	0	0	0	0	0	1	S/C	R/L	*	*	DB3=1 : Shifts display one character DB2=1 : Right shift, DB2=0 : Left shift
SYSTEM SET	0	0	0	0	1	DL	N	F	*	*	DB4=1 : 8 bits, DB4=0 : 4 bits DB3=1 : 2 lines display (1/16 duty), DB3=0 : 1 line display (DB2=1 : 5x10 dots, 1/11 duty DB2=0 : 5x7dots, 1/8 duty)
SET CGRAM ADDRESS	0	0	0	1	ACG						The address length that can be set is 64 addresses.
SET DDRAM ADDRESS	0	0	1	ADD							The address length that can be set is 80 addresses.
READ BUSY FLAG/ ADDRESS COUNTER	0	1	BF	AC							DB7=1 : Busy (instruction not accepted) DB7=0 : Ready (instruction accepted)
WRITE DATA	1	0	Write Data								
READ DATA	1	1	Read Data								

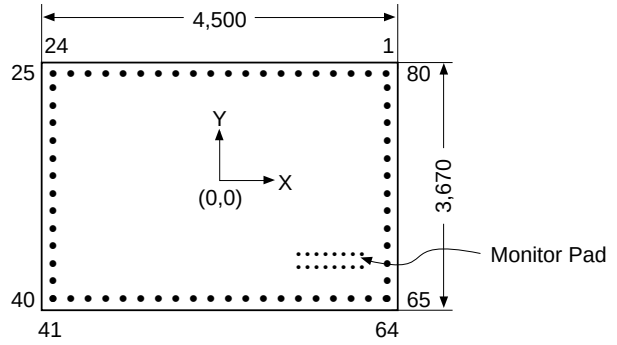
* Don't care

■ **EXAMPLE OF APPLICATION (2 lines × 20 characters)**



SED1278 is usually connected to 8-bit MPU via I/O ports.

■ **PAD LAYOUT**

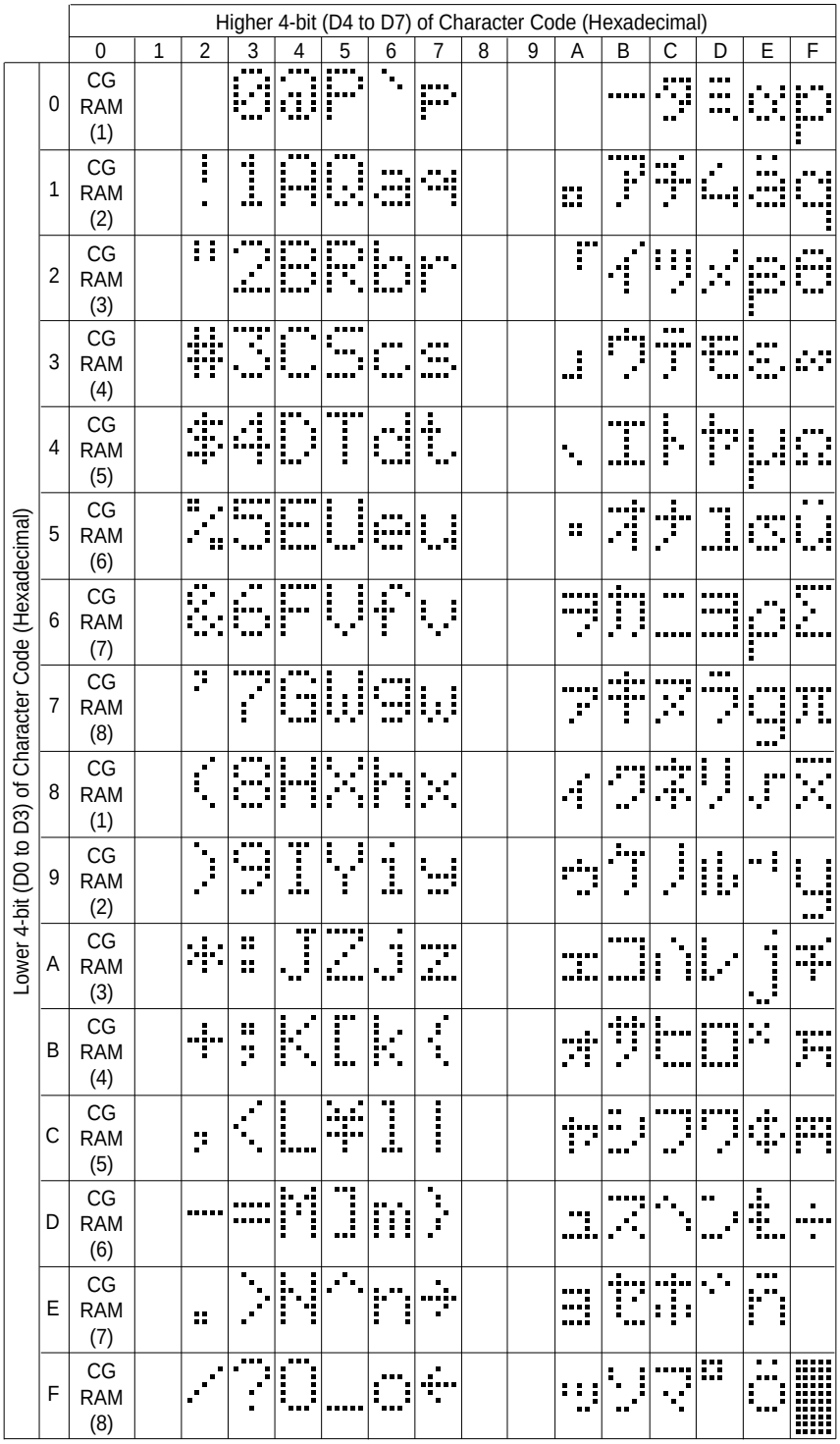


Pad size: 109 × 109

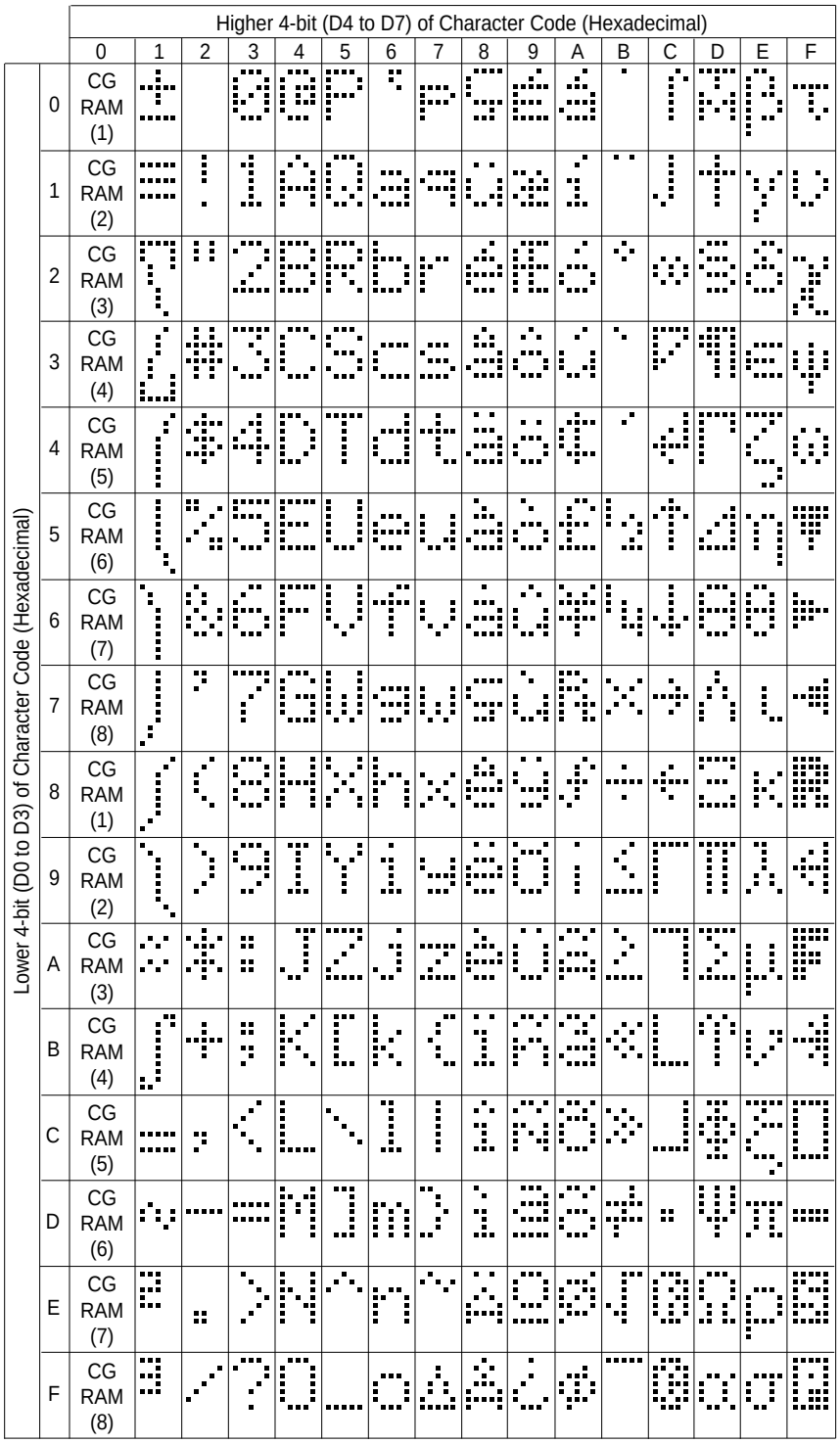
● **PAD COORDINATES**

Pad No.	Pad Name	X	Y	Pad No.	Pad Name	X	Y
1	SEG22	2087	1671	41	DB2	–2087	–1671
2	SEG21	1905	1671	42	DB3	–1905	–1671
3	SEG20	1723	1671	43	DB4	–1723	–1671
4	SEG19	1541	1671	44	DB5	–1541	–1671
5	SEG18	1359	1671	45	DB6	–1359	–1671
6	SEG17	1177	1671	46	DB7	–1177	–1671
7	SEG16	995	1671	47	COM1	–995	–1671
8	SEG15	814	1671	48	COM2	–814	–1671
9	SEG14	633	1671	49	COM3	–633	–1671
10	SEG13	452	1671	50	COM4	–452	–1671
11	SEG12	272	1671	51	COM5	–272	–1671
12	SEG11	91	1671	52	COM6	–91	–1671
13	SEG10	–91	1671	53	COM7	91	–1671
14	SEG9	–272	1671	54	COM8	272	–1671
15	SEG8	–452	1671	55	COM9	452	–1671
16	SEG7	–633	1671	56	COM10	633	–1671
17	SEG6	–814	1671	57	COM11	814	–1671
18	SEG5	–995	1671	58	COM12	995	–1671
19	SEG4	–1177	1671	59	COM13	1177	–1671
20	SEG3	–1359	1671	60	COM14	1359	–1671
21	SEG2	–1541	1671	61	COM15	1541	–1671
22	SEG1	–1723	1671	62	COM16	1723	–1671
23	GND	–1905	1671	63	SEG40	1905	–1671
24	OSC1	–2087	1671	64	SEG39	2087	–1671
25	OSC2	–2087	1365	65	SEG38	2087	–1365
26	V1	–2087	1183	66	SEG37	2087	–1183
27	V2	–2087	1001	67	SEG36	2087	–1001
28	V3	–2087	819	68	SEG35	2087	–819
29	V4	–2087	637	69	SEG34	2087	–637
30	V5	–2087	455	70	SEG33	2087	–455
31	LP	–2087	273	71	SEG32	2087	–273
32	XSCL	–2087	91	72	SEG31	2087	–91
33	VCC	–2087	–91	73	SEG30	2087	91
34	FR	–2087	–273	74	SEG29	2087	273
35	DO	–2087	–455	75	SEG28	2087	455
36	RS	–2087	–637	76	SEG27	2087	637
37	R/W	–2087	–819	77	SEG26	2087	819
38	E	–2087	–1001	78	SEG25	2087	1001
39	DB0	–2087	–1183	79	SEG24	2087	1183
40	DB1	–2087	–1365	80	SEG23	2087	1365

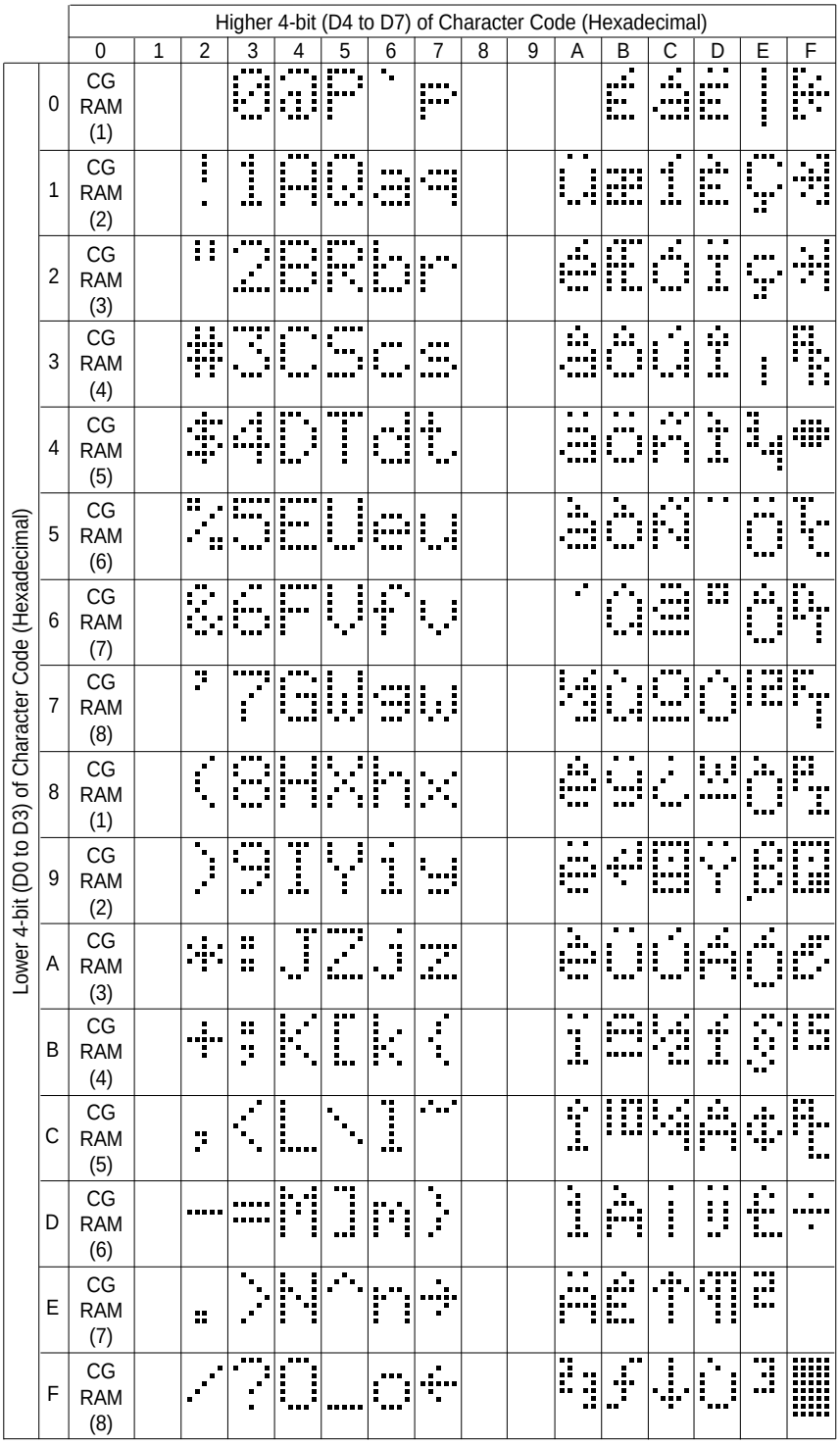
■ SED1278F0A/D0A CHARACTER FONT



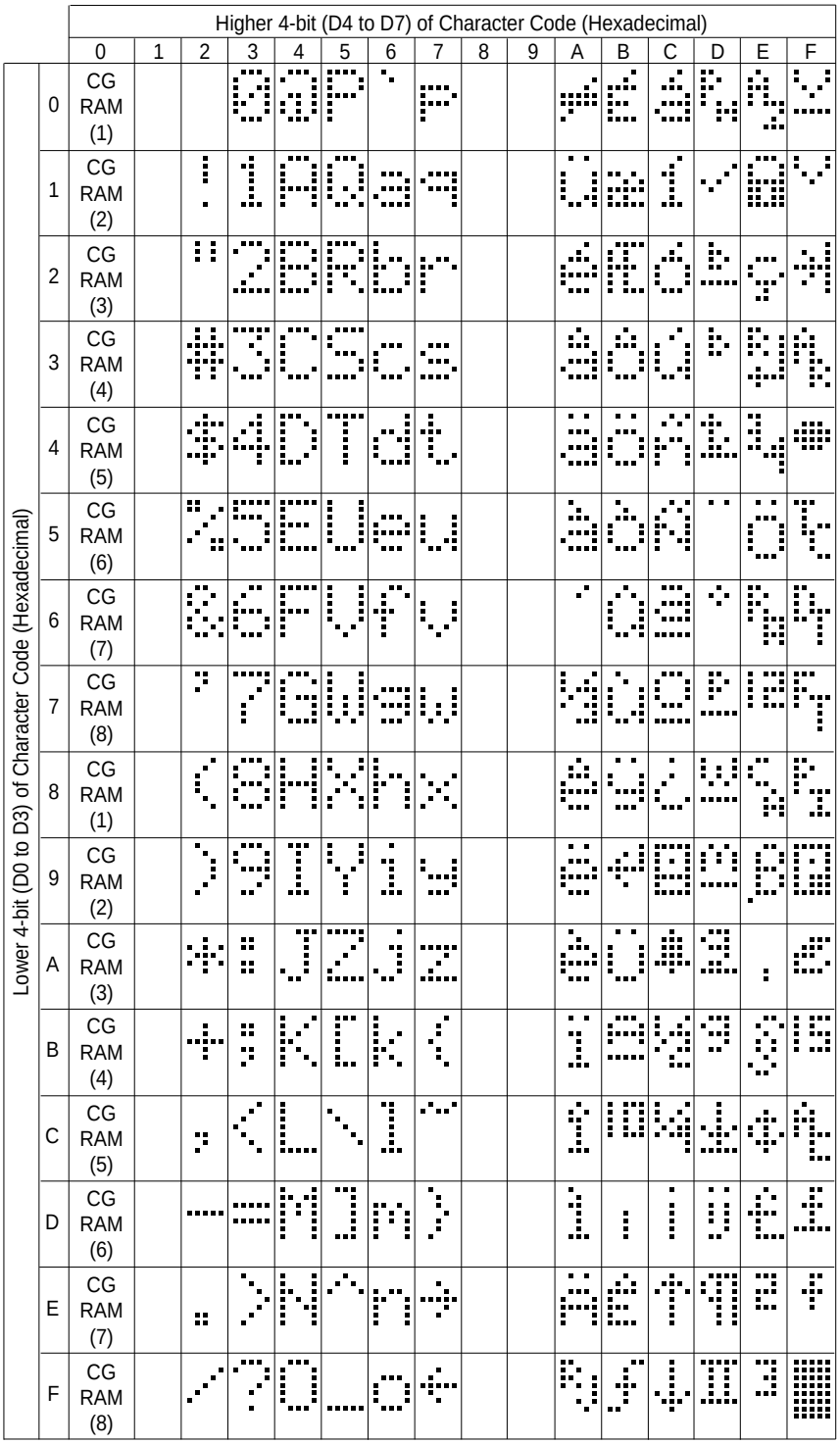
■ **SED1278F0B/D0B CHARACTER FONT**



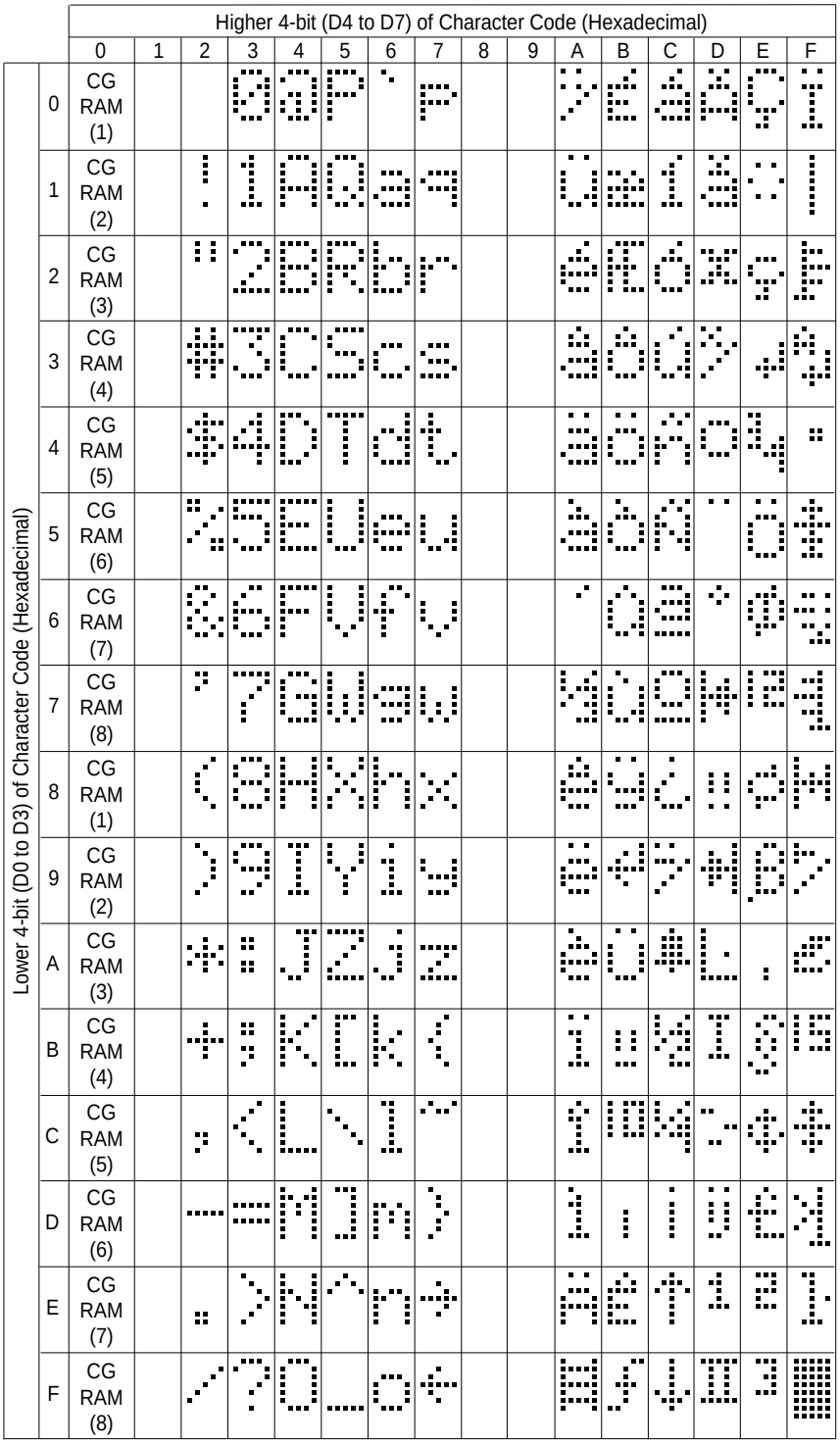
■ **SED1278F0C/D0C CHARACTER FONT**



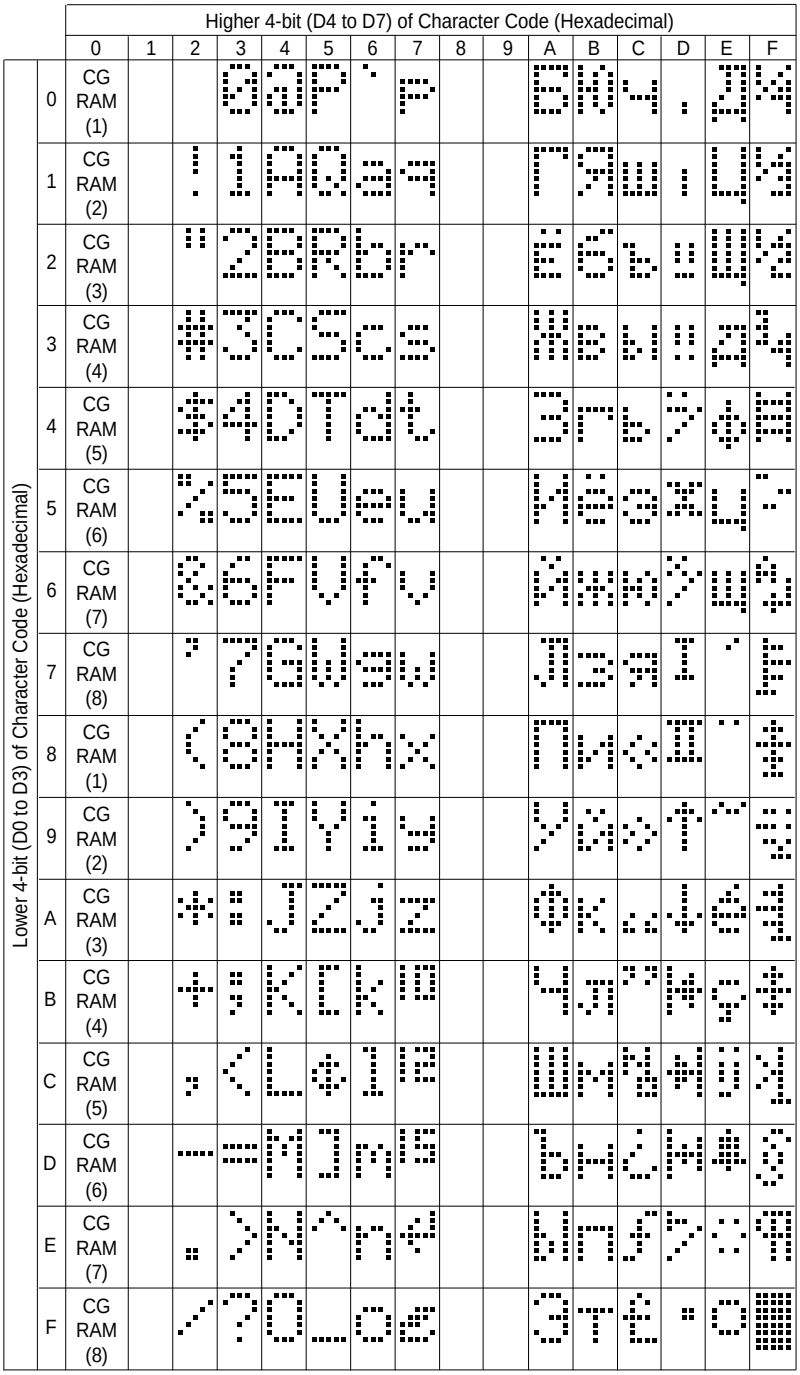
■ **SED1278F0D/D0D CHARACTER FONT**



■ **SED1278F0G/D0G CHARACTER FONT**



■ SED1278F0H/D0H CHARACTER FONT



* Character codes (00H-0FH) of SED1278F are assigned to the area of character generator RAM (CG RAM). The CG ROM of the SED1278F is masked; if you wish to have your own CG ROM, consult S-MOS Marketing Department for conversion of the masked ROM.

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