256K x 32 EDO DRAM
3.3 Volt, 66 / 83 MHz

Features

- 262,144-Word by 32-Bit organization
- Single +3.3V ± 0.3V power supply
- 512 refresh cycles / 8 ms
- Refresh modes: RAS-only, CAS-before-RAS (CBR) and Hidden
- Optional Self Refresh (S Version only)
- 4 CAS inputs for Byte Write and Read control
- Fast Page Mode with Extended Data Out (EDO)
- +5V I/O tolerance
- JEDEC standard 100-Pin LQFP package

Description

The SM81L256K32A is a high-speed randomly accessed memory organized in a 262,144-word by 32-bit configuration. This product can execute Byte Write and Read operation via four CAS pins.

The SM81L256K32A offers an accelerated Fast Page Mode cycle with a feature called Extended Data Out (EDO). This allows random access of up to 512 (x32) words within a row at an 83-MHz EDO cycle, making the SM81L256K32A ideally suited for graphics, digital signal processing and high performance computing systems. The SM81L256K32, in the LQFP package, greatly benefits low power and small factor applications such as notebooks and PDAs as well.

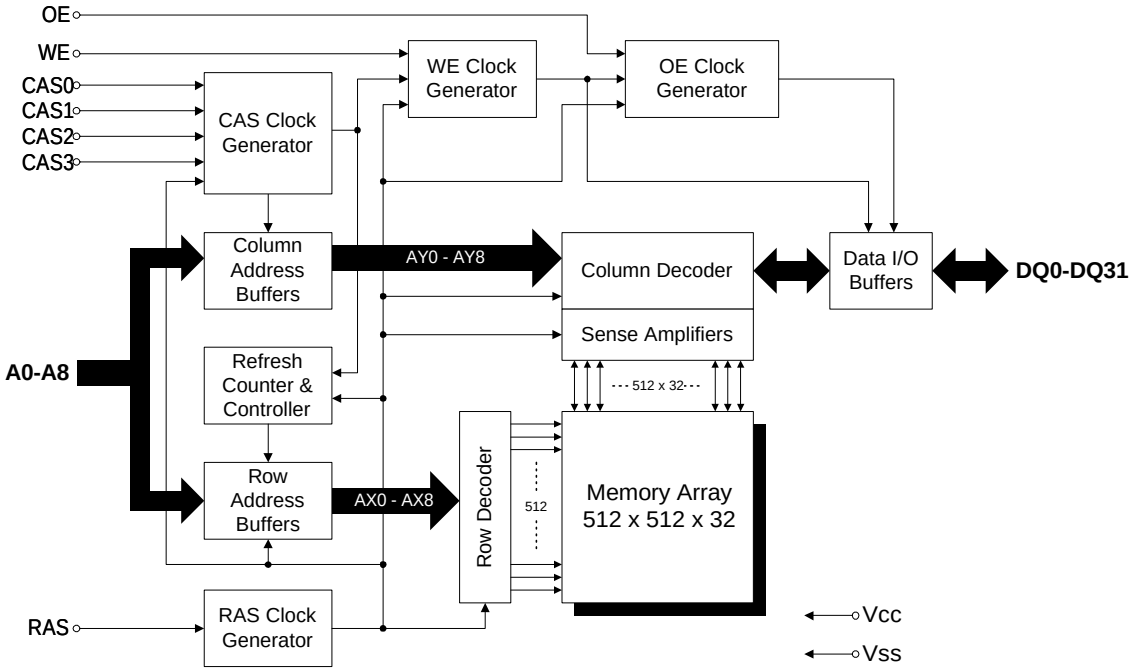
Key Timing Parameters

SM81L256K32A	-28 / -28S (83MHz)	-35 / -35S (66MHz)
Max. Access Time from RAS (t_{RAC})	28 ns	35 ns
Max. Access Time from Column Address (t_{AA})	15 ns	19 ns
Max. Access Time from CAS (t_{CAC})	9 ns	10 ns
Max. Access Time from OE (t_{OEA})	9 ns	10 ns
Min. Random Write Cycle Time (t_{RC})	48 ns	60 ns
Min. Random Read Cycle Time (t_{RC})	60 ns	75 ns
Min. EDO Cycle Time (t_{PC})	12 ns	15 ns

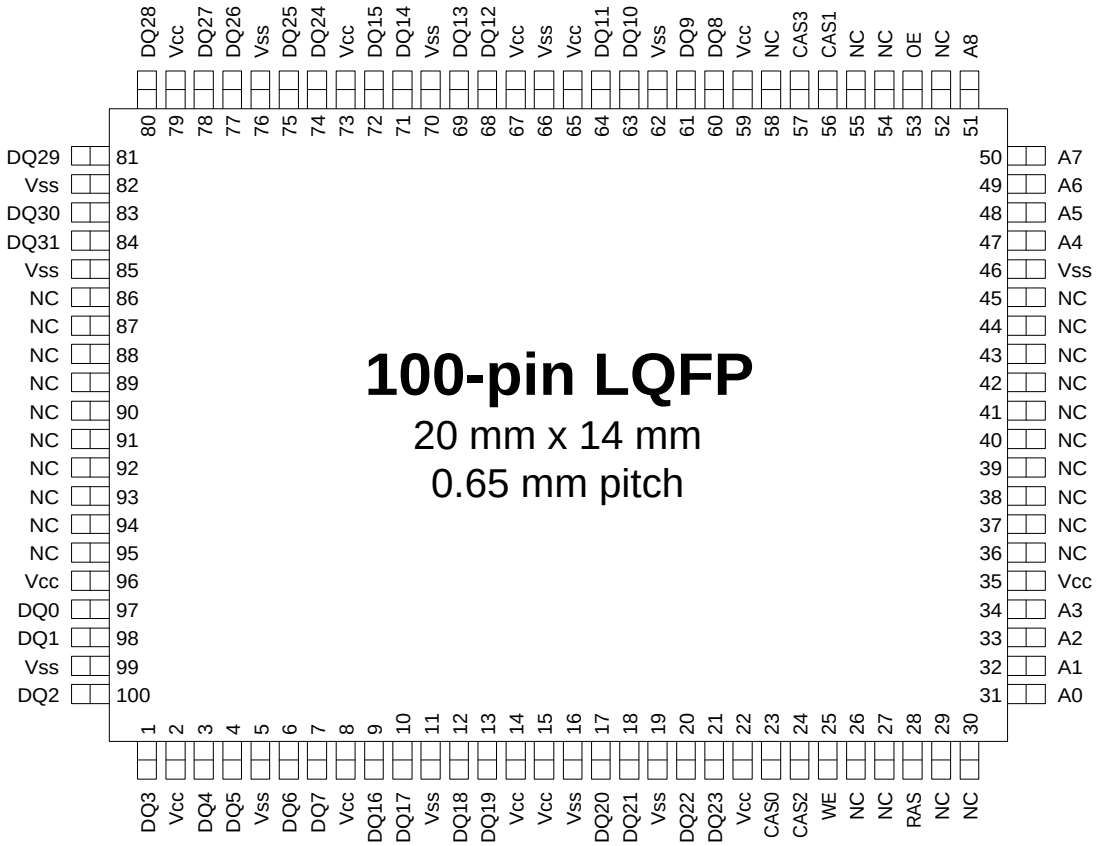
Ordering Information

Part Number	Speed Grade	Package	Optional Feature
SM81L256K32AL - 28	83 MHz	100-pin LQFP	
SM81L256K32AL - 28S	83 MHz	100-pin LQFP	Self Refresh
SM81L256K32AL - 35	66 MHz	100-pin LQFP	
SM81L256K32AL - 35S	66 MHz	100-pin LQFP	Self Refresh

Functional Block Diagram



Pin Assignment (Top View)



Pin Descriptions

Pin Name	Description
A0 - A8	Address Inputs
RAS	Row Address Strobe
CAS0	Column Address Strobe for 1st Byte (DQ0 - DQ7)
CAS1	Column Address Strobe for 2nd Byte (DQ8 - DQ15)
CAS2	Column Address Strobe for 3rd Byte (DQ16 - DQ23)
CAS3	Column Address Strobe for 4th Byte (DQ24 - DQ31)
WE	Write Enable
OE	Output Enable
DQ0 – DQ31	Data Input / Output
Vcc	+3.3V Supply
Vss	Ground
NC	No Connection: This pin should be left unconnected or tied to ground.

Functional Description

The SM81L256K32A reads and writes data by multiplexing an 18-bit address into a 9-bit row and 9-bit column address. RAS and CAS are used to strobe the row address and the column address, respectively.

The SM81L256K32A has four CAS inputs: CAS0 controls DQ0 - DQ7, CAS1 controls DQ8 - DQ15, CAS2 controls DQ16 - DQ23, and CAS3 controls DQ24 - DQ31. CAS0 – CAS3 function in an identical manner to CAS in that any will generate an internal CAS signal. The CAS function and timing are determined by the first CAS (CAS0, CAS1, CAS2 or CAS3) to transition low and by the last to transition high. Byte Read and Byte Write are controlled by using CAS0 – CAS3 separately.

A Read cycle is performed by holding the WE signal high during RAS/CAS operation. A Write cycle is executed by holding the WE signal low during RAS/CAS operation; the input data is latched by the falling edge of WE or CAS, whichever occurs later. The data inputs and outputs are routed through 32 common I/O pins, with RAS, CAS, WE and OE controlling the pin direction.

Fast Page Mode operation permits all 512 columns within a selected row to be randomly accessed at a high data rate. A Fast Page Mode cycle is initiated with a row address latched by RAS followed by a column address latched by CAS. While holding RAS low, CAS can be toggled to strobe changing column addresses, thus achieving shorter cycle times.

The SM81L256K32A offers an accelerated Fast Page Mode cycle through a feature called Extended Data Out, which keeps the output drivers on during the CAS precharge time (t_{CP}). Since data can be output after CAS goes high, the user is not required to wait for valid data to appear before starting the next access cycle. Data-out will remain valid as long as RAS and OE are low, and WE is high; this is the only characteristic which differentiates Extended Data Out operation from a standard Read or Fast Page Read.

A memory cycle is terminated by returning both RAS and CAS high. Memory cell data will retain its correct state by maintaining power and accessing all 512 combinations of the 9-bit row addresses, regardless of sequence, at least once every 8ms through any RAS cycle (Read, Write) or RAS Refresh cycle (RAS-only, CBR, Hidden and Self Refresh). The CBR Refresh cycle automatically controls the row addresses by invoking the refresh counter and controller.

Power-Up Sequence

The initial application of the Vcc supply requires a 200-µs wait followed by a minimum of any eight initialization cycles containing a RAS clock. During Power-Up, the Vcc current is dependent on the input levels of RAS and CAS. It is recommended that RAS and CAS track with Vcc or be held at a valid V_{IH} during Power-Up.

Truth Table

(X = Don't Care)

Function	RAS	CAS0	CAS1	CAS2	CAS3	WE	OE	Address	DQ0 – DQ31	Notes
Standby	H	H	H	H	H	X	X	X	High-Z	
Read: Double Word	L	L	L	L	L	H	L	Row/Col.	Data Out	
Read: 1st Byte	L	L	H	H	H	H	L	Row/Col.	DQ0-7 = Data Out DQ8-31 = High-Z	
Read: 2nd Byte	L	H	L	H	H	H	L	Row/Col.	DQ0-7 = High-Z DQ8-15 = Data Out DQ16-31 = High-Z	
Read: 3rd Byte	L	H	H	L	H	H	L	Row/Col.	DQ0-15 = High-Z DQ16-23 = Data Out DQ24-31 = High-Z	
Read: 4th Byte	L	H	H	H	L	H	L	Row/Col.	DQ0-23 = High-Z DQ24-31 = Data Out	
Write: Double Word (Early)	L	L	L	L	L	L	X	Row/Col.	Data In	
Write: 1st Byte (Early)	L	L	H	H	H	L	X	Row/Col.	DQ0-7 = Data In DQ8-31 = X	
Write: 2nd Byte (Early)	L	H	L	H	H	L	X	Row/Col.	DQ0-7 = X DQ8-15 = Data In DQ16-31 = X	
Write: 3rd Byte (Early)	L	H	H	L	H	L	X	Row/Col.	DQ0-15 = X DQ16-23 = Data In DQ24-31 = X	
Write: 4th Byte (Early)	L	H	H	H	L	L	X	Row/Col.	DQ0-23 = X DQ24-31 = Data In	
Read-Write	L	L	L	L	L	H→L	L→H	Row/Col.	Data Out → Data In	1, 2
Fast-Page-Mode Read: EDO										
- First cycle	L	H→L	H→L	H→L	H→L	H	L	Row/Col.	Data Out	2
- Subsequent cycles	L	H→L	H→L	H→L	H→L	H	L	Col.	Data Out	2
Fast-Page-Mode Read: Hi-Z										
- First cycle	L	H→L	H→L	H→L	H→L	H	H→L	Row/Col.	Data Out	2
- Subsequent cycles	L	H→L	H→L	H→L	H→L	H	H→L	Col.	Data Out	2
Fast-Page-Mode Write (Early)										
- First cycle	L	H→L	H→L	H→L	H→L	L	X	Row/Col.	Data In	1
- Subsequent cycles	L	H→L	H→L	H→L	H→L	L	X	Col.	Data In	1
Fast-Page-Mode Read-Write										
- First cycle	L	H→L	H→L	H→L	H→L	H→L	L→H	Row/Col.	Data Out → Data In	1, 2
- Subsequent cycles	L	H→L	H→L	H→L	H→L	H→L	L→H	Col.	Data Out → Data In	1, 2
Hidden Refresh Read	L→H→L	L	L	L	L	H	L	Row/Col.	Data Out	2
Hidden Refresh Write	L→H→L	L	L	L	L	L	X	Row/Col.	Data In → High-Z	1
RAS-Only Refresh	L	H	H	H	H	X	X	Row	High-Z	
CBR Refresh	H→L	L	L	L	L	X	X	X	High-Z	3

Note: 1. Byte Write may be executed with CAS0, CAS1, CAS2 or CAS3 active.
2. Byte Read may be executed with CAS0, CAS1, CAS2 or CAS3 active.
3. Only one CAS signal (CAS0, CAS1, CAS2 or CAS3) must be active.

Electrical Characteristics

*Absolute Maximum Ratings**

Ambient Temperature Under Bias..... -1.0 °C to +80 °C
Storage Temperature ..... -50 °C to 125 °C
Voltage Relative to Vss .....-1.0 V to +7.0 V **
Data Output Current..... 50 mA
Power Dissipation..... 1.0 W

* Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

** Note : Guaranteed +5.0V I/O tolerance

Recommended Operating Conditions

(T_A = 0 °C to 70 °C)

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Power Supply	Vcc	3.0	3.3	3.6	V	1
Input High Voltage (+5.0V I/O Tolerance)	V_{IH}	2.4	—	Vcc + 0.5	V	1
Input Low Voltage	V_{IL}	-0.5	—	0.4	V	1

*Capacitance**

(Vcc = 3.3V, T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Maximum	Unit
Input Capacitance (A0-A8, RAS, CAS, WE,OE)	C_{IN}	5	pF
Input/Output Capacitance (DQ0-DQ31)	C_{IO}	7	pF

* Note: Capacitance is sampled and not 100% tested.

DC Characteristics

(Note: 1, Vcc = 3.3V ± 0.3V, T_A = 0°C – 70°C)

Parameter	Symbol	Condition	- 28		- 35		Unit	Notes
			Min.	Max.	Min.	Max.		
Input High (Logic 1) Voltage, all inputs Note : +5.0V I/O Tolerance	V_{IH}		2.0	Vcc+0.5	2.0	Vcc+0.5	V	
Input Low (Logic 0) Voltage, all inputs	V_{IL}		-0.5	0.8	-0.5	0.8	V	
Output High Voltage	V_{OH}	I_{OH} = -2mA	2.4	Vcc	2.4	Vcc	V	
Output Low Voltage	V_{OL}	I_{OL} = 2mA	0	0.4	0	0.4	V	
Input Leakage Current	I_{LI}	0V ≤ V_{IN} ≤ Vcc	-10	10	-10	10	µA	
Output Leakage Current	I_{LO}	0V ≤ V_{OUT} ≤ 3.6V; outputs disabled	-10	10	-10	10	µA	
Average Power Supply Current (Operating)	I_{CC1}	RAS, CAS = cycling; t_{RC} = Min.	-	260	-	200	mA	2, 3, 15, 16
Power Supply Current (Standby)	I_{CC2}	RAS, CAS = V_{IH}	-	2	-	2	mA	
Power Supply Current (CMOS Standby) Note : For S Version only	I_{CC3}	RAS, CAS = Vcc - 0.2 V	-	300	-	300	µA	20
Average Power Supply Current (Self Refresh) Note : For S Version only	I_{CC4}	CBR Cycle with RAS > $t_{RASS(min.)}$, CAS= V_{IL}	-	500	-	500	µA	20
Average Power Supply Current (Fast Page Mode)	I_{CC5}	RAS = V_{IL}; CAS = cycling; t_{PC} = Min.	-	240	-	180	mA	2, 3, 15, 18

AC Characteristics

(Vcc = 3.3V ± 0.3V, T_A = 0°C – 70°C)

Parameter	Symbol	-28		-35		Unit	Notes
		Min.	Max.	Min.	Max.		
Random Read Cycle Time	t_{RC}	60		75		ns	
Random Write Cycle Time	t_{RC}	48		60		ns	
Read Modify Write Cycle Time	t_{RMW}	75		85		ns	
EDO Cycle Time	t_{PC}	12		15		ns	
Fast Page Mode Read-Modify-Write Cycle Time	t_{PRMW}	34		40		ns	
Access Time from RAS	t_{RAC}		28		35	ns	7, 10, 12, 13
Access Time from Column Address	t_{AA}		15		19	ns	7, 13
Access Time from CAS	t_{CAC}		9		10	ns	7, 12
Access Time from CAS Precharge	t_{CPA}		17		21	ns	7, 12
Output Buffer Turn-Off Delay Time from RAS	t_{REZ}	3	7	3	8	ns	8
Output Buffer Turn-Off Delay Time from CAS	t_{CEZ}	3	7	3	8	ns	8
Transition Time (Rise and Fall)	t_T	0.5	35	1	35	ns	6
RAS Precharge Time	t_{RP}	17		20		ns	
RAS Pulse Width	t_{RAS}	32	10K	35	10K	ns	
RAS Pulse Width (Fast Page Mode Only)	t_{RASP}	32	100K	35	100K	ns	
RAS Hold Time	t_{RSH}	7		8		ns	
CAS Hold Time	t_{CSH}	22		27		ns	
CAS Pulse Width	t_{CAS}	5	10k	6	10k	ns	
RAS to CAS Delay Time	t_{RCD}	10	23	11	25	ns	12
RAS to Column Address Delay Time	t_{RAD}	8	17	9	19	ns	13
Column Address to RAS Lead Time	t_{RAL}	15		19		ns	
CAS to RAS Precharge Time	t_{CRP}	5		5		ns	
CAS Precharge Time (Fast Page Mode)	t_{CP}	5		5		ns	
Row Address Set-Up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	6		7		ns	
Column Address Set-Up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	5		6		ns	
Column Address Hold Time referenced to RAS	t_{AR}	21		25		ns	
Read Command Set-Up Time	t_{RCS}	0		0		ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0		0		ns	9
Read Command Hold Time referenced to RAS	t_{RRH}	0		0		ns	9
CAS "H" to RAS "H" Lead Time	t_{CRL}	0		0		ns	
RAS "H" to CAS "H" Lead Time	t_{RCL}	0		0		ns	
Data Output Hold after CAS low	t_{DOH}	3		3		ns	17

AC Characteristics (continued)

(Vcc = 3.3V ± 0.3V, T_A = 0°C – 70°C)

Parameter	Symbol	-28		-35		Unit	Notes
		Min.	Max.	Min.	Max.		
Write Command Set-Up Time	t_{WCS}	0		0		ns	11
Write Command Hold Time	t_{WCH}	5		6		ns	
Write Command Hold Time referenced to RAS	t_{WCR}	21		25		ns	
Write Command Pulse Width	t_{WP}	5		6		ns	
Write Command to RAS Lead Time	t_{RWL}	7		8		ns	
Write Command to CAS Lead Time	t_{CWL}	5		6		ns	
Output Buffer Turn-Off Delay Time from WE	t_{WEZ}	3	10	3	12	ns	8
Data Set-Up Time	t_{DS}	0		0		ns	19
Data Hold Time	t_{DH}	5		6		ns	19
Data Hold Time referenced to RAS	t_{DHR}	21		25		ns	
RAS to WE Delay Time	t_{RWD}	41		48		ns	11
Column Address to WE Delay Time	t_{AWD}	24		29		ns	11
CAS to WE Delay Time	t_{CWD}	18		20		ns	11
Access Time from OE	t_{OEA}		9		10	ns	
Output Buffer Turn-Off Delay Time from OE	t_{OEZ}	3	7	3	8	ns	8
OE to Data Delay Time	t_{OED}	7		8		ns	
OE Command Hold Time	t_{OEH}	5		5		ns	
RAS Hold Time referenced to OE	t_{ROH}	7		8		ns	
OE "L" to CAS "H" Lead Time	t_{OCH}	5		8		ns	
CAS "H" to OE "L" Lead Time	t_{CHO}	5		8		ns	
Hi-Z Command Pulse Width	t_{OEP}	5		8		ns	
CAS Set-Up Time for CAS-before-RAS Cycle	t_{CSR}	5		8		ns	
CAS Hold Time for CAS-before-RAS Cycle	t_{CHR}	7		8		ns	
RAS Precharge to CAS Active Time	t_{RPC}	0		0		ns	
Refresh Period	t_{REF}		8		8	ms	20

DC/AC Characteristics for Optional Self Refresh (S Version only)

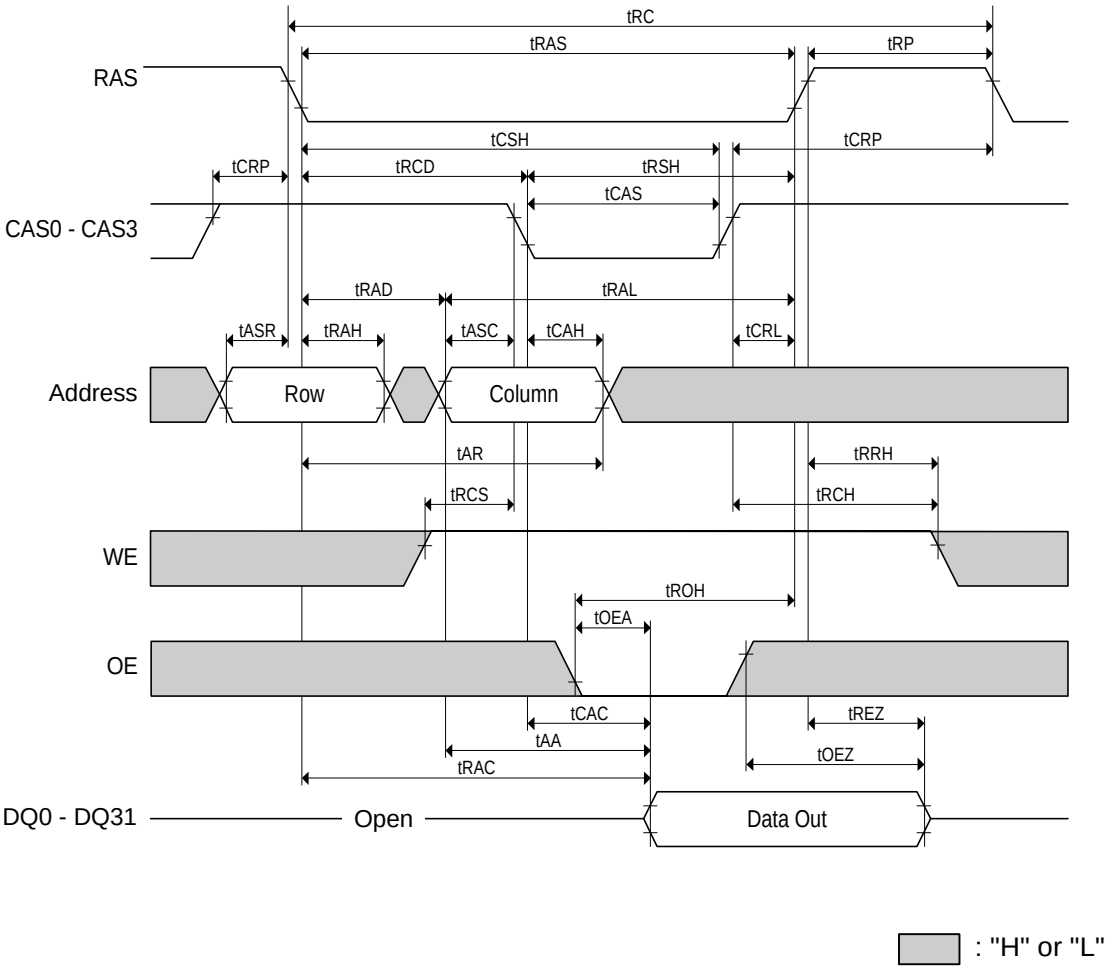
(Vcc = 3.3V ± 0.3V, T_A = 0°C – 70°C)

Parameter	Symbol	-28		-35		Unit	Notes
		Min.	Max.	Min.	Max.		
Average Self Refresh Power Supply Current	I_{CC4}	-	500	-	500	µA	20
RAS Pulse Width during Self-Refresh Cycle	t_{RASS}	100		100		us	20
CAS "L" to "don't care" during Self-Refresh Cycle	t_{CHD}	600		600		us	20
RAS Precharge Time during Self-Refresh Cycle	t_{RPS}	60		75		ns	20
Refresh Period	t_{REF}		8		8	ms	20

Notes

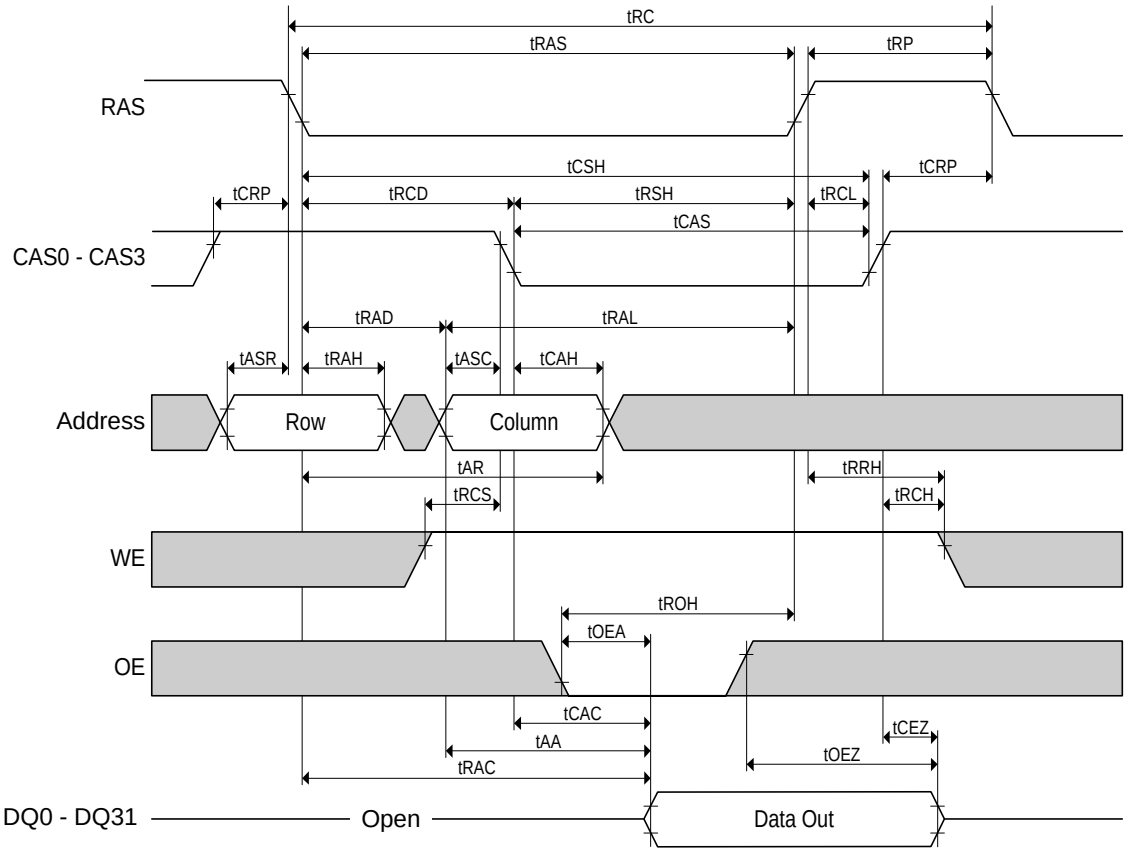
1. All voltages are referenced to Vss.
2. This parameter is dependent upon the cycle rate.
3. This parameter is dependent upon the output loading. Specified values are obtained with the output open.
4. An initial pause of 200µs is required after power-up followed by any eight RAS cycles (example: RAS-only-refresh) before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight CAS-before-RAS cycles instead of eight RAS cycles are required.
5. The AC characteristics assume at t_T = 1.5ns.
6. $V_{IH(min.)}$ and $V_{IL\ (max.)}$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
7. Data outputs are measured with a load of 50pF. DOUT reference levels: V_{OH}/V_{OL} = 2.0V/0.8V.
8. $t_{REZ(max.)}$, $t_{CEZ(max.)}$, $t_{WEZ(max.)}$, and $t_{OEZ(max.)}$ define the time at which the outputs achieve the open circuit condition and are not referenced to output voltage levels. This parameter is sampled and not 100% tested.
9. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
10. This parameter is guaranteed under nominal operating conditions.
11. t_{WCS}, t_{RWD}, t_{CWD}, and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS(min.)}$, the cycle is an early Write cycle, and the data out pins will remain tri-state throughout the entire cycle. If $t_{RWD} \geq t_{RWD(min.)}$, $t_{CWD} \geq t_{CWD(min.)}$, and $t_{AWD} \geq t_{AWD(min.)}$, the cycle is a Read-Modify-Write cycle, and the output data will contain data read from the addressed memory cells. If neither of the above sets of conditions is satisfied, the condition of the output data is indeterminate.
12. Operation within the $t_{RCD(max.)}$ limit insures that $t_{RAC(max.)}$ can be met. $t_{RCD(max.)}$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD(max.)}$ limit, then access time is controlled by t_{CAC}.
13. Operation within the $t_{RAD(max.)}$ limit ensures that $t_{RAC(max.)}$ can be met. $t_{RAD(max.)}$ is specified as a reference point only: if t_{RAD} is greater than the specified $t_{RAD(max.)}$ limit, then access time is controlled by t_{AA}.
14. Input levels at the AC testing are 2.4V/0V.
15. Addresses (A0-A8) may be changed at most two times while RAS = V_{IL}.
16. Addresses (A0-A8) may be changed at most once while CAS = V_{IH} and RAS = V_{IL}.
17. This is guaranteed by design. ($t_{DOH} = t_{CAC}$ – output transition time). This parameter is not 100% tested.
18. This parameter is dependent upon the number of address transitions. Specified values are measured with a maximum of two transitions per address cycle in Fast Page Mode.
19. These parameters are referenced to CAS leading edge of early Write cycles and to WE leading edge in OE-controlled Write cycles and Read-Modify-Write cycles.
20. This feature is guaranteed for S Version parts (SM81L256K32AL-28S and SM81L256K32AL-35S) only.

Read Cycle (Outputs Controlled by RAS)



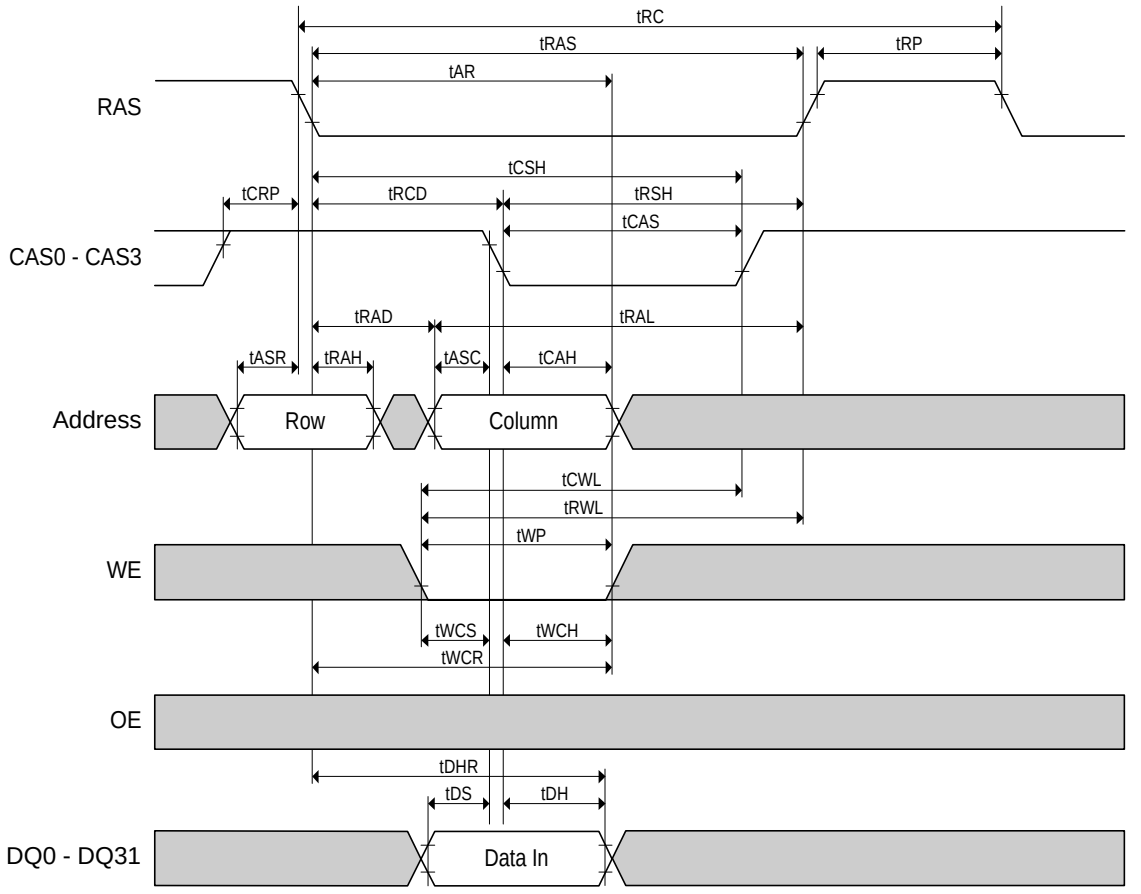
: "H" or "L"

Read Cycle (Outputs Controlled by CAS)



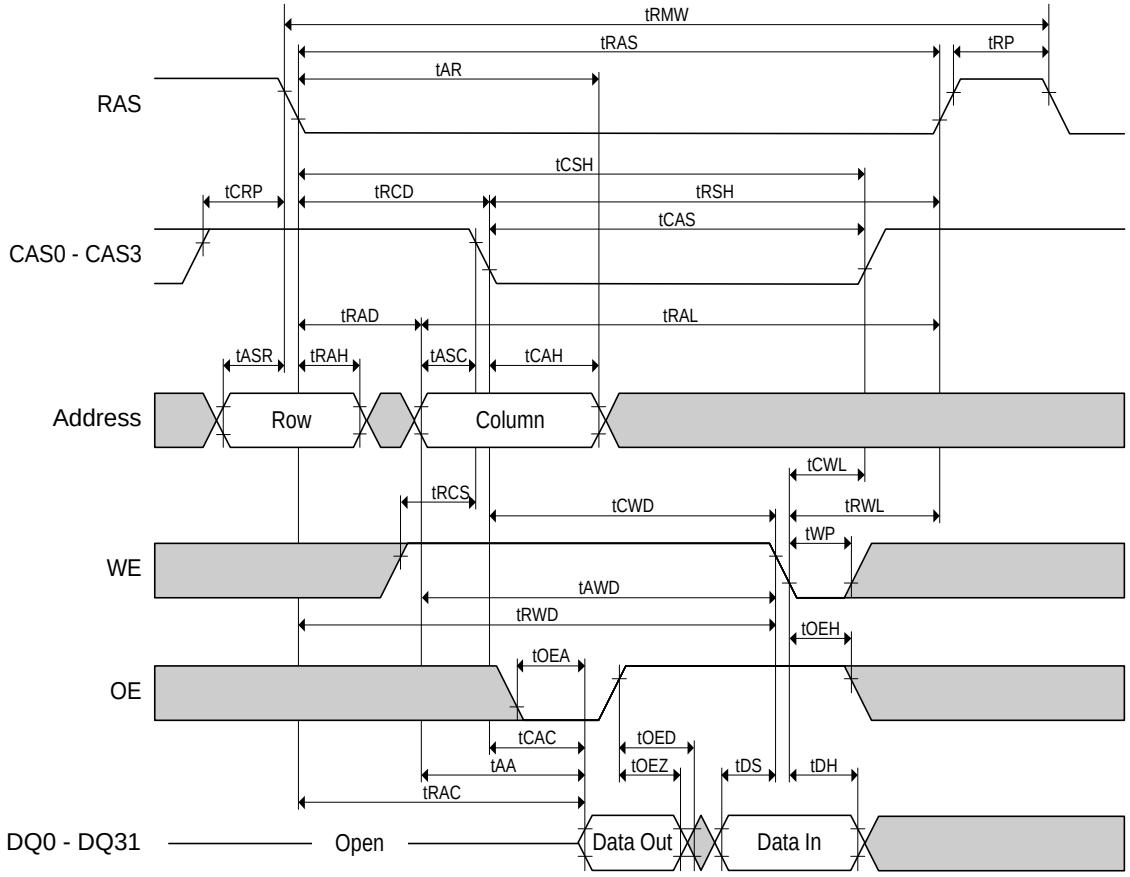
: "H" or "L"

Write Cycle (Early Write)



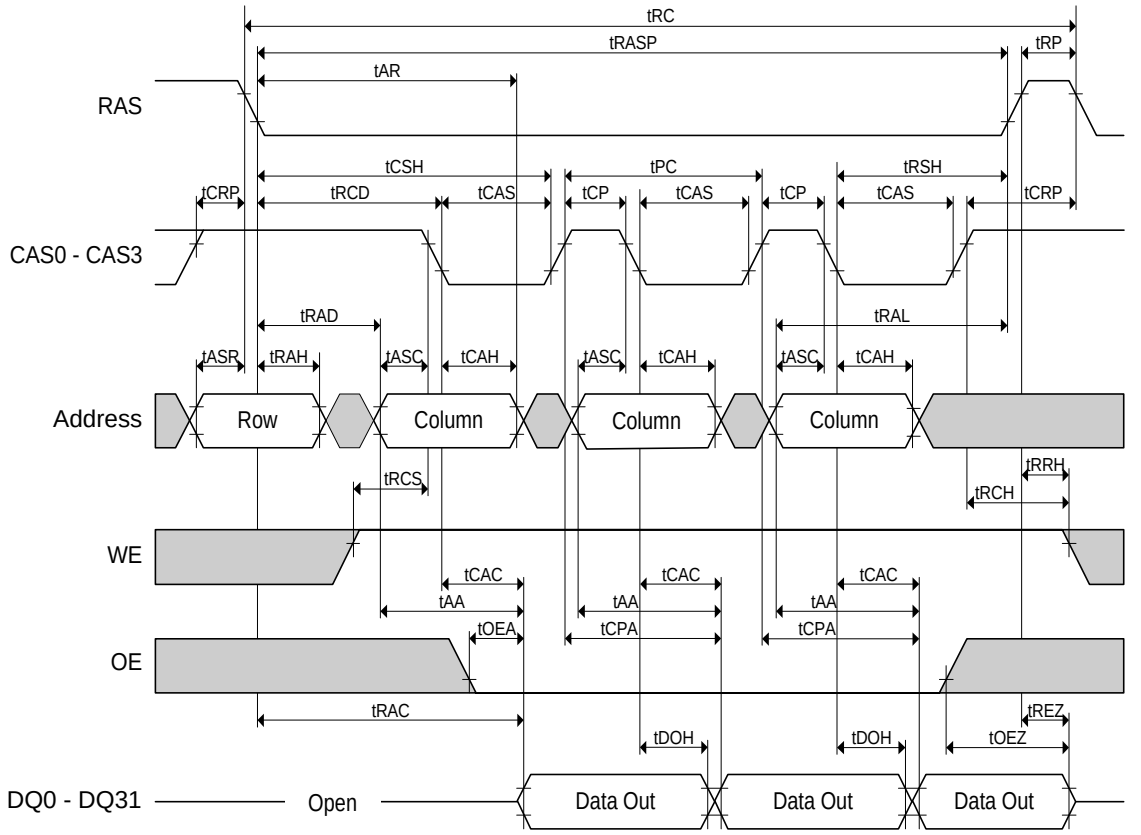
: "H" or "L"

Read-Modify-Write Cycle



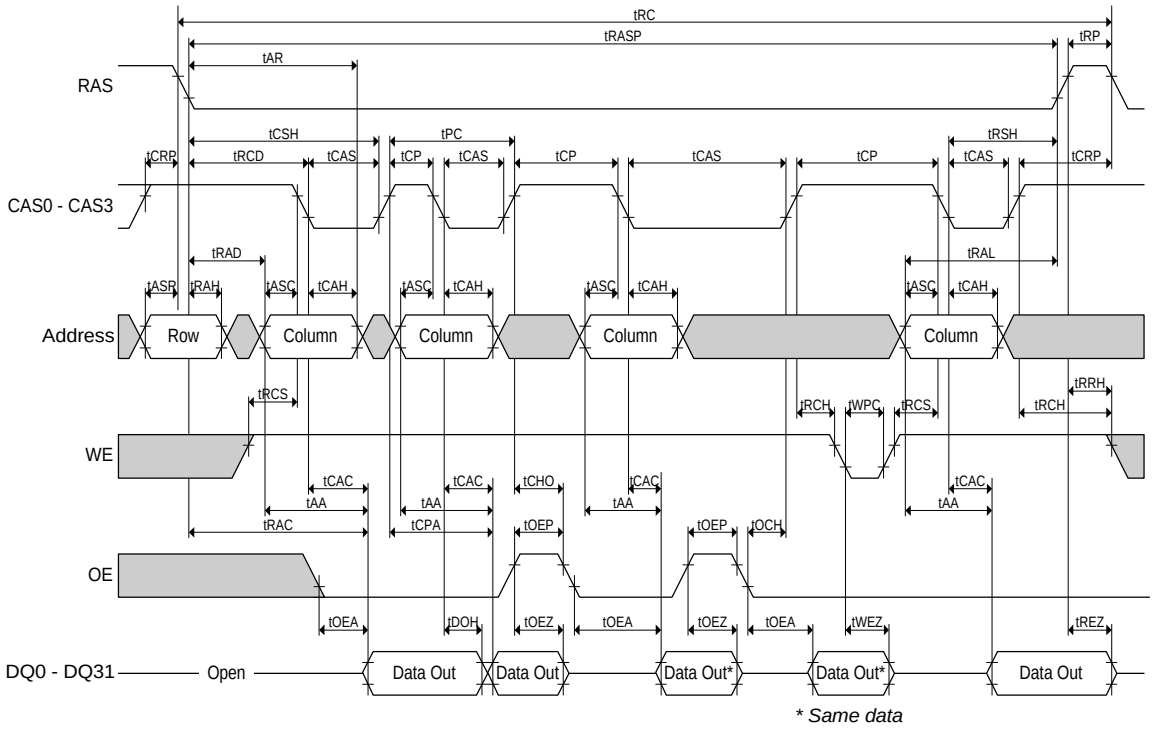
: "H" or "L"

Fast-Page-Mode Read Cycle with Extended Data Out



: "H" or "L"

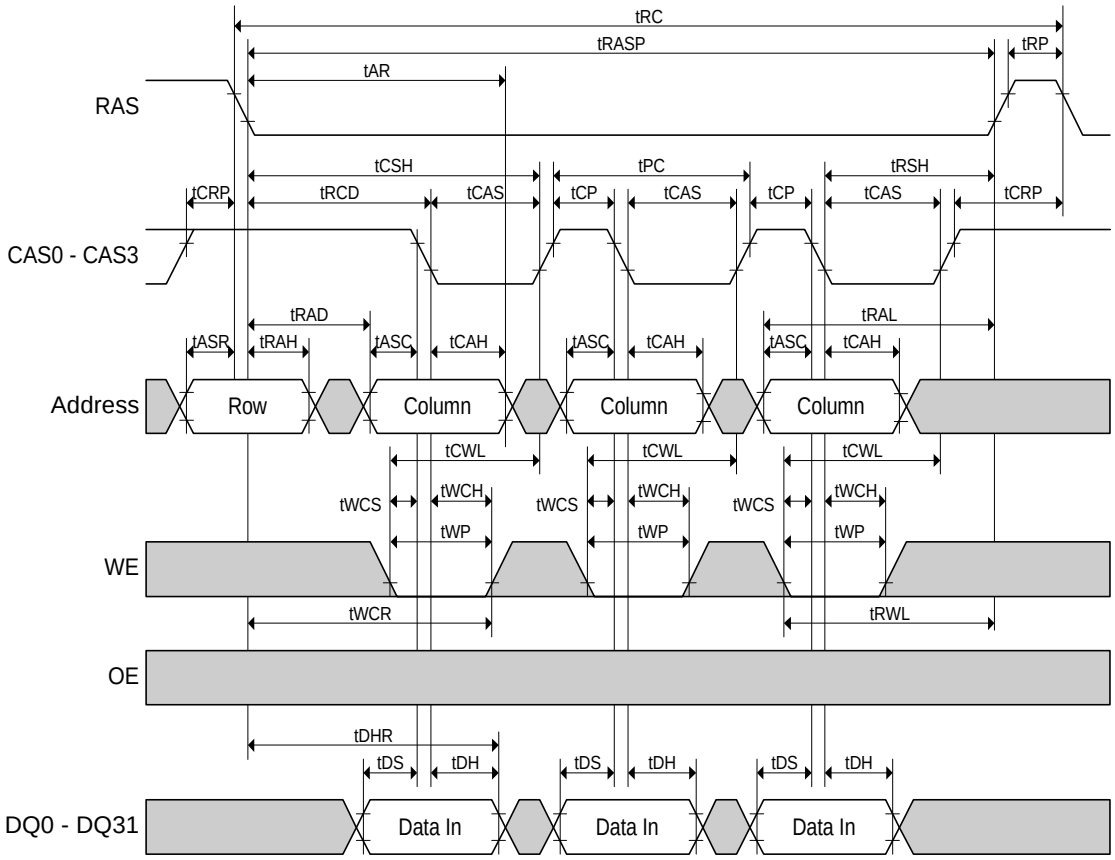
Fast-Page-Mode Read Cycle with Hi-Z Operation



* *Same data*

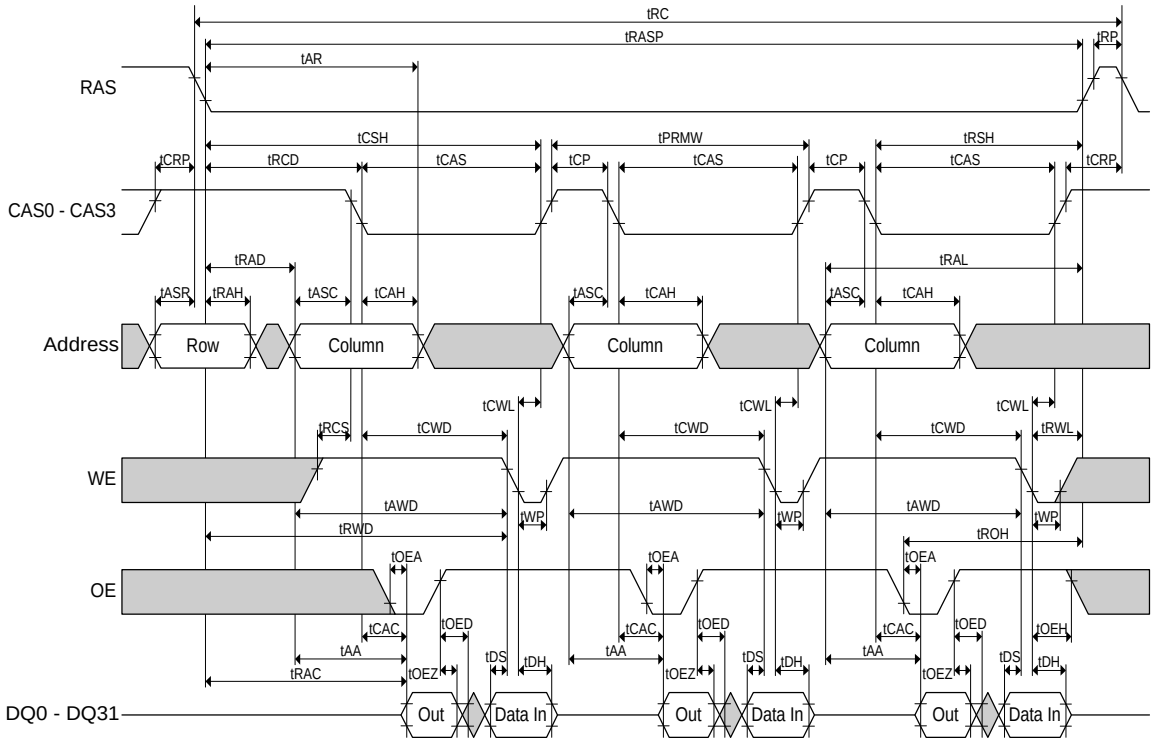
: "H" or "L"

Fast-Page-Mode Write Cycle (Early Write)



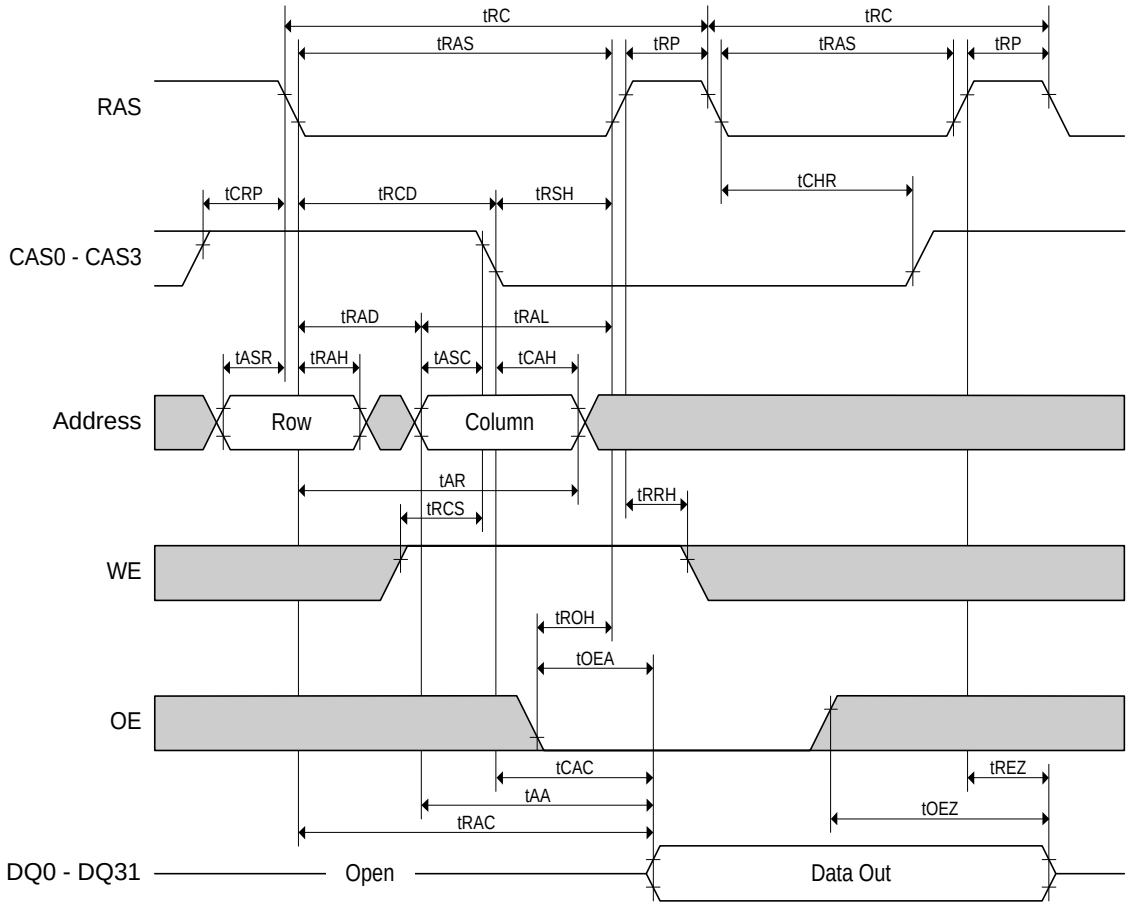
: "H" or "L"

Fast-Page-Mode Read-Modify-Write Cycle



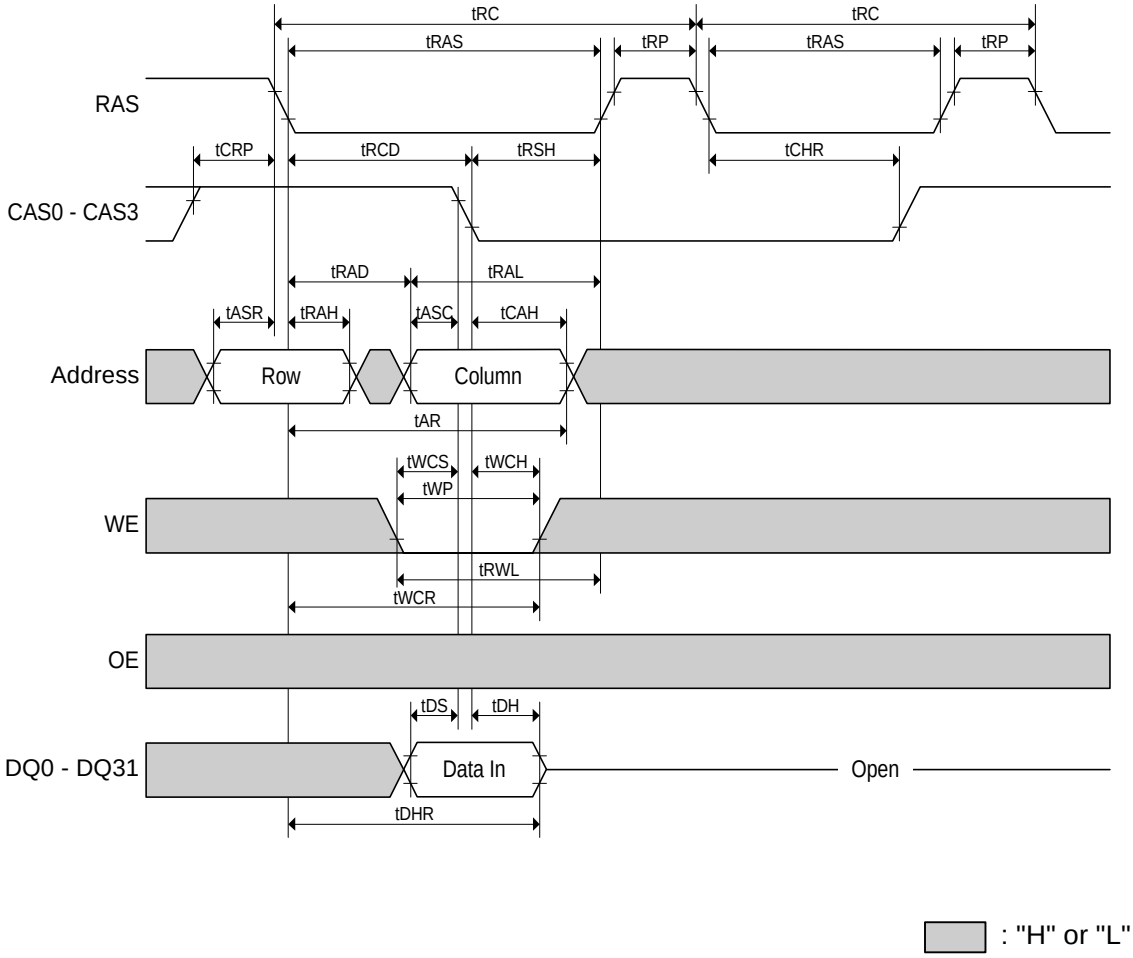
: "H" or "L"

Hidden Refresh Read Cycle

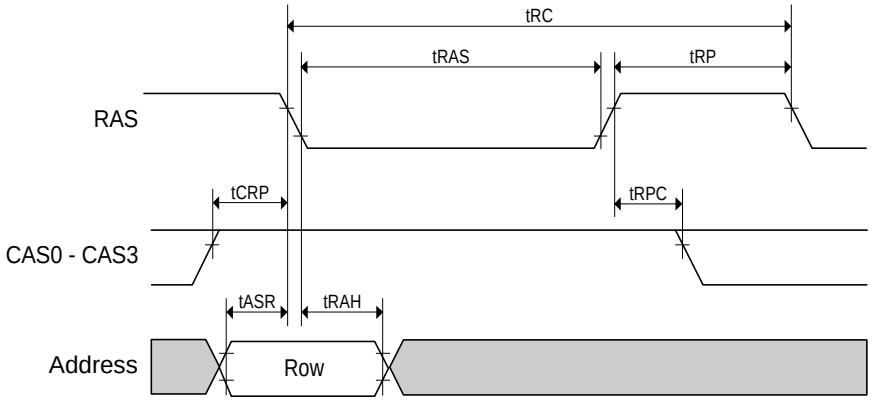


: "H" or "L"

Hidden Refresh Write Cycle

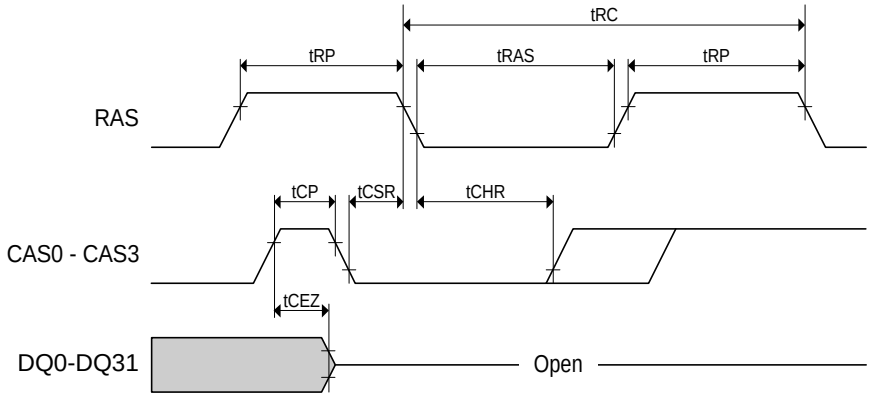


RAS-Only Refresh Cycle



Note: DQ's are open; WE and OE = "H" or "L"

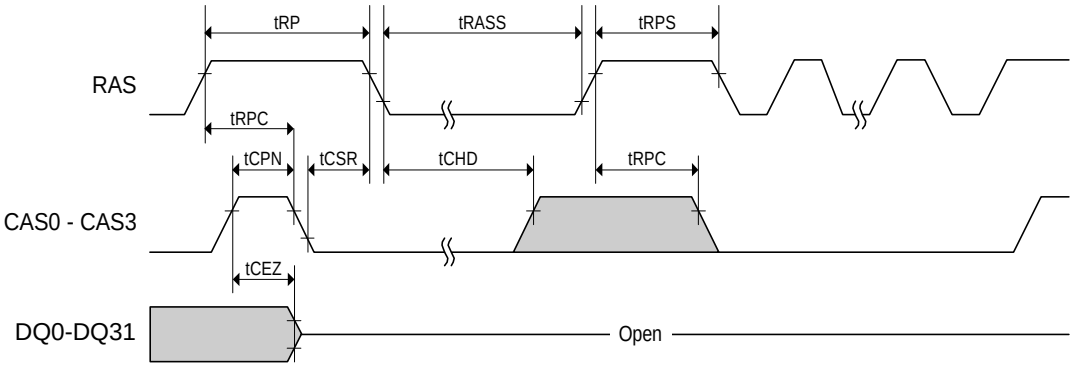
CAS-Before-RAS Refresh Cycle



Note: WE, OE and Address = "H" or "L".

: "H" or "L"

Self Refresh Cycle (S Version only)



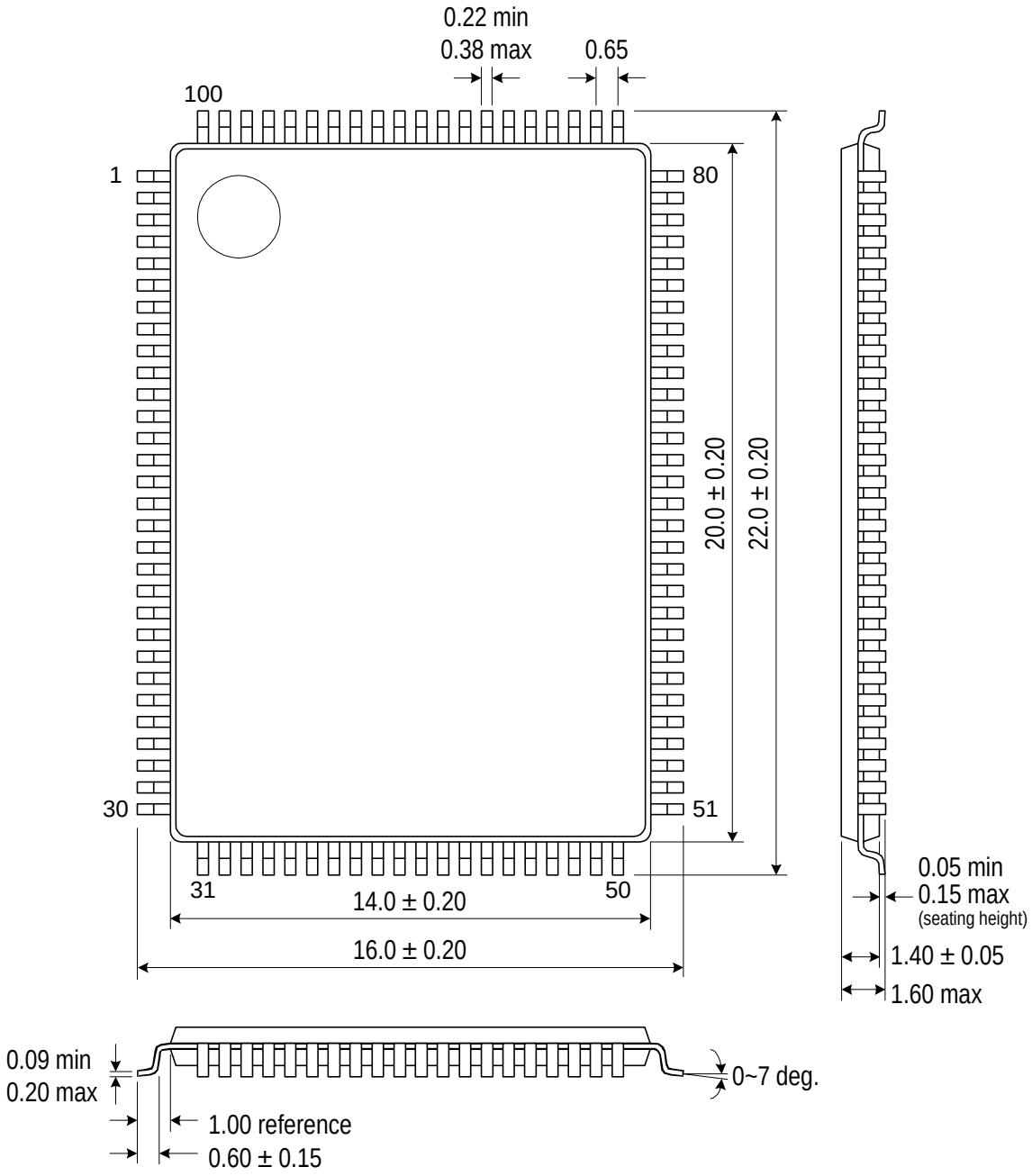
Note: 1. WE, OE and Address = "H" or "L".

2. After t_{RPS} has been satisfied, a complete burst of all 512 rows should be executed.

: "H" or "L"

Package Information

100-Pin LQFP



Note: Dimensions are given in millimeters.