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The S-29LX94A Series is low power 1K/2K/4K-bit serial E<sup>2</sup>PROMs with a low operating voltage range. They are organized as 64-word×16-bit, 128-word×16-bit and 256-word×16-bit, respectively. Each is capable of sequential read, where addresses are automatically incremented in 16-bit blocks.

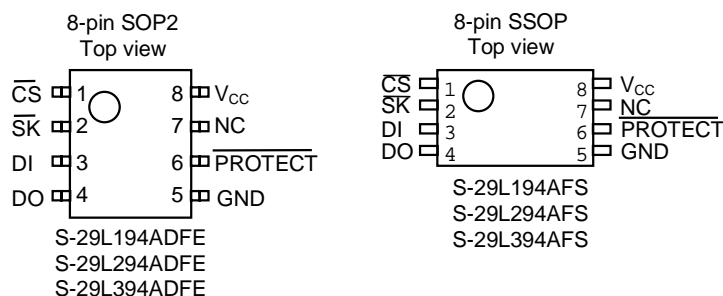
The S-29LX94A Series is capable of protecting the memory, 50% of which can be protected starting from address 00.

Interface is structured so that this IC can be directly connected to the CPU with serial ports. 8-bit instructions make it easy to prepare your own software.

## ■ Features

- Low power consumption
  - Standby : 0.8  $\mu$ A Max. ( $V_{CC}=5.5$  V)
  - Operating : 0.8 mA Max. ( $V_{CC}=5.5$  V)
  - 0.4 mA Max. ( $V_{CC}=2.7$  V)
- Low operating voltage range
  - Write : 1.8 to 5.5 V
  - Read : 1.8 to 5.5 V
- Sequential read capable
- Memory Protection
- Can be easily connected to the serial port
- CS Active "L"
- Endurance :  $10^5$  cycles/word
- Data retention : 10 years
- S-29L194A : 1 Kbits
- S-29L294A : 2 Kbits
- S-29L394A : 4 Kbits

## ■ Pin Assignment



\*See ■ Dimensions

Figure 1

## ■ Pin Functions

Table 1

Name	Pin Number		Function
	SOP2	SSOP	
$\overline{CS}$	1	1	Chip select input
$\overline{SK}$	2	2	Serial clock input
DI	3	3	Serial data input
DO	4	4	Serial data output
GND	5	5	Ground
$\overline{PROTECT}$	6	6	Memory Protection Control Input Connected to GND or Open : Protection Valid Connected to Vcc : Protection Invalid
NC	7	7	No Connection
V <sub>CC</sub>	8	8	Power supply

■ Block Diagram

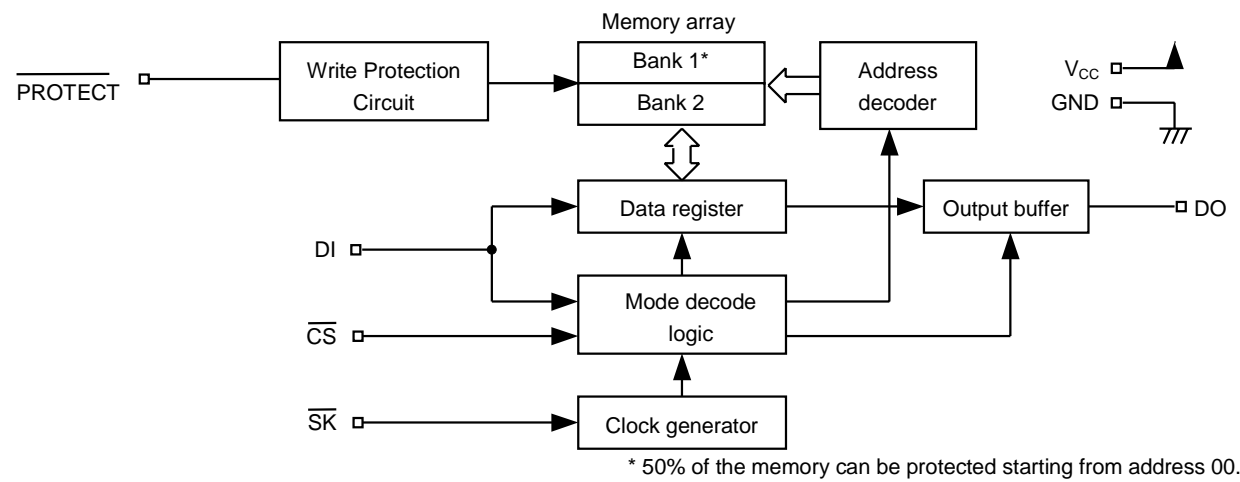


Figure 2

■ Instruction Set

Table 2

Instruction	Start Bit	Ope code	Address			Data
			S-29L194A	S-29L294A	S-29L394A	
READ (Read data)	1	1000xxx	xx A5toA0	x A6toA0	A7toA0	D <sub>15</sub> to D <sub>0</sub> Output*
PROGRAM (Program data)	1	x100xxx	xx A5toA0	x A6toA0	A7toA0	D <sub>15</sub> to D <sub>0</sub> Input
PEN (Program enable)	1	0011xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—
PDS (Program disable)	1	0000xxx	xxxxxxxx	xxxxxxxx	xxxxxxxx	—

x: Doesn't matter.

\*: When 16-bit data of the specified address is output, the data of the next address is output.

■ Absolute Maximum Ratings

Table 3

Parameter	Symbol	Ratings	Unit
Power supply voltage	V <sub>CC</sub>	−0.3 to +7.0	V
Input voltage	V <sub>IN</sub>	−0.3 to V <sub>CC</sub> +0.3	V
Output voltage	V <sub>OUT</sub>	−0.3 to V <sub>CC</sub>	V
Storage temperature under bias	T <sub>bias</sub>	−50 to +95	°C
Storage temperature	T <sub>stg</sub>	−65 to +150	°C

■ Recommended Operating Conditions

Table 4

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	Read Operation	1.8	—	5.5	V
		Write Enable/Disable				
		Write Operation	1.8	—	5.5	V
High level input voltage	VIH		0.8×VCC	—	VCC	V
Low level input voltage	VIL		0.0	—	0.2×VCC	V
Operating temperature	Topr		−40	—	+85	°C

■ **Pin Capacitance**

**Table 5**

(Ta=25°C, f=1.0 MHz, V<sub>CC</sub>=5 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> =0 V	—	—	8	pF
Output Capacitance	C <sub>OUT</sub>	V <sub>OUT</sub> =0 V	—	—	10	pF

■ **Endurance**

**Table 6**

Parameter	Symbol	Min.	Typ.	Max.	Unit
Endurance	N <sub>W</sub>	10 <sup>5</sup>	—	—	cycles/word

■ **DC Characteristics**

**Table 7**

Parameter	Smb1	Conditions	V <sub>CC</sub> =4.5 to 5.5 V			V <sub>CC</sub> =2.7 to 4.5 V			V <sub>CC</sub> =1.8 to 2.7 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Current consumption (READ)	I <sub>CC1</sub>	DO unloaded	—	—	0.8	—	—	0.6	—	—	0.4	mA
Current consumption (PROGRAM)	I <sub>CC2</sub>	DO unloaded	—	—	2.0	—	—	1.5	—	—	1.0	mA

**Table 8**

Parameter	Smb	Conditions	V <sub>CC</sub> =4.5 to 5.5 V			V <sub>CC</sub> =2.7 to 4.5 V			V <sub>CC</sub> =1.8 to 2.7 V			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Standby current consumption	I <sub>SB</sub>	CS=V <sub>CC</sub> DO=Open Other input: Connected Qto V <sub>CC</sub> or GND	—	—	0.8	—	—	0.6	—	—	0.4	μA
Input leakage current	I <sub>LI</sub>	V <sub>IN</sub> =GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Output leakage current	I <sub>LO</sub>	V <sub>OUT</sub> =GND to V <sub>CC</sub>	—	0.1	1.0	—	0.1	1.0	—	0.1	1.0	μA
Low level output voltage	V <sub>OL</sub>	I <sub>OL</sub> =2.1 mA	—	—	0.45	—	—	—	—	—	—	V
		I <sub>OL</sub> =100 μA	—	—	0.1	—	—	0.1	—	—	0.1	V
High level output voltage	V <sub>OH</sub>	I <sub>OH</sub> = - 400 μA	2.4	—	—	—	—	—	—	—	—	V
		I <sub>OH</sub> = - 100 μA	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.7	—	—	—	—	—	V
		I <sub>OH</sub> = - 10 μA	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.7	—	—	V <sub>CC</sub> -0.3	—	—	V
Write enable latch data hold voltage	V <sub>DH</sub>	Only when write disable mode	1.5	—	—	1.5	—	—	1.5	—	—	V
Pull-down current	I <sub>PD</sub>	PROTECT Terminal=V <sub>CC</sub>	15	—	80	4	—	50	1	—	15	μA

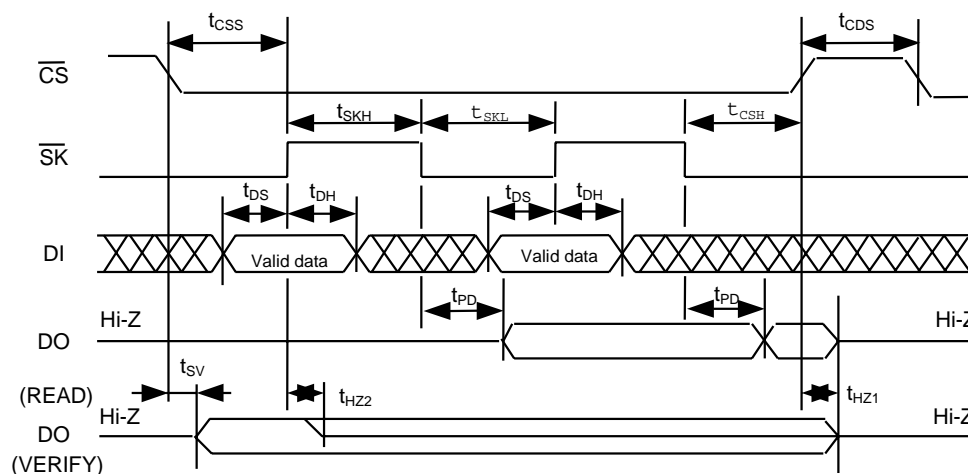
■ AC Characteristics

**Table 9 Measuring conditions**

Input pulse voltage	$0.1 \times V_{CC}$ to $0.9 \times V_{CC}$
Output reference voltage	$0.5 \times V_{CC}$
Output load	100pF

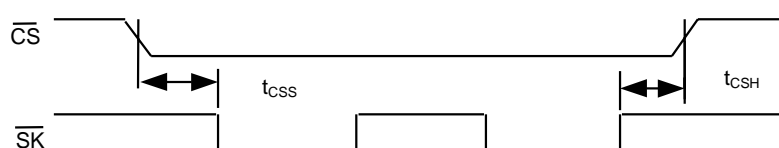
**Table 10**

Parameter	Smb1	$V_{CC}=4.5$ to $5.5V$			$V_{CC}=2.7$ to $4.5 V$			$V_{CC}=1.8$ to $2.7V$			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
CS setup time	$t_{CSS}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu s$
CS hold time	$t_{CSH}$	0.2	—	—	0.4	—	—	1.0	—	—	$\mu s$
CS deselect time	$t_{CDS}$	0.2	—	—	0.2	—	—	0.4	—	—	$\mu s$
Data setup time	$t_{DS}$	0.2	—	—	0.4	—	—	0.8	—	—	$\mu s$
Data hold time	$t_{DH}$	0.2	—	—	0.4	—	—	0.8	—	—	$\mu s$
Output delay time	$t_{PD}$	—	—	0.4	—	—	1.0	—	—	2.0	$\mu s$
Clock frequency	$f_{SK}$	0	—	2.0	0	—	0.5	—	—	0.25	MHz
Clock pulse width	$t_{SKH}$ $t_{SKL}$	0.25	—	—	1.0	—	—	2.0	—	—	$\mu s$
Output disable time	$t_{HZ1}$ $t_{HZ2}$	0	—	0.15	0	—	0.5	0	—	1.0	$\mu s$
Output enable time	$t_{SV}$	0	—	0.15	0	—	0.5	0	—	1.0	$\mu s$
Programming time	$t_{PR}$	—	4.0	10.0	—	4.0	10.0	—	4.0	10.0	ms



Input data is retrieved on the rising edge of  $\overline{SK}$ .  
Output data is triggered on the falling edge of  $\overline{SK}$ .

**Figure 3 Timing Chart**



**Figure 4 Timing Chart for  $t_{CSS}$  and  $t_{CSH}$  when  $\overline{SK}$  is "H"**

## ■ Operation

Instructions (in the order of start-bit, instruction, address, and data) are latched to DI in synchronization with the rising edge of  $\overline{SK}$  after  $\overline{CS}$  goes low. A start-bit can only be recognized when the high of DI is latched at the rising edge of  $\overline{SK}$  after changing  $\overline{CS}$  to low, it is impossible for it to be recognized as long as DI is low, even if there are  $\overline{SK}$  pulses after  $\overline{CS}$  goes low. Instruction finishes when  $\overline{CS}$  goes high, where it must be high between commands during  $t_{CDS}$ .

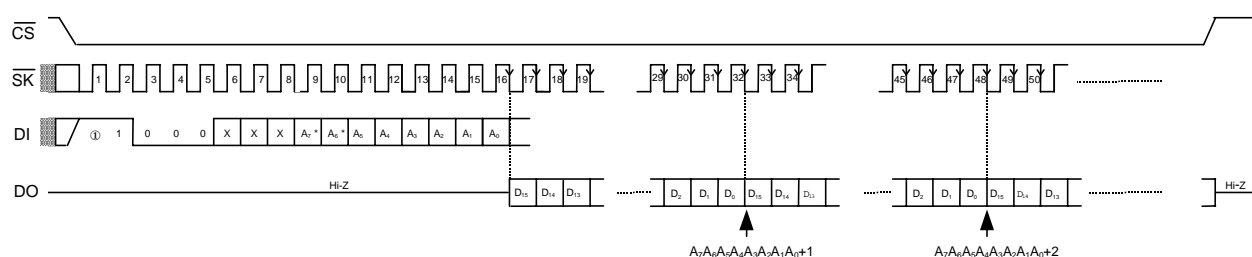
All input, including DI and  $\overline{SK}$  signals, is ignored while  $\overline{CS}$  is high, which is stand-by mode. The start bit + instruction, address, and data are 8-bit instructions. This makes it easy to prepare your own software using a serial interface incorporated into the CPU.

### 1. READ

The READ instruction reads data from a specified address. After A0 is latched at the rising edge of  $\overline{SK}$ , 16-bit data is continuously output in synchronization with the falling edge of  $\overline{SK}$ .

When all of the data ( $D_{15}$  to  $D_0$ ) in the specified address has been read, data in the next address can be read with the input of another  $\overline{SK}$  clock. Thus, the data over whole area of the memory can be read by continuously inputting  $\overline{SK}$  clocks as long as  $\overline{CS}$  is low.

The last address ( $A_n \dots A_1 A_0 = 1 \dots 11$ ) rolls over to the top address ( $A_n \dots A_1 A_0 = 0 \dots 00$ )



\* On the S-29L194A,  $A_7$  and  $A_6$  are optional.  
On the S-29L294A,  $A_7$  is optional.

Figure 5 Read Timing (S-29L394A)

## 2. PROGRAM

The PROGRAM instruction automatically begins writing to the non-volatile memory when  $\overline{CS}$  goes high at the completion of the specified clock input.

The write operation is completed in 10 ms ( $t_{PR}$  Max.), and the typical write period is less than 5 ms. In the S-29LX94A Series, it is easy to VERIFY the completion of the write operation in order to minimize the write cycle by setting  $\overline{CS}$  to low and checking the DO pin, which is low during the write operation and high after its completion. This VERIFY procedure can be executed over and over again.

There are two methods to detect a change in the DO output. One is to detect a change from low to high setting  $\overline{CS}$  to low, and the other is to detect a change from low to high as a result of repetitious operations of returning the  $\overline{CS}$  to high after setting  $\overline{CS}$  to low and checking the DO output.

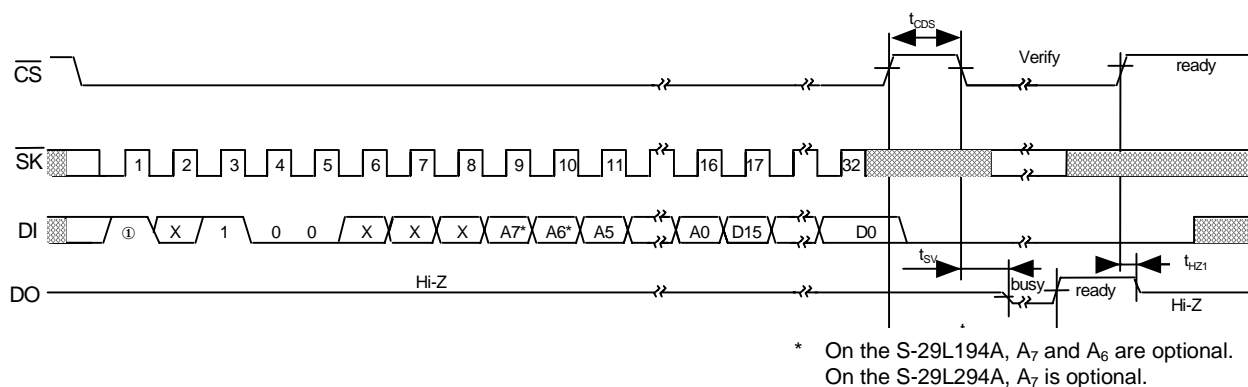
Because all  $\overline{SK}$  and DI inputs are ignored during the write operation, any input of instruction will also be disregarded. When DO outputs high after completion of the write operation or if it is in the high-impedence state (Hi-Z), the input of instructions is available. Even if the DO pin remains high, it will enter the high-impedence state upon the recognition of a high of DI (start-bit) attached to the rising edge of an  $\overline{SK}$  pulse.

DI input should be low during the VERIFY procedure.

### 2.1 PROGRAM

This instruction writes 16-bit data to a specified address.

After changing  $\overline{CS}$  to low, input a start-bit, op-code (PROGRAM), address, and 16-bit data. If there is a data overflow of more than 16 bits, only the last 16-bits of the data is considered valid. Changing  $\overline{CS}$  to high will start the PROGRAM operation. It is not necessary to make the data "1" before initiating the PROGRAM operation.



**Figure 6 WRITE Timing (S-29L394A)**

### 3. Write enable (PEN) and Write disable (PDS)

The PEN instruction puts the S-29LX94A Series into write enable mode, which accepts PROGRAM instruction. The PDS instruction puts the S-29LX94A Series into write disable mode, which refuses PROGRAM instruction. The S-29LX94A Series powers on in write disable mode, which protects data against unexpected, erroneous write operations caused by noise and/or CPU malfunctions. It should be kept in write disable mode except when performing write operations.

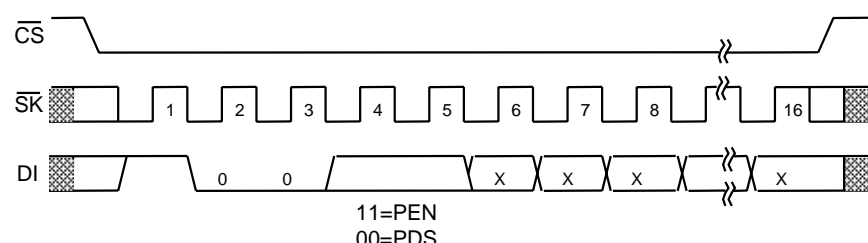


Figure 7 PEN/PDS Timing

#### ■ Receiving a Start-Bit

A start-bit can be recognized by latching the high level of DI at the rising edge of  $\overline{SK}$  after changing  $\overline{CS}$  to low (Start-Bit Recognition). The write operation begins by inputting the write instruction and setting  $\overline{CS}$  to high. The DO pin then outputs low during the write operation and high at its completion by setting  $\overline{CS}$  to low (Verify Operation). Therefore, only after a write operation, in order to accept the next command by having  $\overline{CS}$  go low, the DO pin is switched from a state of high-impedence to a state of data output; but if it recognizes a start-bit, the DO pin returns to a state of high-impedence (see Figure 3).

Make sure that data output from the CPU does not interfere with the data output from the serial memory IC when you configure a 3-wire interface by connecting DI input pin and DO output pin. Such interference may cause a start-bit fetch problem.

#### ■ Three-wire Interface (DI-DO direct connection)

Although the normal configuration of a serial interface is a 4-wire interface to  $\overline{CS}$ ,  $\overline{SK}$ , DI, and DO, a 3-wire interface is also a possibility by connecting DI and DO. However, since there is a possibility that the DO output from the serial memory IC will interfere with the data output from the CPU with a 3-wire interface, install a resistor between DI and DO in order to give preference to data output from the CPU to DI (See Figure 8).

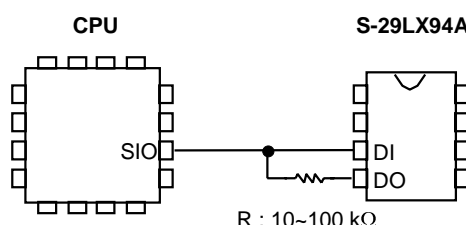


Figure 8 3-wire interface



■ Connecting to the CPU with a Serial Port

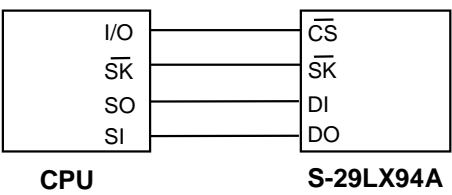


Figure 9 Connectin Example

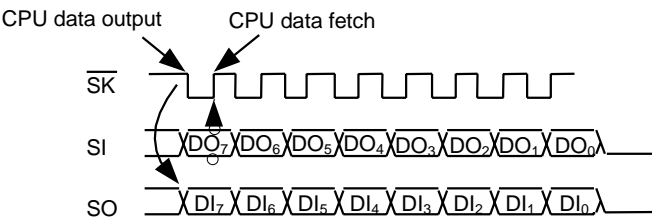


Figure 10 Serial Shift Timing

■ Memory Protection

The S-29LX94A Series is capable of protecting the memory. So, the contents of the memory will not be miswritten due to error run or malfunction of the CPU. When the  $\overline{\text{PROTECT}}$  terminal is connected to GND or OPEN, write to Bank 1 in the memory array is prohibited (50% of the memory can be protected starting from address 00). Because the pull-down resistance is connected to the  $\overline{\text{PROTECT}}$  terminal internally, the memory can be automatically protected when the  $\overline{\text{PROTECT}}$  terminal is OPEN. When the protection is valid, the data in the memory of Bank 1 will not be rewritten. However, because the write control circuit inside the IC functions, the next instruction cannot be executed during the time period of writing ( $t_{PR}$ ). While write instruction is being input and write is being executed, always connect the  $\overline{\text{PROTECT}}$  terminal to "H," "L" or OPEN, and leave the input signal unchanged (see Figure 11).

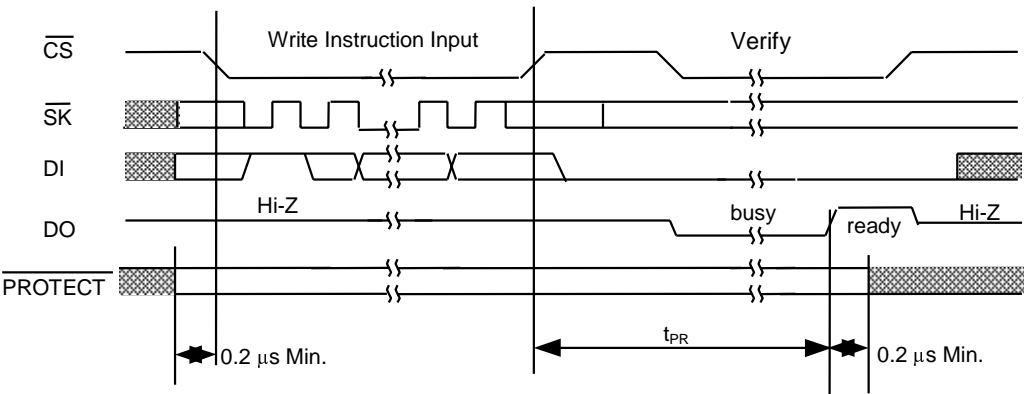


Figure 11  $\overline{\text{PROTECT}}$  Terminal Input Signal Timing

■ Dimensions (Unit : mm)

1. 8-pin SOP

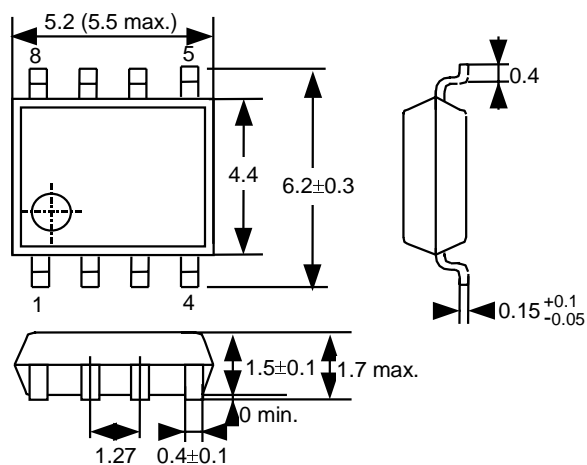


Figure 12

2. 8-pin SSOP

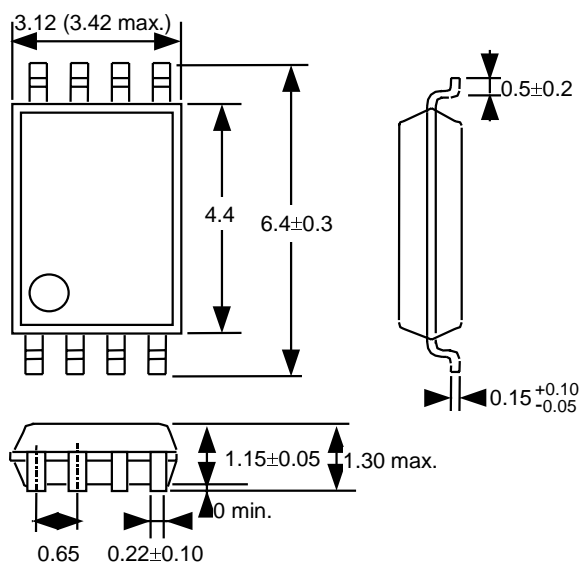
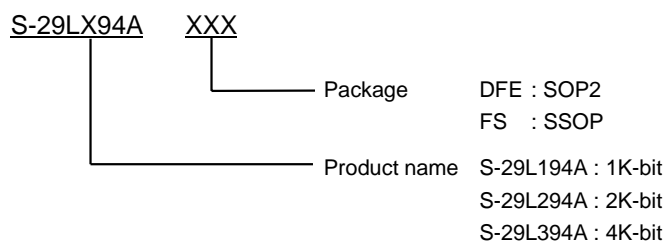


Figure 13

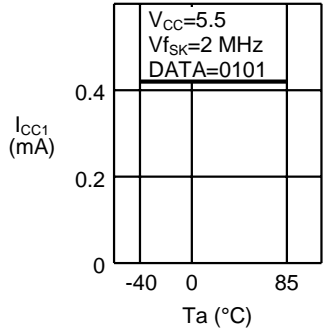
■ Ordering Information



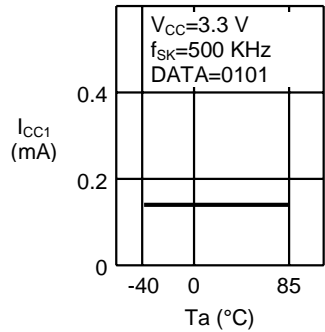
■ Characteristics

1. DC Characteristics

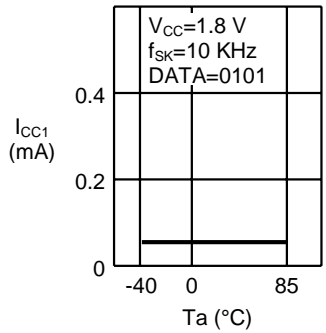
1.1 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



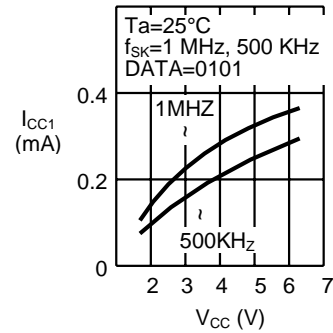
1.2 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



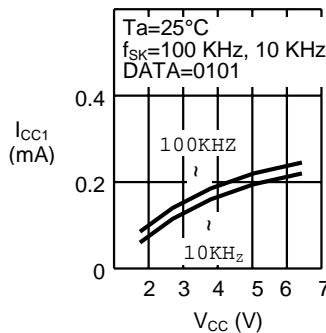
1.3 Current consumption (READ)  $I_{CC1}$  — Ambient temperature  $T_a$



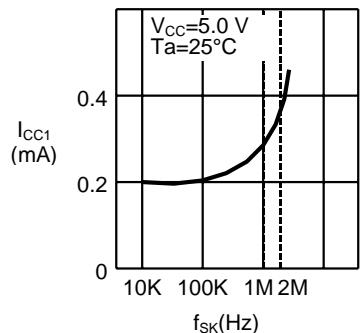
1.4 Current consumption (READ)  $I_{CC1}$  — Power supply voltage  $V_{CC}$



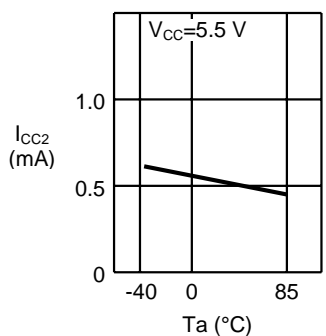
1.5 Current consumption (READ)  $I_{CC1}$  — Power supply voltage  $V_{CC}$



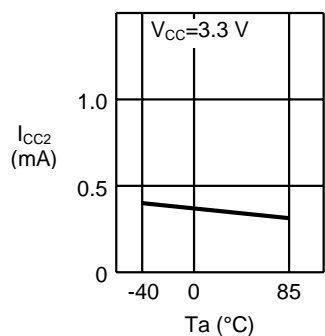
1.6 Current consumption (READ)  $I_{CC1}$  — Clock frequency  $f_{SK}$



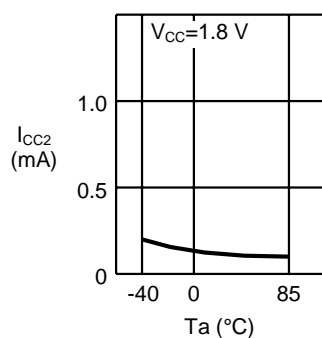
1.7 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



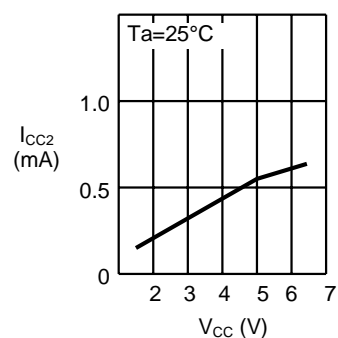
1.8 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



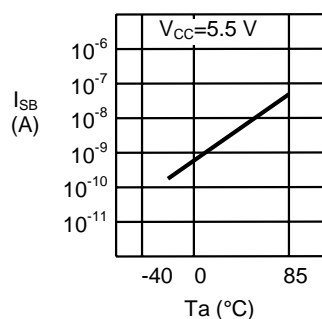
1.9 Current consumption (PROGRAM)  $I_{CC2}$  — Ambient temperature  $T_a$



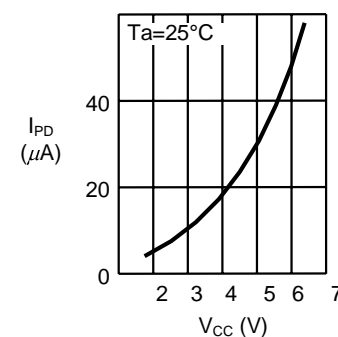
1.10 Current consumption (PROGRAM)  $I_{CC2}$  — Power supply voltage  $V_{CC}$



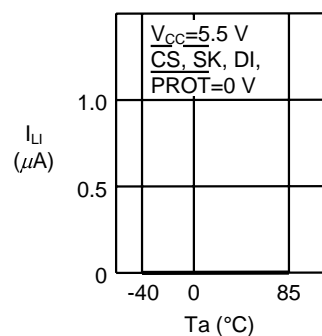
1.11 Standby current consumption  $I_{SB}$  — Ambient temperature  $T_a$



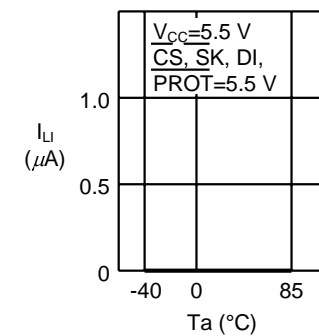
1.12 Pull-Down current  $I_{PD}$  — Power supply voltage  $V_{CC}$



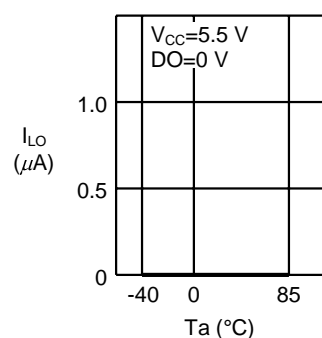
1.13 Input leakage current  $I_{LI}$  — Ambient temperature  $T_a$



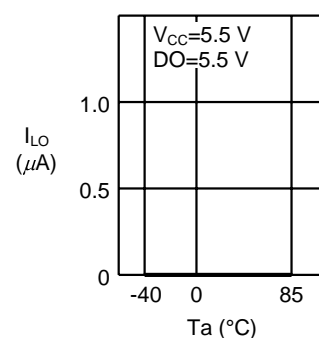
1.14 Input leakage current  $I_{LI}$  — Ambient temperature  $T_a$



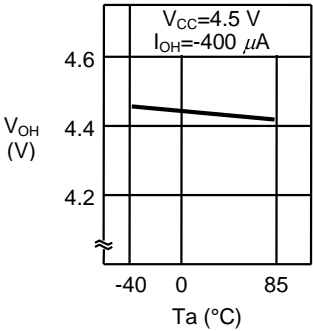
1.15 Output leakage current  $I_{LO}$  — Ambient temperature  $T_a$



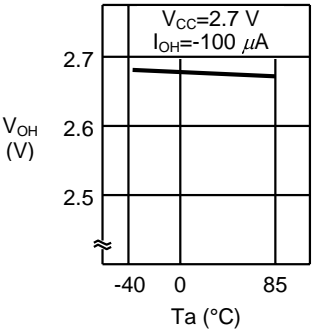
1.16 Output leakage current  $I_{LO}$  — Ambient temperature  $T_a$



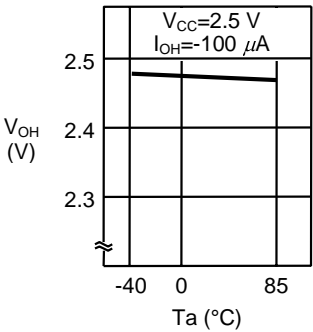
1.17 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



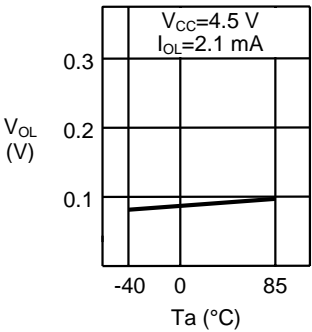
1.18 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



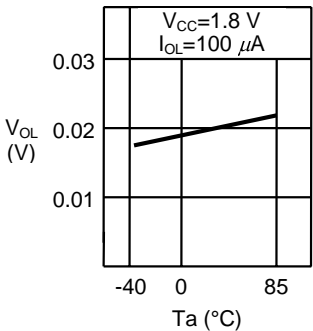
1.19 High level output voltage  $V_{OH}$  – Ambient temperature  $T_a$



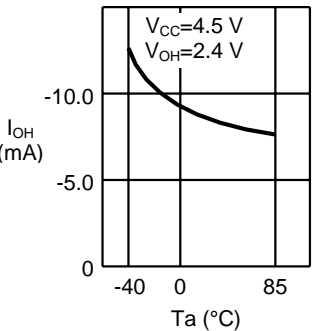
1.20 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



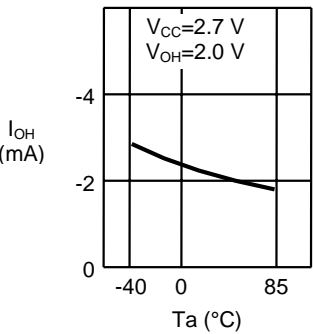
1.21 Low level output voltage  $V_{OL}$  – Ambient temperature  $T_a$



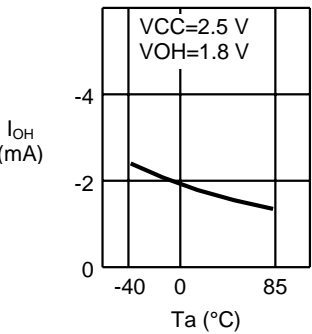
1.22 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



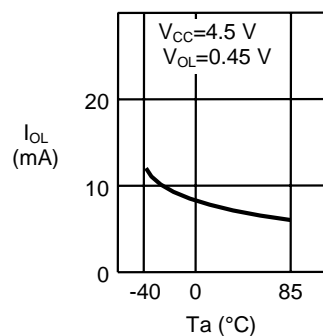
1.23 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



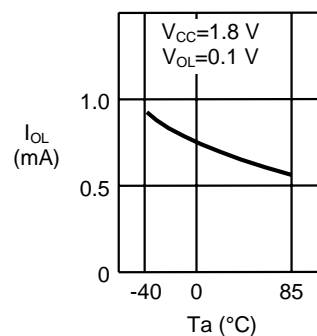
1.24 High level output current  $I_{OH}$  – Ambient temperature  $T_a$



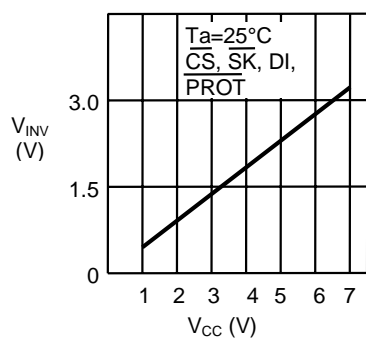
1.25 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



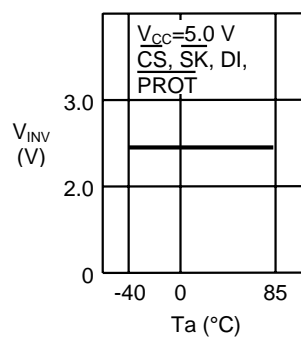
1.26 Low level output current  $I_{OL}$  – Ambient temperature  $T_a$



1.27 Input inversion voltage  $V_{INV}$  – Power supply voltage  $V_{CC}$

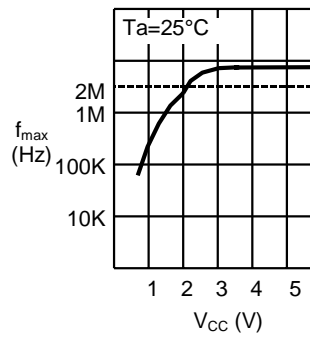


1.28 Input inversion voltage  $V_{INV}$  – Ambient temperature  $T_a$

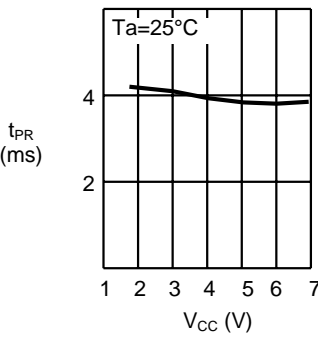


2. AC Characteristics

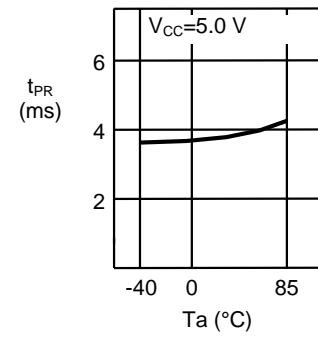
2.1 Maximum operating frequency  $f_{\max}$  –  
Power supply voltage  $V_{CC}$



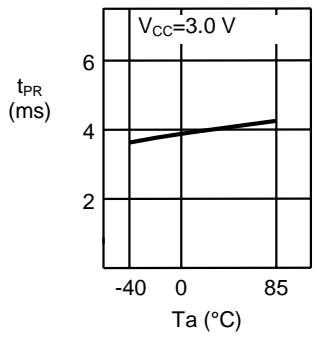
2.2 Program time  $t_{PR}$  –  
Power supply voltage  $V_{CC}$



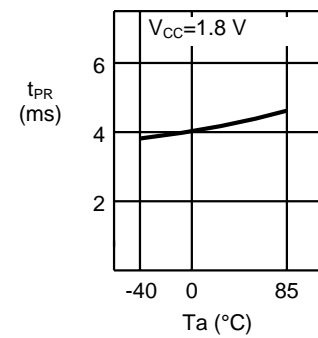
2.3 Program time  $t_{PR}$  –  
Ambient temperature  $T_a$



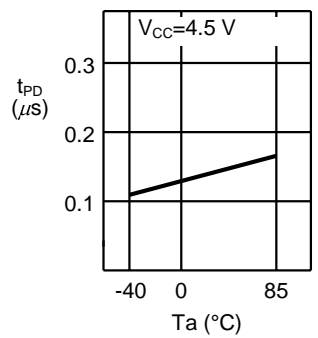
2.4 Program time  $t_{PR}$  –  
Ambient temperature  $T_a$



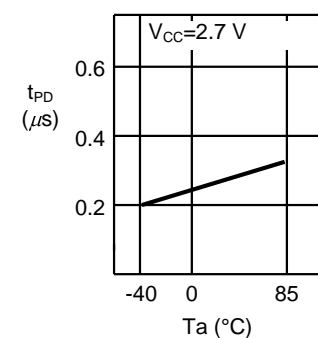
2.5 Program time  $t_{PR}$  –  
Ambient temperature  $T_a$



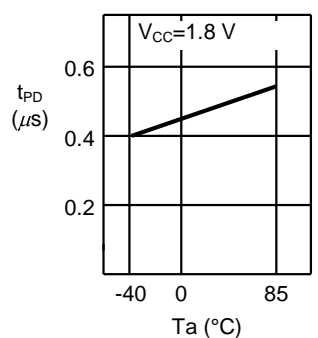
2.6 Data output delay time  $t_{PD}$  –  
Ambient temperature  $T_a$



2.7 Data output delay time  $t_{PD}$  –  
Ambient temperature  $T_a$



2.8 Data output delay time  $t_{PD}$  –  
Ambient temperature  $T_a$



# Collection of Product FAQs

Author: Ebisawa Takashi

Date: 99/01/13 (Wednesday) 18:19 (modified: 99/01/14)

## <Information level>

A: Public (Printing O.K.)  
Index: C: quality, reliability

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal No.: Overall

Related documents:

## Question:

What about the reliability and quality of the EEPROM?

## Answer:

1. The EEPROM must have a quality that is “special in a sense” and that differs from that of the other ICs.

<What is this special quality?>

- (1) Number of possible rewrites: 105 or 106

A specified minimum number of data rewrites must be assured.

- (2) Data retention: 10 years

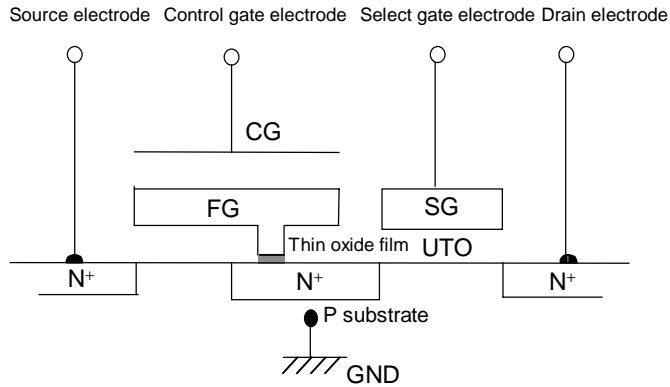
It must be ensured that written data ('1' and '0') will be stored for at least 10 years.

Ensuring (1) and (2) is very difficult in a technical sense, as well as in the sense that high quality must be maintained despite the need for mass production.

2. Why this guarantee is technically difficult

As shown in the figure below, the EEPROM functions as a non-volatile memory by holding charges in FG.





#### [Data rewrite]

Data rewrite refers to the injection or removal of electrons into or from the FG. In this process, electrons pass through a thin oxide film (UTO). The oxide film inherently acts as an insulator, but in this case the film conducts electricity (electrons are transferred).

#### [Data retention]

Data retention refers to the prevention of leakage of electrons stored in the FG. This must be assured for at least 10 years.

To meet the above stated contradictory properties, high-quality thin oxide films (UTO) must be manufactured. Such UTOs are very thin (on the order of 10 nm), and stably manufacturing them requires a very difficult technique.

#### <Remarks>

FAQ No.: 12022

# Collection of Product FAQs

Author: Ebisawa Takashi

Date: 99/01/13 (Wednesday) 18:57 (modified: 99/01/13)

## <Information level>

X: Working  
Index: A: General

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal. No.: Overall

Related documents:

## Question:

What about the distribution of application notes, usage notes, and malfunctions?

## Answer:

Distribution of application notes

All EEPROMS, including ours, may malfunction (false-writes may occur) due to an "operation in a low-voltage region upon power-on/off" or "improper recognition of a command due to a noise signal." This defect is particularly common in the voltage region of the microcomputer transmitting commands to the EEPROM, where the voltage is lower than the lowest operating voltage of the microcomputer.

To prevent this defect, usage notes have been prepared for the EEPROM.

- S-93C series, S29 series
- S-24CxxA series
- S-24CxxB series

## <Remarks>

FAQ No.: 12022

# Collection of Product FAQs

Author: Ebisawa Takashi

Date: 99/01/13 (Wednesday) 17:43 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)

Index: A: General

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

## Question:

What are some applications of the serial EEPROM?

## Answer:

### 1. Applications of the EEPROM

The applications of the EEPROM can be roughly divided into the following types:

- Tuning memory, mode setting, ID codes: Arbitrary data can easily be rewritten and data can be retained during power-off.
- Replacement of a DIP switch (from a mechanical to an electronic switch): User costs are substantially reduced.
- Adjustment data for IC elements and other electronics: The accuracy of final products is increased. Adjustments, which had been performed manually, can be automated.

### 2. Specific examples of applications

Based on the above applications, general examples are shown below. Basically, the EEPROM (a non-volatile memory) is useful for electronic applications.

[Television] TV channel memory, screen setting data, data backup during power-off  
S-24C series

[Video] VTR channel memory, program reservation data, image-quality adjustment data,  
data backup during power-off  
S-93Cx6A, S-29xx0A, S-24C series

[White goods] Maintenance data, adjustment data  
S-93Cx6A, S-29xx0A, S-24C series

[Vehicle-mounted] Troubleshooting data, maintenance data, adjustment data: Air bags, ABS,  
distance meters  
S-93Cx6A, S-29xx0A, S-24C series

[Printers] Printer maintenance data  
S-93Cx6A, S-29xx0A, S-24C series

[Modems]	Replacement of DIP switches, software (firmware) data S-93Cx6A, S-29xx0A, S-24C series
[Mobile telephones]	Personal ID, telephone-number data, address data, adjustment data S-24C series
[Pagers]	Personal ID, telephone-number data, address data S-93Cx6A, S-29Z series, S-24C series
[PC cards]	LAN cards and modem cards, replacement of dip switches, software data S-93C46A, S-29, S-24C series

<Remarks>

FAQ No.: 12021

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

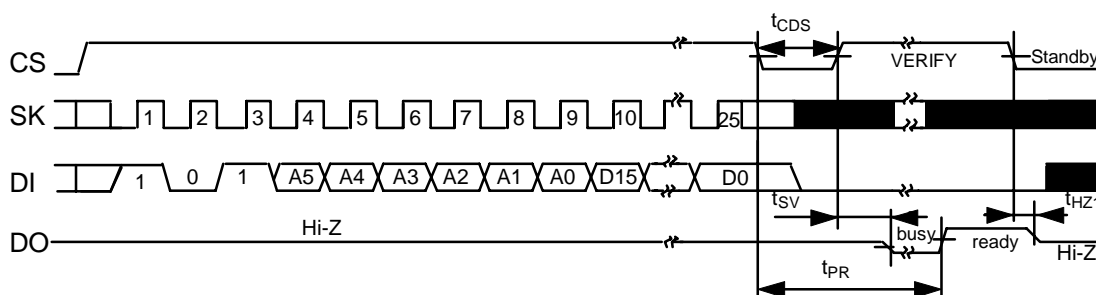
## Question:

What about the basic terms (verify, ready/busy function)?

## Answer:

Verify, ready/busy (R/B) function

This is a function to find out about an actual write operation (time). There are two methods, a “monitoring method based on the output condition of the DO pin” and a “method for monitoring the output condition of the Ready/Busy pin.” This function eliminates the need to wait 10 ms for writing to be completed, thereby minimizing the write time according to the performance of the IC (performance value: 4 ms to 5 ms; 1 ms is ensured for the S-24C series).



(Note) Note that this differs from a normal verify function, which checks written data for errors.

## <Remarks>

FAQ No.: 12018

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

## Question:

What about the basic term (page write)?

## Answer:

Page write S-24C series

Writing to memory is normally executed in addresses. With the page write function, however, writing can be executed in pages (multiple addresses). This function can improve the efficiency of write commands and reduce writing time.

Ex.:S-24C04B (4 K = 512 addresses x 8 bits) 16-byte page write function

Writing in addresses: A write time of 10 msec. x 512 = 5.1 sec. is required.

Page write: 10 msec. x 512 / 16 = 320 msec.

However, compatibility with products from other companies must be confirmed.

## <Remarks>

FAQ No.: 12017

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing)  
Index: D: Technical terms

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal. No.: Overall

Related documents:

## Question:

What about the basic terms (Test pin, ORG pin)

## Answer:

### TEST pin

This is an input pin used to enter a test mode when tests are conducted during an SII inspection process. This information is not provided to users. It can be used with a GND or Vcc connection, or in an open state (see note). This is important in maintaining compatibility with the pin layouts of other companies. Some users fear that the test mode may be inadvertently entered during operation, but such fears are unnecessary, as a potential of at least 10 V must be constantly supplied to enter the test mode.

(Note) Since the TEST pin has a C-MOS input structure, the GND or Vcc connection is most suited for this pin.

### ORG (Organization) pin

Input pin used to specify a memory configuration. A normal memory has a "16 bit/1 address" data configuration and includes no ORG pin. Competing manufacturers, however, have released products that enable data to be switched between "x16" and "x8" using "H" or "L" of the ORG pin. Since this function is provided for the 93C series of the NS code, there is a compatibility problem. SII has not yet released products featuring this function.

## <Remarks>

FAQ No.: 12014

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)  
Index: B: Technical

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal. No.: Overall

Related documents:

## Question:

Malfunction (false-write, illegal data)

## Answer:

[Malfunction of the EEPROM] (key words: false-store(illegal data))

The EEPROM may malfunction (false-store) due to power-on/off or noise from the microcomputer. The defect rate, however, is on the order of ppm. Even though, this could be a serious problem for the users and to the applications.

- This problem essentially results from users' design techniques, but the manufacturer should make efforts to prevent this defect. As the unit price continuously decreases, this is particularly important in discriminating us from our competitors.
- Improving the business techniques of the manufacturer  
Malfunction basically results from a user's inappropriate operation, so the user is the responsible party. We, however, must bear responsibility for defects in the IC. Thus, the best action to take depends on whether the user or SII is responsible for the defect. In practice, however, it is difficult to determine from a user's claim or inquiry, or through an agent, who is responsible for a defect.

In such a case, inform the Business Techniques section of the situation as soon as possible. In addition, see FAQ on other "malfunctions" for technical information.

## <Remarks>

FAQ No.: 12012



# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)  
Index: B: Technical

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal. No.: Overall

Related documents:

## Question:

Power-on clear in S-93CxxA, S-29xxxA, notes for power-on (malfunction)

## Answer:

1. This IC series has a built-in power-on clear circuit.

This circuit instantly initializes the EEPROM when the power voltage is activated. Since malfunction may occur if initialization has not been completed normally, the conditions specified below are required to activate the power voltage in order to operate the power-on clear circuit normally.

2. Notes on power-on

- ① Method for activating the power voltage

As shown in Fig. 1, activate the power voltage starting from a maximum of 0.2 V so that the power voltage reaches the operating value within the time specified as tRISE. If the operating power voltage is, for example, 5.0 V, tRISE = 200 ms, as shown in Fig. 2. Thus, the power voltage must be activated within 200 ms.

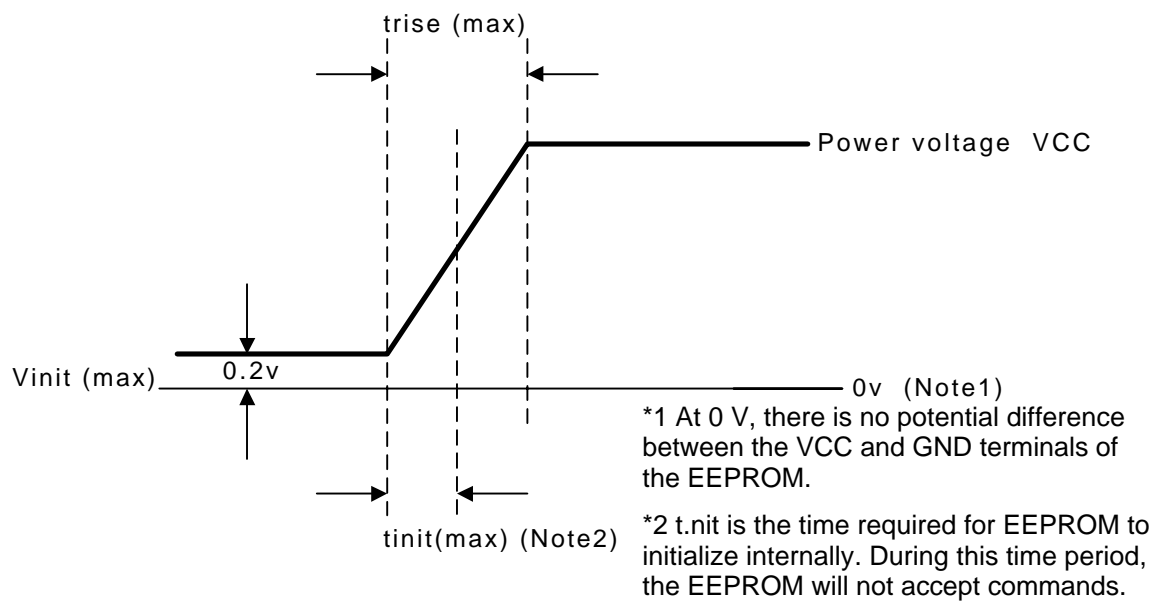


Fig. 1 Activation of the Power Voltage

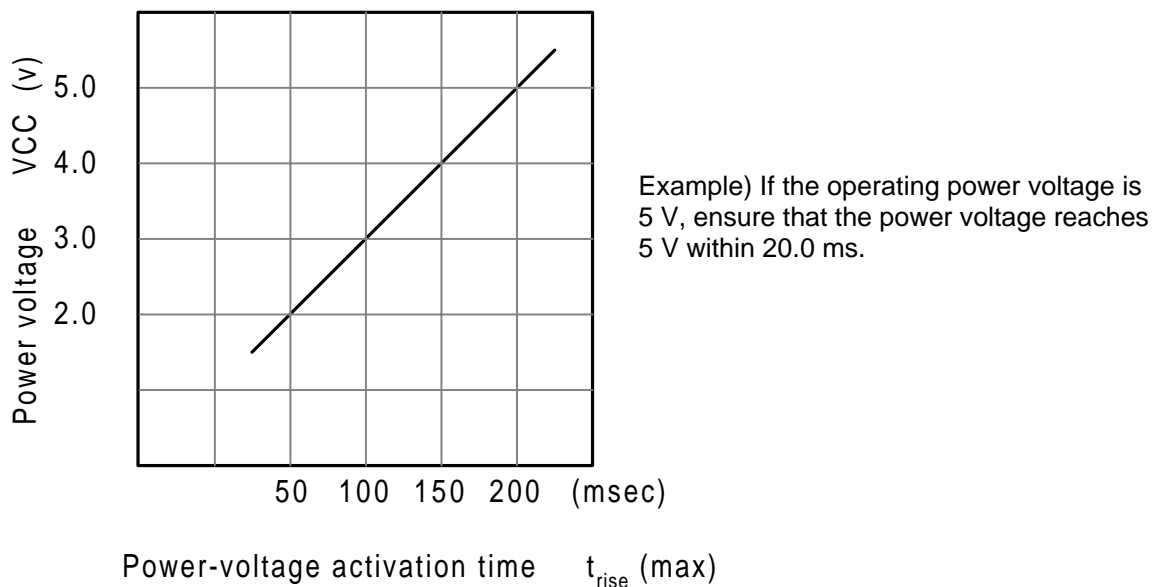


Fig. 2 Maximum power-voltage activation time

## ② Initialize time tinit

The EEPROM is instantly initialized when the power voltage is activated.

Since the EEPROM does not accept commands during initialization, the transmission of commands to the EEPROM must be started after this initialization time period.

Fig. 3 shows the time required to initialize the EEPROM.

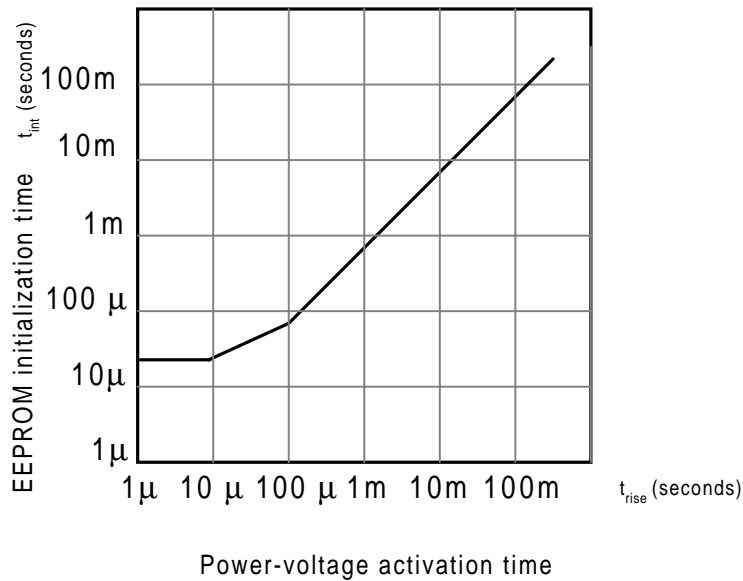


Fig. 3 EEPROM initialization time

When the power-on clear circuit has finished initialization normally, the EEPROM enters a program-disabled state. If the power-on clear circuit does not operate, the following situation is likely:

- In some cases, a previously entered command has been enabled. If, for example, a program-enabled command has been enabled and the input terminal mistakenly recognizes a write command due to extraneous noise while the next command is being entered, writing may be executed.

The following may prevent the power-on clear circuit from operating:

- If the power lines of the microcomputer and EEPROM are separated from each other, and the output terminals of the microcomputer and EEPROM are wired or connected to each other, there may be a potential difference between the power lines of the EEPROM and microcomputer. If the voltage of the microcomputer is higher, a current may flow from the output terminal of the microcomputer to the power line of the EEPROM via a parasitic diode in the DO pin of the EEPROM. Therefore, the power voltage of the EEPROM has an intermediate potential to prevent power-on from being cleared.
- During an access to the EEPROM, the voltage may decrease due to power-off. Even if the microcomputer has been reset due to a decrease in voltage, the EEPROM may malfunction if EEPROM power-on clear operation conditions are not met. For the EEPROM power-on clear operation conditions, see "Method for Activating the Power Voltage."

<Remarks>

FAQ No.: 12011

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

B: For Distri & Rep (Printing N.G.)

Index: B: Technical

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

## Question:

False-writes in S-93C, S-29 series: inadvertent activation of CS (malfunction)

## Answer:

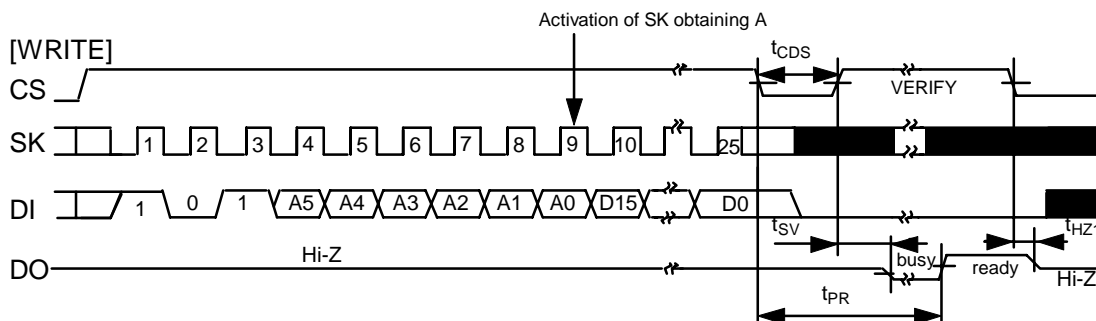
Inadvertent writing in the S-29 series

In the S-29 series, when a CS input is inadvertently activated during a write command, undefined data may be written. Relevant timings are shown below.

A command is composed of the following: "start bit + two command bits + address + (data)."

The figure below shows the timings in which commands are set (In the figure, the portion denotes the rising edge of SK.)

In the case of a write command, after a final address has been input and while 16-bit data is being input, undefined data is written when the CS input is changed from H to L.



Case in which, during a command entry, CS is changed from H to L with a timing that differs by a predetermined minimum number of clocks.

In the case of a write command, if the number of clocks is smaller than the predetermined value, data is loaded so as to be changed from D15 to D0. When, for example, CS is shifted from H to L after three clocks, data, which would otherwise have been stored in D15 to D13, is stored in D2 to D0, while undefined data is stored on the upper side a storage state in which the internal logic has been changed to either H or L). In addition, if the number of clocks is greater than the predetermined value, the last 16 pieces of data are stored correctly.

<Remarks>

FAQ No.: 12008

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)  
Index: A: General

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal. No.: Overall

Related documents:

## Question:

EEPROM compatibility table, cross reference

## Answer:

### EEPROM compatibility table

Product name	Key word	NATIONAL SEMICONDUCTOR	ATMEL	ST Micro electronic
S-29130ADPA	EE,1KB,DIP,3W	NM93C(S)46ZEN	AT93C46-10PI-2.5	ST93C46(7)AB6
S-93C46ADP	↑	↑	↑	↑
S-29130AFJA-TB	EE,1KB,SOP1,3W	NM93C(S)46ZEM8	AT93C46R-10SI-2.5	ST93C46(7)TM6013TR
S-93C46AFJ-TB	↑		↑	↑
S-29130ADFJA-TB	EE,1KB,SOP2,3W		AT93C46W-10SI-2.5	ST93C46(7)AM6013TR
S-93C46ADFJ-TB	↑		↑	↑
S-29131ADPA	EE,1KB,DIP,3W,PROT	NM93C46ZEN	AT93C46-10PI-2.5	ST93C46(7)B6
S-29131AFJA-TB	EE,1KB,SOP1,3W,PROT	NM93C46ZEM8	AT93C46R-10SI-2.5	ST93C46(7)TM6013TR
S-29220ADPA	EE,2KB,DIP,3W	NM93C(S)56ZEN	AT93C56-10PI-2.5	ST93C56(7)AB6
S-29220AFJA-TB	EE,2KB,SOP1,3W	NM93C(S)56ZEM8	AT93C56R-10SI-2.5	ST93C56(7)TM6013TR
S-29220ADFJA-TB	EE,2KB,SOP2,3W		AT93C56W-10SI-2.5	ST93C56(7)AM6013TR
S-29221ADPA	EE,2KB,DIP,3W,PROT	NM93C56ZEN	AT93C56-10PI-2.5	ST93C56(7)B6
S-29221AFJA-TB	EE,2KB,SOP1,3W,PROT	NM93C56ZEM8	AT93C56R-10SI-2.5	ST93C56(7)TM6013TR
S-29330ADPA	EE,4KB,DIP,3W	NM93C(S)66ZEN	AT93C66-10PI-2.5	ST93C66(7)AB6
S-29330AFJA-TB	EE,4KB,SOP1,3W	NM93C(S)66ZEM8	AT93C66R-10SI-2.5	ST93C66(7)TM6013TR
S-29330ADFJA-TB	EE,4KB,SOP2,3W		AT93C66W-10SI-2.5	ST93C66(7)AM6013TR
S-29331ADPA	EE,4KB,DIP,3W,PROT	NM93C66ZEN	AT93C66-10PI-2.5	ST93C66(7)B6
S-29331AFJA-TB	EE,4KB,SOP1,3W,PROT	NM93C66ZEM8	AT93C66R-10SI-2.5	ST93C66(7)TM6013TR
S-29430ADP	EE,8KB,DIP,3W			
S-29430AFE-TF	EE,8KB,SOP1,3W			
S-24C01ADPA-01	EE,1KB,DIP,2W		AT24C01A-10PI-2.5	ST24(25)C(W)01B6
S-24C01AFJA-TB-01	EE,1KB,SOP,2W		AT24C01A-10SI-2.5	ST24(25)C(W)01M6TR
S-24C02ADPA-01	EE,2KB,DIP,2W	NM24C02(03)LEN	AT24C02-10PI-2.5	ST24(25)C(W)02B6
S-24C02AFJA-TB-01	EE,2KB,SOP,2W	NM24C02(03)LEM8	AT24C02N-10SI-2.5	ST24(25)C(W)02M6TR
S-24C04ADPA-01	EE,4KB,DIP,2W	NM24C04(05)LEN	AT24C04-10PI-2.5	ST24(25)C(W)04B6

S-24C04AFJA-TB-01	EE,4KB,SOP,2W	NM24C04(05)LEM8	AT24C04N-10SI-2.5	ST24(25)C(W)04M6TR
S-24C08ADPA-01	EE,8KB,DIP,2W	NM24C08(09)LEN	AT24C08-10PI-2.5	ST24(25)C(W)08B6
S-24C08AFJA-TB-01	EE,8KB,SOP,2W	NM24C08(09)LEM8	AT24C08N-10SI-2.5	ST24(25)C(W)08M6TR
S-24C16ADPA-01	EE,16KB,DIP,2W	NM24C16(17)LEN	AT24C16-10PI-2.5	ST24(25)C(W)16B6
S-24C16AFJA-TB-01	EE,16KB,SOP,2W	NM24C16(17)LEM8	AT24C16N-10SI-2.5	ST24(25)C(W)16M6TR
S-29L130AFE-TB	EE,1KB,SOP1,3W,L/V	NM93C(S)46XLZEM8	AT93C46R-10SI-1.8	ST93C46(7)TM6013TR
S-29L130ADFE-TB	EE,1KB,SOP2,3W,L/V		AT93C46W-10SI-1.8	ST93C46(7)AM6013TR
S-29L131ADFE-TB	EE,1KB,SOP2,3W,L/V,PROT	NM93C(S)46XLZEM8	AT93C46W-10SI-1.8	ST93C46(7)AM6013TR
S-29L220AFE-TB	EE,2KB,SOP1,3W,L/V	NM93C(S)56XLZEM8	AT93C56R-10SI-1.8	ST93C56(7)TM6013TR
S-29L220ADFE-TB	EE,2KB,SOP2,3W,L/V		AT93C56W-10SI-1.8	ST93C56(7)AM6013TR
S-29L221ADFE-TB	EE,2KB,SOP2,3W,L/V,PROT	NM93C(S)56XLZEM8	AT93C56W-10SI-1.8	ST93C56(7)AM6013TR
S-29L330AFE-TB	EE,4KB,SOP1,3W,L/V	NM93C(S)66XLZEM8	AT93C66R-10SI-1.8	ST93C66(7)TM6013TR
S-29L330ADFE-TB	EE,4KB,SOP2,3W,L/V		AT93C66W-10SI-1.8	ST93C66(7)AM6013TR
S-29L331ADFE-TB	EE,4KB,SOP2,3W,L/V,PROT	NM93C(S)66XLZEM8	AT93C66W-10SI-1.8	ST93C66(7)AM6013TR

<Remarks>

FAQ No.: 12007

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13)

## <Information level>

A: Public (Printing O.K.)

Index: D (Technical terms)

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal. No.: Overall

Related documents:

## Question:

What about the basic terms (memory protect, reset, CS)?

## Answer:

Memory protect, reset → S-29xx1A, S-29x94A, S-29x55A

Function for prohibiting a write command from being executed in a certain region of the memory space. This function is enabled by controlling the protect or reset input pin (select/deselect protect). This reset prevents the microcomputer from running uncontrollably and also prevents false-writes caused by noise in order to protect data.

Ex.: Storage of ID codes and product shipment adjustment data

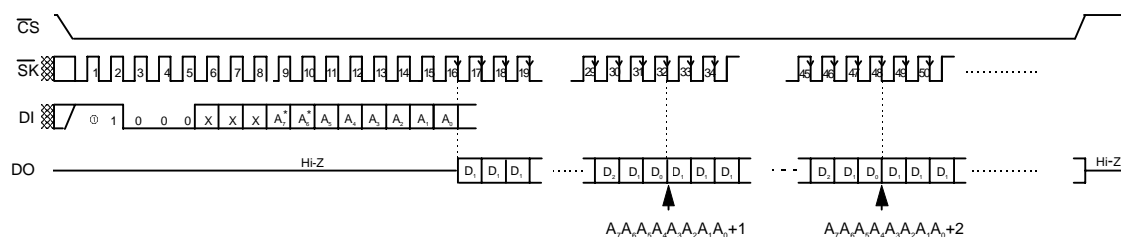
(Note) S-29xx1A and S-29x94A protect 50% of memory, starting with the leading address.

CS, /CS (/CS: S-29x55A, S-29x94A)

CS is an input pin used to select the execution of a command. It is selected using "H" and deselected using "L" (the reverse is true for /CS)

→ /CS is useful on the interface of the microcomputer (L active is mainly used for the microcomputer).

Malfunction, however, is likely to be caused by noise upon power-on if a command is executed at the GND level.





<Remarks>

FAQ No.: 12006

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

## <Information level>

A: Public (Printing O.K.)

Index: A: General

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

## Question:

Concept of the compatibility, features, and markets of the S-29 series

## Answer:

[Compatibility of the EEPROM]

In terms of memory, most SII EEPROMs are compatible with our competitors' standard products in their operation codes. If another company's product is to be replaced by a corresponding SII product, the DC/AC specifications desired by the user must be carefully determined.

The key words for the products are given below.

Our competitor's 93C-series products are compatible with SII's S-29xx0A-series products, and our competitor's 24C-series products are compatible with SII's S-24C-series products.

The key word for each company is given below.

NM93C : National Semiconductor

AT93C : ATMEL

93C : Microchip

M93C : ST Micro electronic (formerly SGS Tomson ST93C)

CAT93C : Catalyst

AK93C : Asahi Kasei

BR93C : ROHM

## <Remarks>

FAQ No.: 12005

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

<Information level>

A: Public (Printing O.K.)

Index: A: General

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

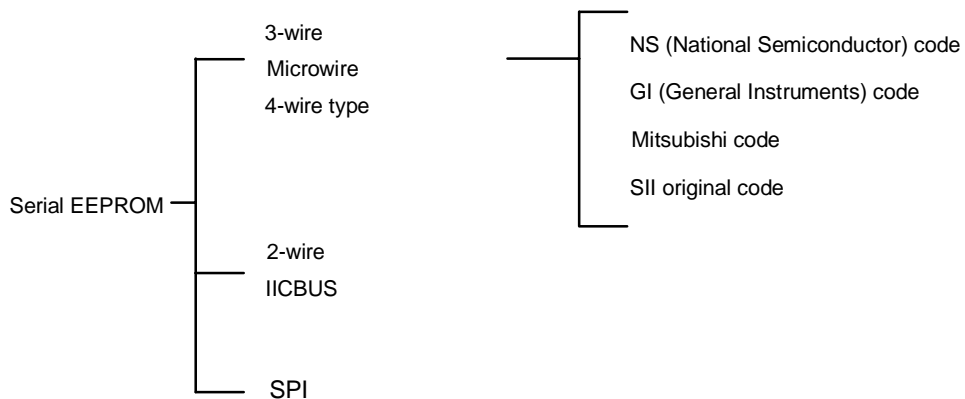
## Question:

How are operation codes classified?

A:

[EEPROM operation codes]

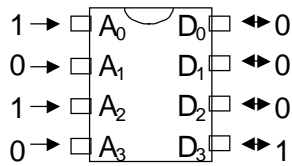
In the serial EEPROM, the operation codes can be classified into several types. Our competitors have released products compatible with each type of operation code. The key words of the operation codes are given below.



### 1. Serial and parallel

Data reading and writing are divided into serial and parallel types.

ex.: Parallel

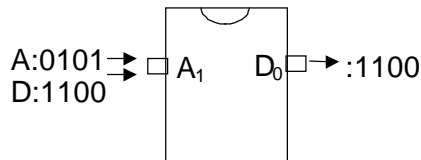


Addresses and data are processed in parallel.

[Advantage]

Fast processing

ex.: Serial



Addresses and data are processed in serial.

[Advantages]

The size can be reduced due to the reduced number of I/O terminals, and fewer wires are required for the substrate.

The package can be downsized and manufactured inexpensively.

## 2. 3-wire type, microwire, 4-wire type

Composed of four pins, including three input pins CS, SK, and DI, and an output pin DO. Since DI and DO can be directly coupled together, the EEPROM can be virtually composed of three pins (the 4-wire type includes an additional Ready/Busy pin, but is still referred to as a "3-wire type").

- ① NS code: The key word is "93Cx." Compatible with SII S-29xxOA.

General code used by many competing companies. Mass produced and low in cost.

- ② GI code

General Instrument Inc.'s original code. Its markets continue to dwindle.

- ③ Mitsubishi code: The key word is "M6M8." Compatible with SII S-29x55A. Serial-port direct-coupling type in which commands and data are composed of x8 units. Intended for the TV and VTR markets and primarily sold as a set with Mitsubishi microcomputers.

- ④ SII original code: S-29x9xA

Serial-port direct-coupling type in which commands and data are composed of x8 units. Intended for technology-oriented users.

- 3. 2-wire type, IICBUS: The key word is "24C." Compatible with SII S-24CxxA. Composed of two pins: an input pin (SCL) and an I/O pin (SDA). Phillips Inc. owns a relevant patent.

[Advantages] Fewer wires are required, and the microcomputer port can be shared with another IICBUS. TV set maker will be main market.

- 4. SPI: The key word is "25C." Not compatible with SII. Under development. Composed of four pins: three input pins CS, SCK, and SI, and an input pin SO. In the case of the EEPROM, the advantages are high speed (5 MHz at 5v) and a high capacity (128 Kbytes).

<Remarks>

FAQ No.: 12004

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

## <Information level>

A: Public (Printing O.K.)  
Index: D: Technical Terms

## <Product>

Division name: 01 IC  
Category 1: 12 Memory  
Category 2: 2. Serial EEPROM  
Cal No.: Overall

Related documents:

## Question:

What are the basic operation codes?

## Answer:

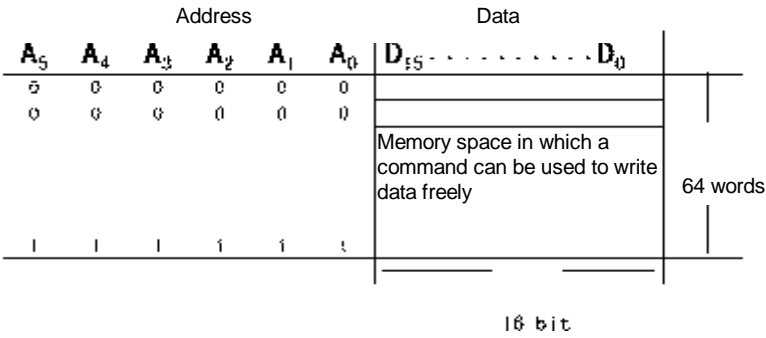
[Terms required to understand EEPROM data sheets (1)] Basic commands

- Data read, READ  
Reads data from a specified address
- Data write, WRITE or PROGRAM  
Writes data to a specified address
- Data erase, ERASE  
Erases data at a specified address (all "1"s)
- Chip write, WRAL  
Writes the same (word) data in all address spaces
- Chip erase, ERAL  
Erases data in all address spaces (all "1"s)
- Program disable, EWDS or PDS  
Prohibits write operations (WRITE), and prevents false-writes caused by noise or uncontrollable running of the CPU
- Program enable, EWES or PEN  
Enables write operations (WRITE)

### [Note]

When the power to the EEPROM is turned on, the internal circuit of the IC is reset and the program disable mode is entered. Thus, following power-on, the program enable command must be entered in order to write data.

Memory space: In the case of the S-29130A (64 words X 16 bits)



<Remarks>  
 FAQ No.: 12003

# Collection of Product FAQs

Author: Kano Tomoo

Date: 98/11/12 (Thursday) 10:17 (modified: 99/01/13(Wednesday))

## <Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

## <Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

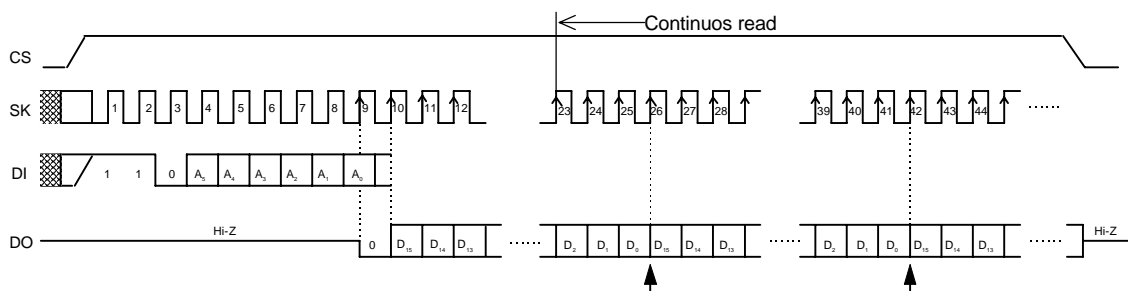
Related documents:

## Question:

What about the basic terms. (continuous read, sequential read)?

## Answer:

- Continuous read, sequential read →S-93C series, S-29 series, S-24C series  
Function by which data is read from a specified address using a read command, followed by the output of the next address. This is useful when there is a large amount of user data (ex.: ID codes).



- Serial-port direct coupling, microcomputer interface, 8-bit command  
→S-29x9xA, S-29x55A, S-2900A

The serial port is a serial I/O port provided for a microcomputer. A device that can be easily and directly coupled to this port is referred to as a "serial-port direct-coupling type" or a "microcomputer interface."

1. The EEPROM is configured as follows for simple direct coupling:
  - ① Data is input at the rising edge of the SK input clock, and output at its falling edge.
  - ② Commands and data are input and output in 8 bits.
2. A microcomputer with a serial port communicates in 8 bits (8 clocks).

This configuration can substantially reduce the number of programs required for the microcomputer. The advantages are easy programming and a reduced ROM capacity.

<Remarks>

FAQ No.: 12002



# Collection of Product FAQs

Creator: Takashi Ebisawa

Date: 98/01/13 (Wednesday) 10:51 (modified: 99/01/13(Wednesday))

<Information level>

A: Public (Printing O.K.)

Index: D: Technical terms

<Product>

Division name: 01 IC

Category 1: 12 Memory

Category 2: 2. Serial EEPROM

Cal No.: Overall

Related documents:

## Question:

What is the EEPROM?

## Answer:

1. Electrically Erasable Programmable Read Only Memory
  - Why this memory is referred to as “read only” despite the fact that it enables data to be rewritten?  
The EEPROM requires a longer time for writing than a RAM, so it is used exclusively for reading.
  - What is the “memory”?  
Elements storing data. Data is generally represented by the digits “0” and “1.”
  - What is the “ROM”?  
Read Only Memory  
Reference: RAM is Random Access read write Memory.

<Remarks>

FAQ No.: 12001